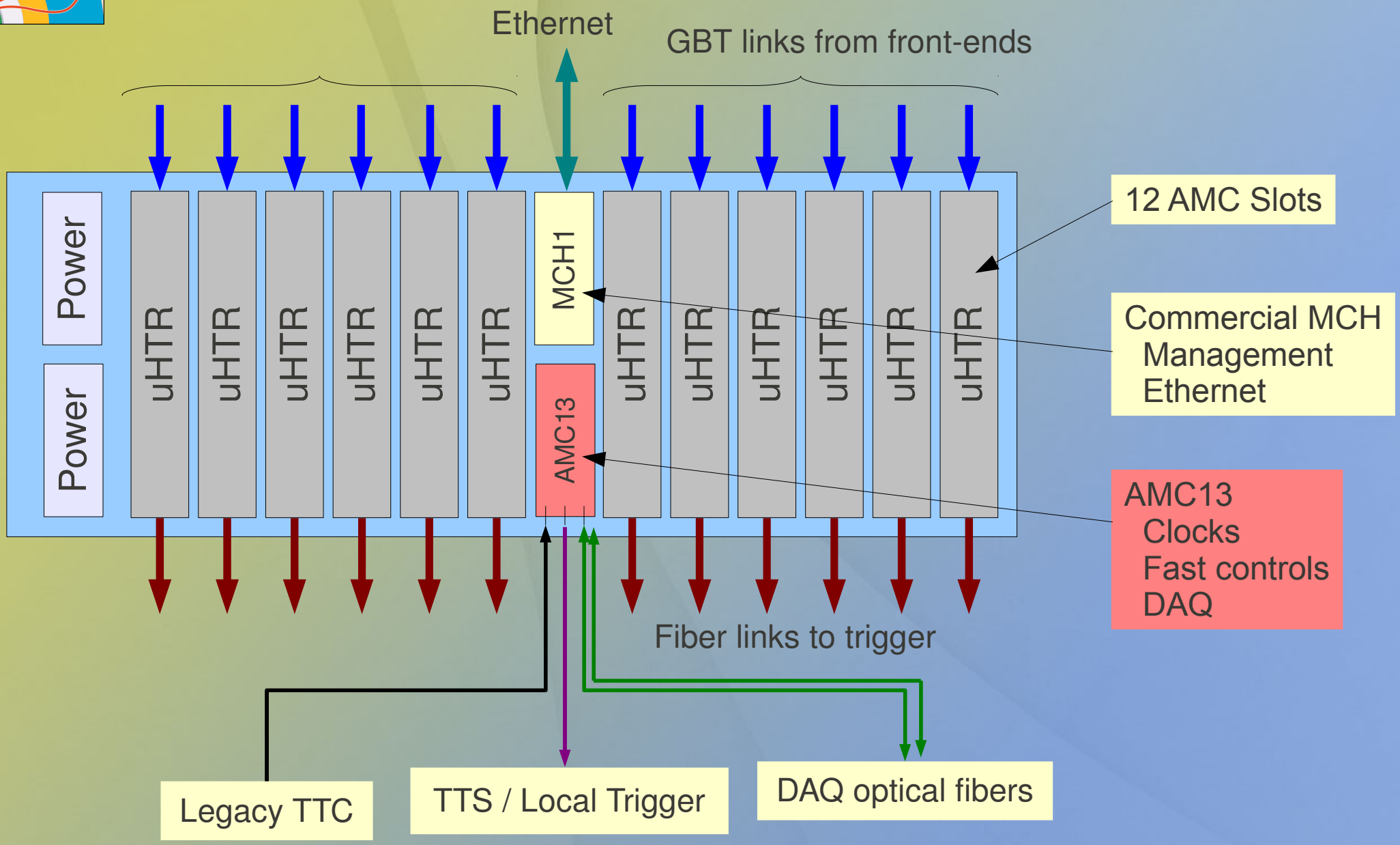
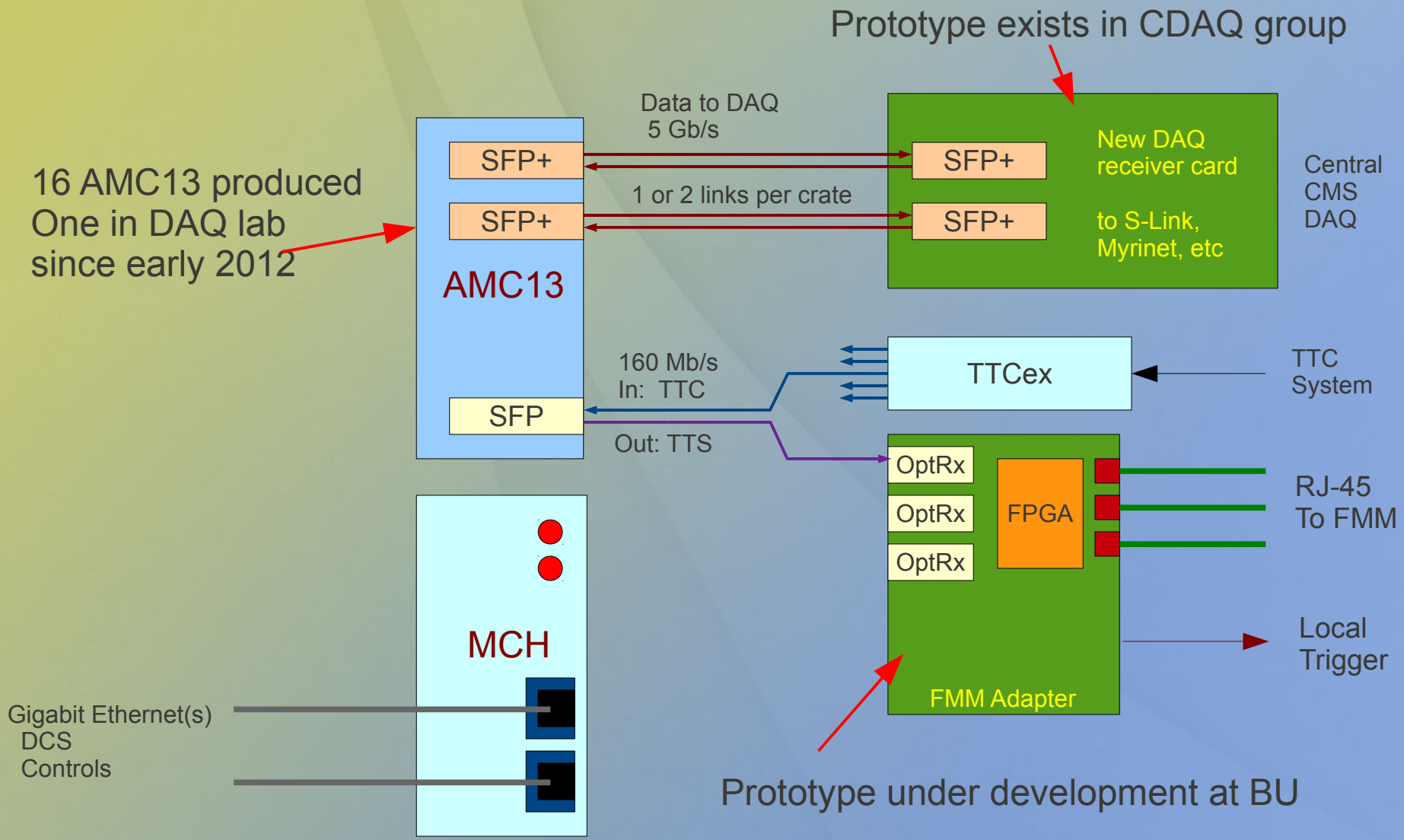
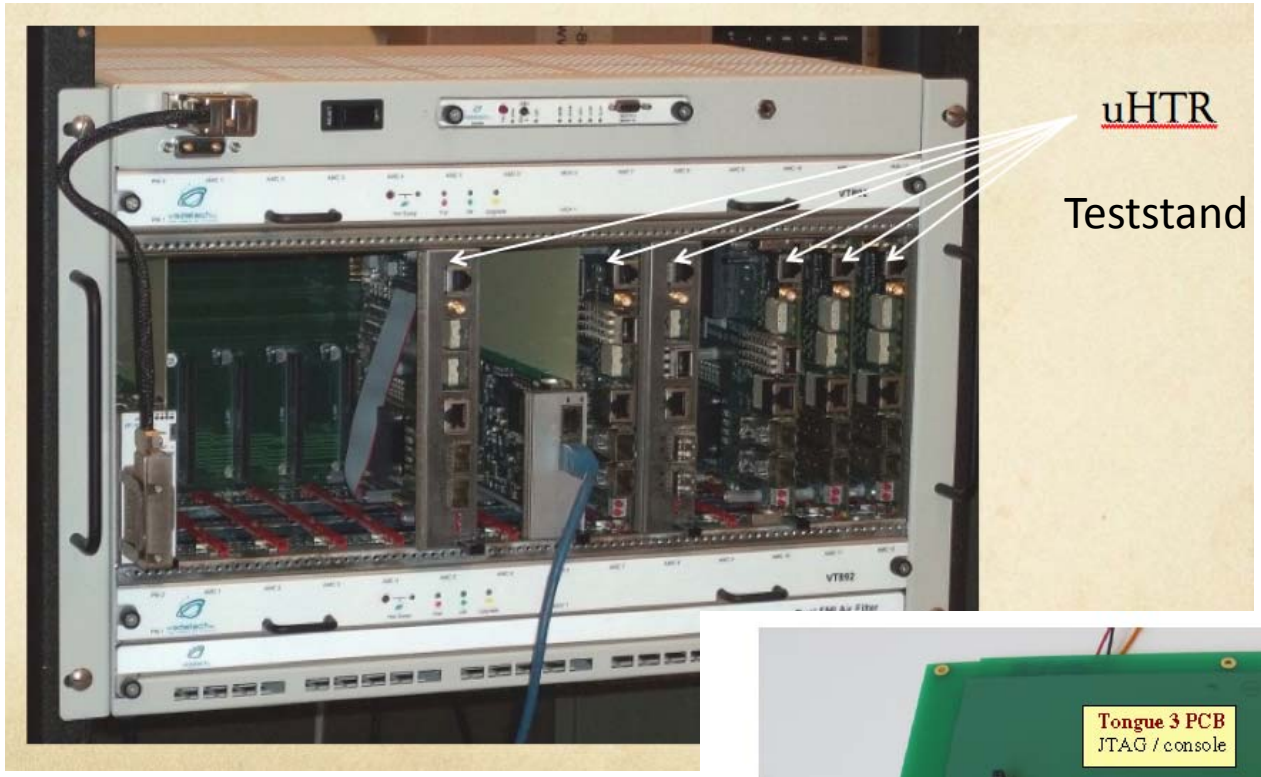
HCAL uTCA Readout Crate



MicroTCA Interface to CMS
(Interim)





Teststand at University of Minnesota

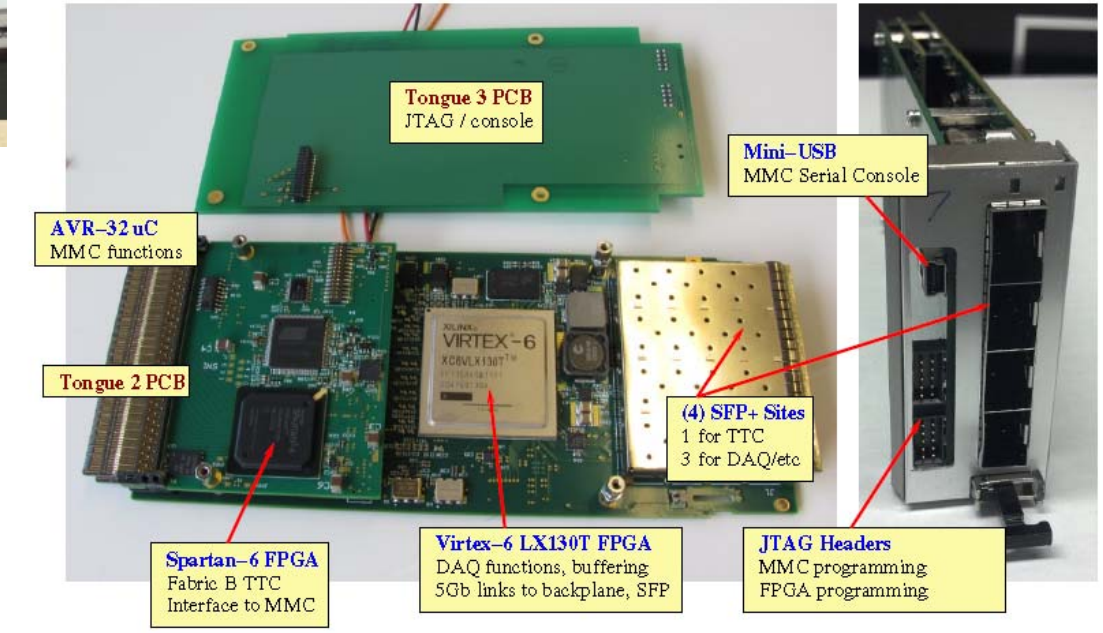


Figure 6.7: AMC13 Photograph

The baseline option to implement the FE control is shown in Fig. 6.10.

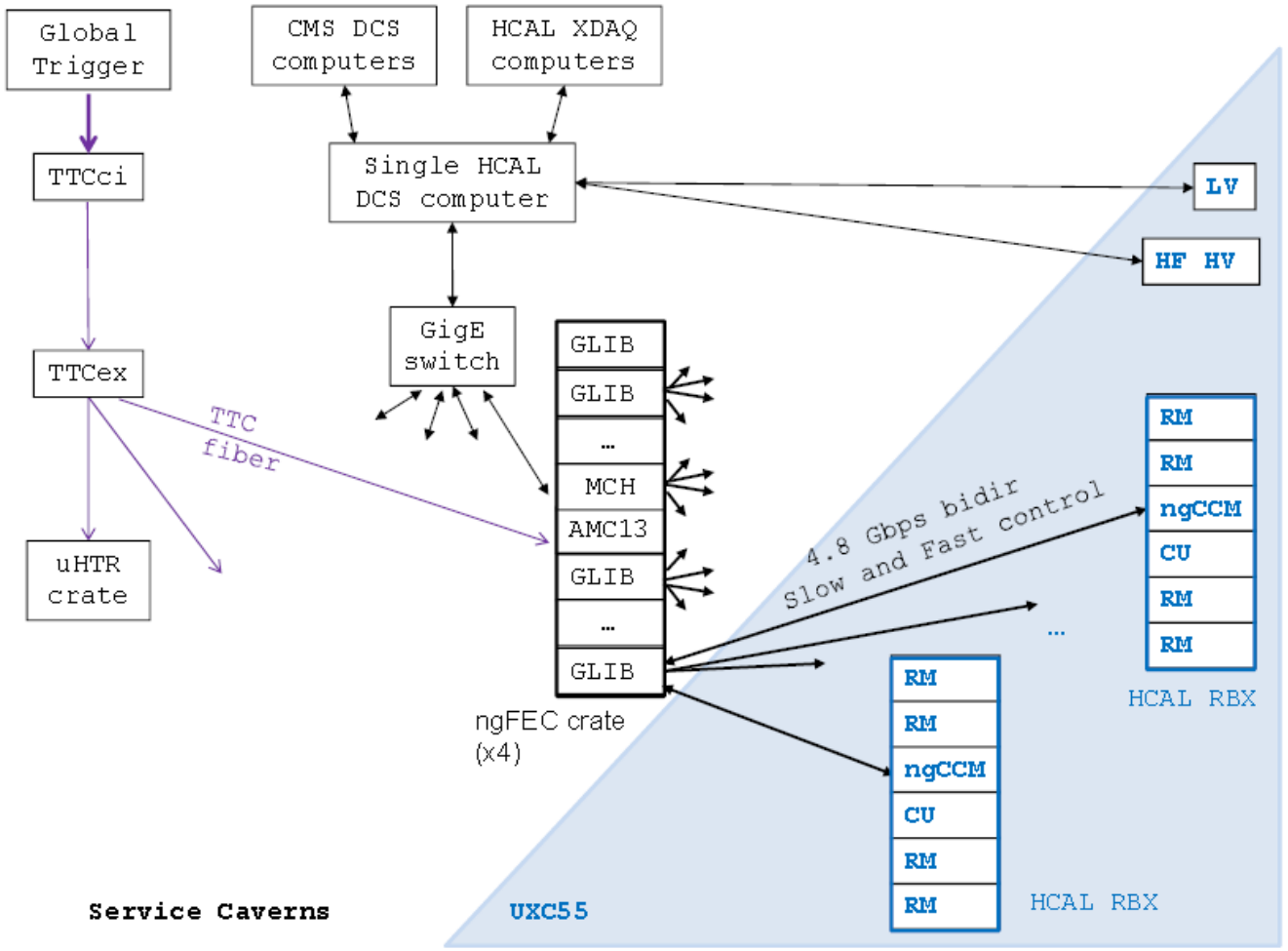
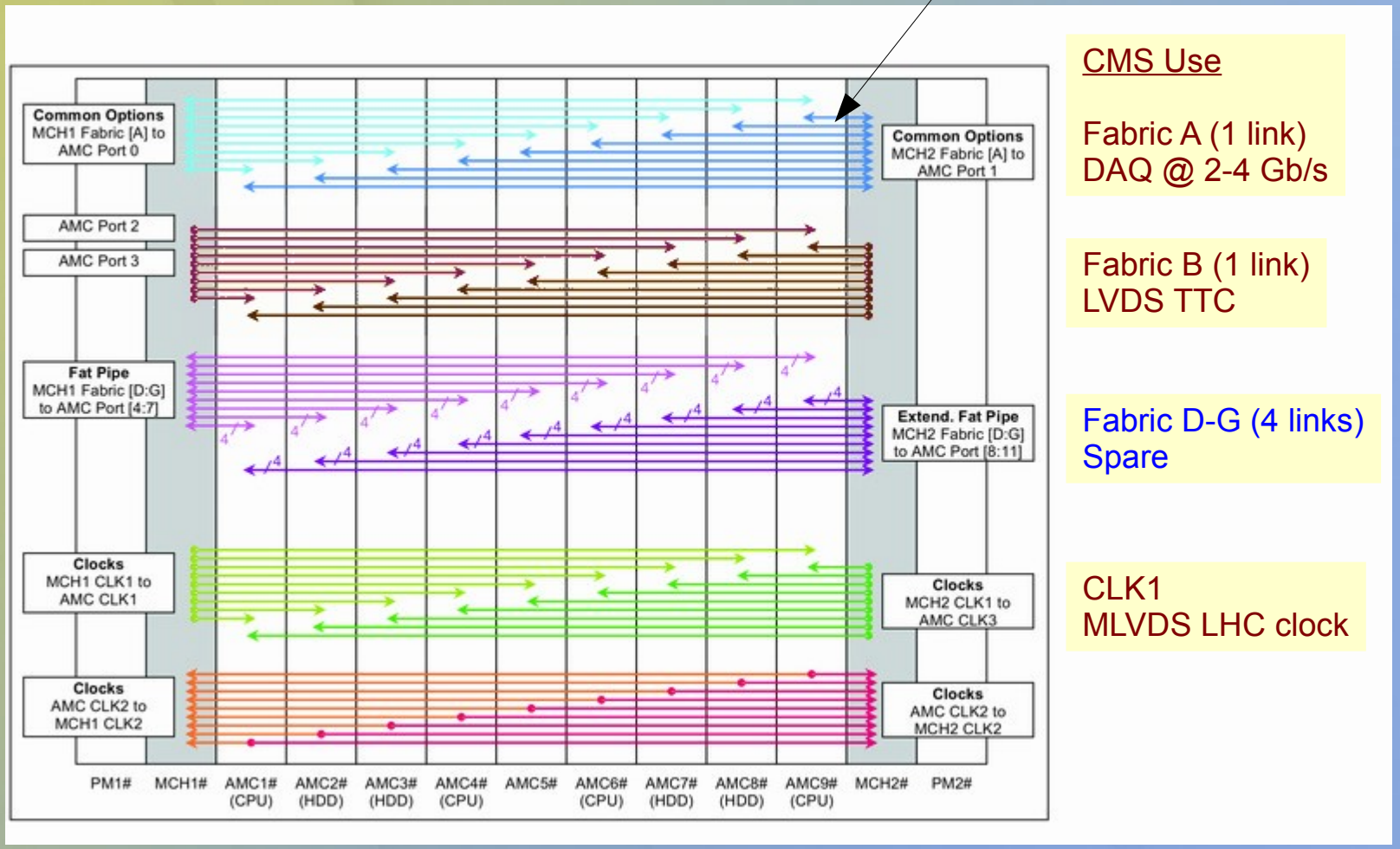


Figure 6.10: Block diagram of the baseline option for the HCAL control

µTCA Dual-Star Backplane

Note: Interconnections can be customized by the backplane manufacturer inexpensively.

Bi-directional serial (up to 10Gb/sec) point-to-point links from each AMC to MCH (redundant links to each MCH)



Fabric A (1 link)
Gigabit Ethernet

Fabric B (1 link)
Spare

Fabric D-G
Spare

CLK1
Spare

CMS Use

Fabric A (1 link)
DAQ @ 2-4 Gb/s

Fabric B (1 link)
LVDS TTC

Fabric D-G (4 links)
Spare

CLK1
MLVDS LHC clock

MCH 1
Commercial /Std

MCH 2 aka “AMC13”
Custom design for CMS

HCAL Development Requirements

- Expect to setup a uTCA at Fermilab which will handle both data and control functions
- It will serve as a working testbench for FE Modules and the readout system
  - Characterize our analog ASICs - QIE10s (Charge Integration Encoder)
    - DC charge calibration -> slope, offset
  - Read/Write to local registers
  - Exercise L1 and L2 buffers
  - Exercise optical links