‡ Fermilab

MicroTCA Application: Real Time Event Building and FIONA

Ryan Rivera Detector Instrumentation Group – Computing Sector October 17, 2012

This Talk

- 1. Completed Work
 - CAPTAN mTCA
- 2. Current Work
 - FIONA
- 3. Future Work
 - CMS Upgrades?
- 4. xTCA Impressions

First DIG xTCA Project

- Goals:
 - Gain experience designing boards in the xTCA form factor.
 - Strive to meet complete mTCA specification.
 - Minimize points of failure.

CAPTAN AMC



Why CAPTAN

- CAPTAN <u>compact</u> And <u>Programmable</u> da<u>T</u>a <u>A</u>cquisition <u>N</u>ode
 - Simple, flexible, scalable data acquisition solution developed by DIG. The user can stack the foundation boards in different combinations to give unique functionality.
 - We had FPGA boards on hand.
 - Reuse of CAPTAN allows the AMC to be simple and avoid errors.

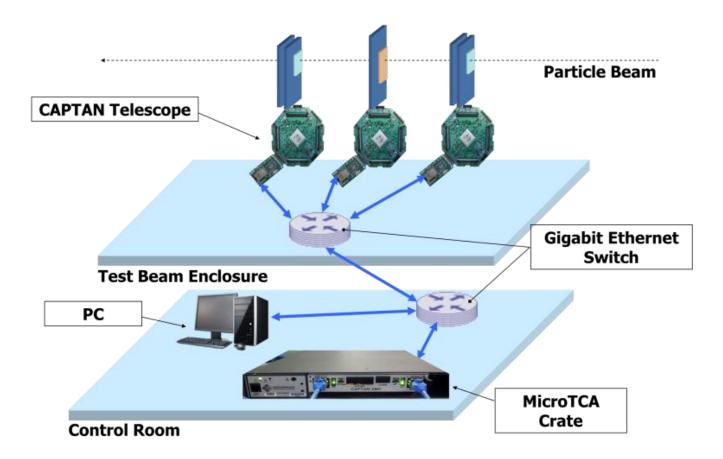


CAPTAN AMC Features

- Passive AMC
- MMC from pluggable Olimex LPC-H2148
 - NXP ARM 7, 60 MHz, 42 KB RAM
- Logic and memory from pluggable CAPTAN
 - Xilinx Virtex-4
 - 162 KB RAM
 - 400 MHz fabric
 - 2 x Full-Duplex GbE

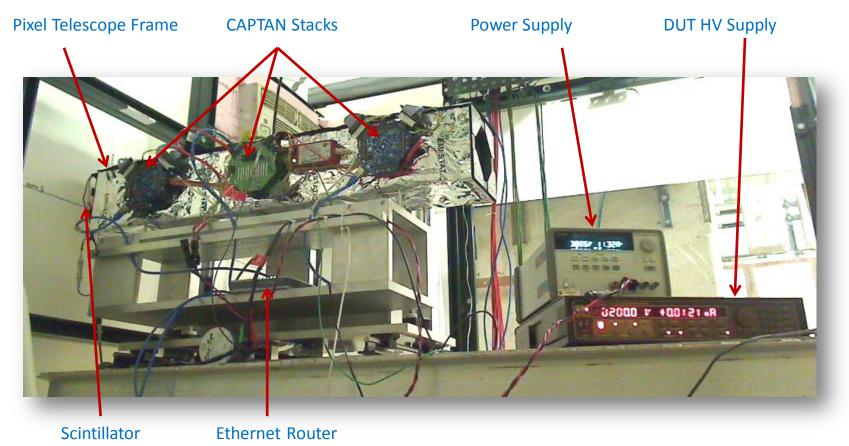


Test Beam Application: Real-Time Event Assembly



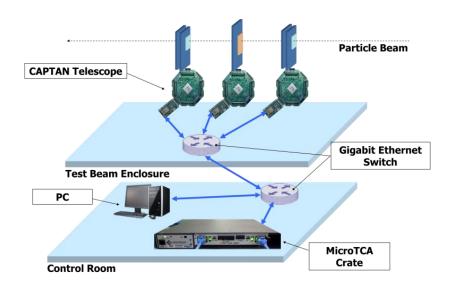
FTBF Pixel Telescope

The CAPTAN pixel telescope is 8 silicon pixel planes leftover from CMS, with space for 2 DUTs in the middle. Pixel size is 100 μ m x 150 μ m. Projected track resolution on DUT is 6-10 μ m. Data acquisition with the CAPTAN system.



Test Beam Outcome

 Successful integration of real-time event assembly, in mTCA form factor, into the T-992 pixel telescope DAQ.



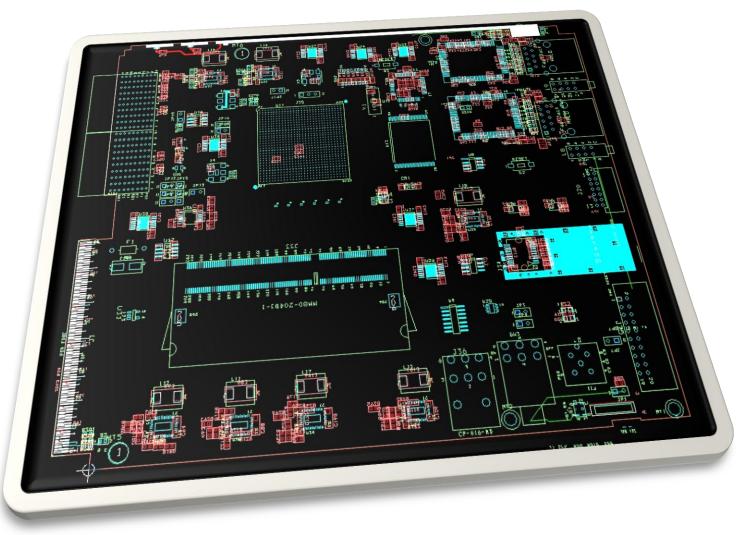
Current Work

- FIONA <u>Fast Input</u>/<u>Output</u> Metworked <u>A</u>MC
- Goals:
 - mTCA.4 RTM experience
 - High speed (~10 Gbps) FPGA TX/RX
 - Explore mTCA.4 backplane and connector speed capabilities
 - Add real-time track generation to event assembly solution

FIONA

- FPGA: Kintex 7
 - 2,000 KB RAM, ~800 MHz fabric, 16 GTX transceivers
- Memory: DDR3 SODIMM
 - 2 GB RAM @ ~1.3 GHz
- μRTM rear transition module
 - 1 SFP+ and 10 TX/RX channels on MiniPods
- AMC front panel
 - 1 SFP+ and 2 x GbE (use GbE for FPGA config)
- Backplane
 - 10GbE Fat Pipes and GbE to MCH crate position

FIONA

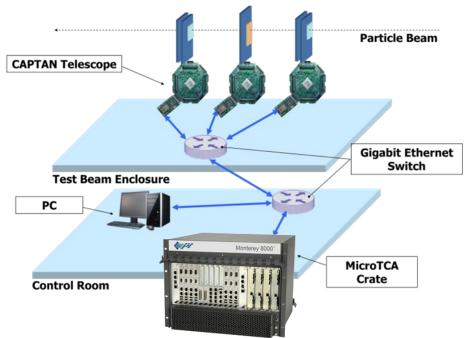


mTCA.4 Crate



FIONA Future Work

• We plan to use 1-3 FIONAs in the mTCA.4 carrier to conduct real-time tracking in a test beam environment.



xTCA Future Work

- Large experiments need DAQ carriers and are considering xTCA over VME.
 - CMS
 - ATLAS
 - LHCb
 - Experiments at DESY
- We want to develop a mTCA-based readout system for a new strips/pixels telescope and leverage the experience to position ourselves for future DAQ opportunities.

xTCA Impressions

 xTCA is a convenient architecture for powering and cooling boards

- Crates are available, affordable, and scalable

- mTCA backplane has limited utility
 - Few channels between boards
- The full specification is extensive
 - Shelf manager interfacing is involved