



# Micro/Nano Fabrication of Superconducting Quantum Devices

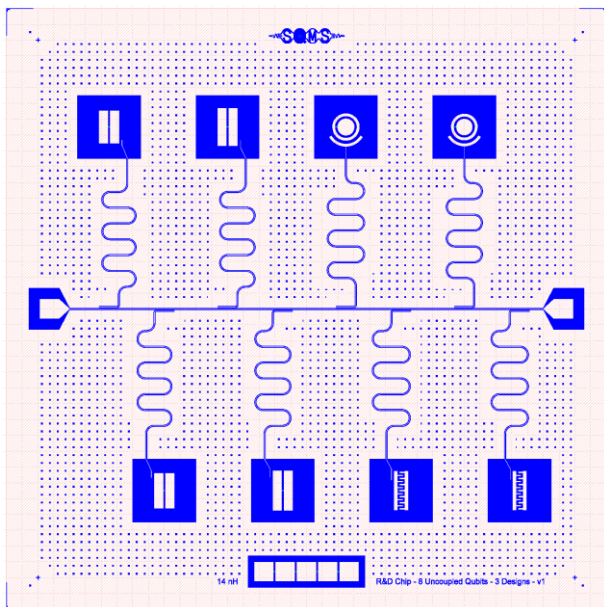
Mustafa Bal

Associate Scientist, SQMS Qubit Fabrication Group Leader, Fermilab

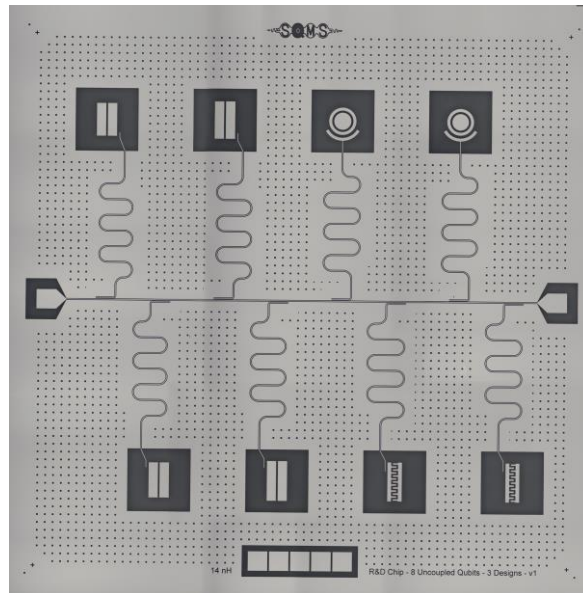
8/14/2023

USQIS Summer School 2023




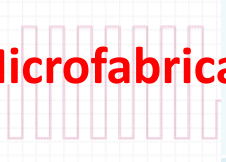





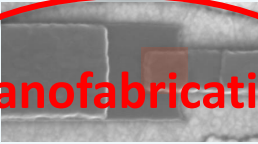
# Design to Device



Micro/Nano  
Fabrication

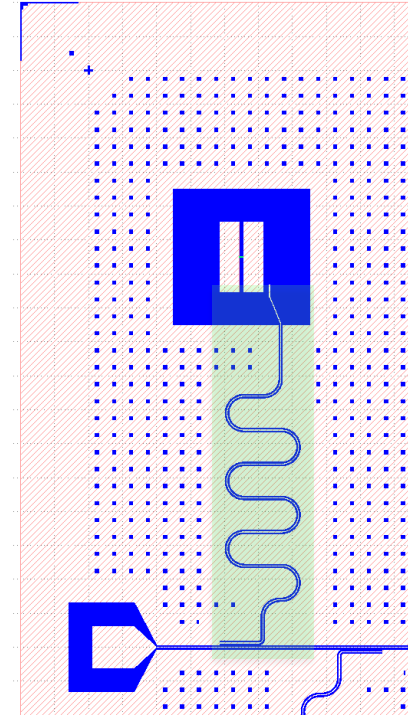


# Basic components in the design

Name	Symbol	Equivalent rep.	Top view
Capacitor			
Inductor			 <p><b>Microfabrication</b></p>
Transmission line (CPW)			 <p>gnd gnd</p>
Josephson Junction			 <p><b>Nanofabrication</b></p>

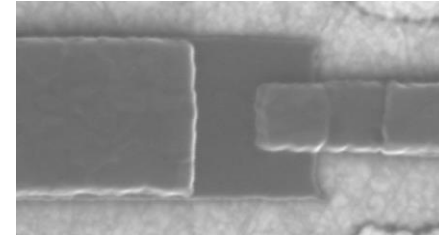
# 1st key component of superconducting circuits - resonators

- Typically meander CPWs,  $l = \lambda/4$  (or  $\lambda/2$ );  $f_r = \frac{v}{l} \sim 6 - 7 \text{ GHz}$  coupled to feedline
  - Loss/cycle,  $\tan \delta \sim 10^{-6} - 10^{-8}$
  - Can define  $Q = f_r / \Delta f = 1 / \tan \delta$
  - long lifetime,  $\tau = Q / 2\pi f_r$
- Measure amplitude & phase of output probe tone
  - Useful as test structures to evaluate loss ( $\delta=1/Q$ )
  - Extensively used circuits as readouts & couplers for qubits
  - Equally space energy levels => difficult to use directly as qubits

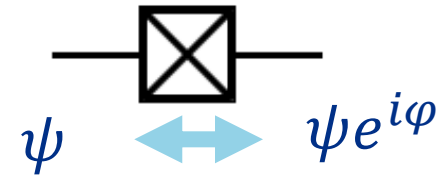


## 2nd key component – Josephson junction

- Wavefunction tunnels across barrier from top electrode to bottom electrode
- Ultra-thin amorphous-AIOX
  - small to reduce loss
  - Thermal oxidation, thickness  $d \sim 1.8$  nm:
    - tunneling current  $I \propto \exp(-d/\lambda)$
- $\varphi$  = phase across junction, Josephson relations



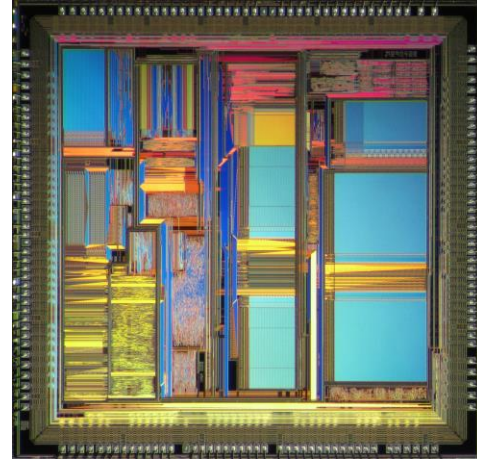
$$\bullet \left\{ \begin{array}{l} I = I_0 \sin(\varphi) \\ V = \frac{\Phi_0}{2\pi} \frac{d\varphi}{dt} \end{array} \right\}$$



$$I_0 = \frac{\pi}{2e} \frac{\Delta_{S.C.}}{R_n} \quad (\text{Ambegoaker – Baratoff Relation})$$

# Micro/Nano Fabrication of ICs

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- Tremendous progress has been achieved in integrated circuit fabrication.
- The same technology provides the basis for micro/nano fabrication of superconducting quantum chips

# Semiconductor IC Fabrication “Toolkit”

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- **Insulating Layers**

- Oxidation, nitridation
- Deposition (LPCVD, PECVD, APCVD)

- **Selective doping of silicon**

- Diffusion (in-situ doping)
- Ion implantation
- Epitaxy (in-situ doping)

- **Material deposition (silicon, metals, insulators)**

- LPCVD
- PECVD
- PVD

- **Patterning of Layers**

- Lithography (UV, deep UV, e-beam & x-ray)

- **Etching of (deposited) material**

- Dry etches—plasma, RIE, sputter etch, DRIE
- Wet etches—etch in liquids, CMP etc

LPCVD: low pressure chemical vapor deposition.

PECVD: plasma enhanced CVD.

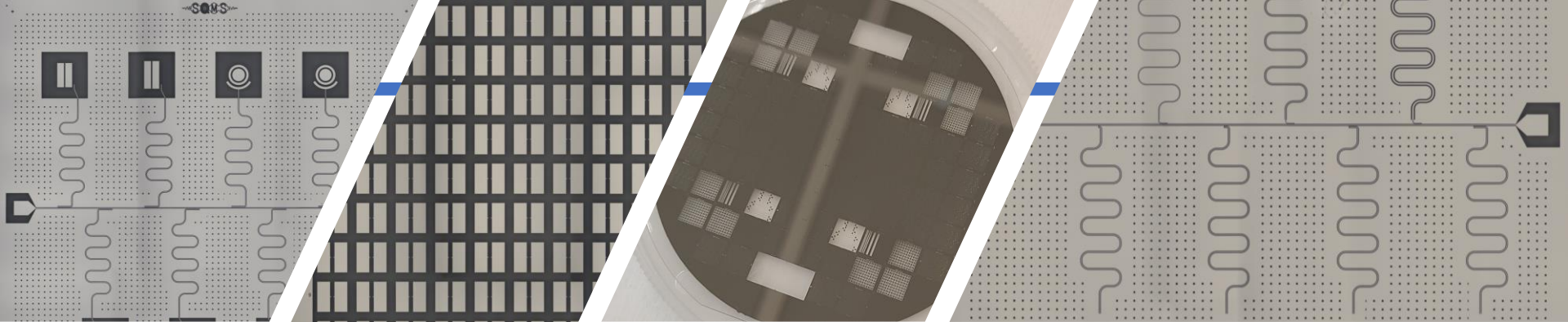
APCVD: atmospheric pressure CVD

RIE: reactive ion etching

DRIE: deep RIE.

CMP: chemical mechanical polishing

Lecture notes on micro/nano fabrication by Bo Cui, ECE, University of Waterloo; <http://ece.uwaterloo.ca/~bcui/>  
Textbook: Nanofabrication: principles, capabilities and limits, by Zheng Cui

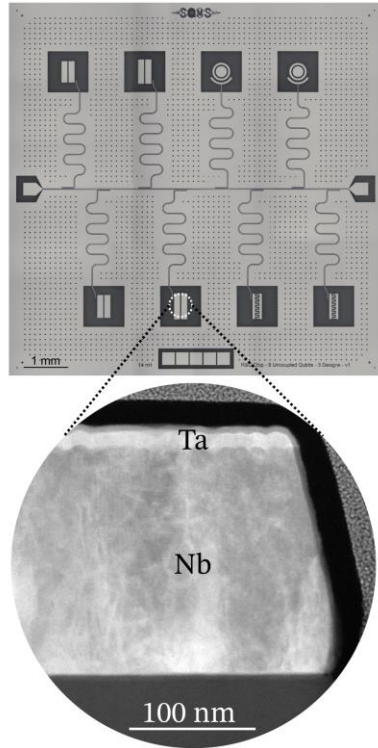


What processing is needed to turn a substrate into superconducting quantum devices?



# Basic Processing Steps

A sequence of additive and subtractive steps with lateral patterning.



Three components for micro/nano fabrication of superconducting quantum devices:

**Lithography (lateral patterning):** generate pattern in a material *called resist*  
photolithography, electron-beam lithography...

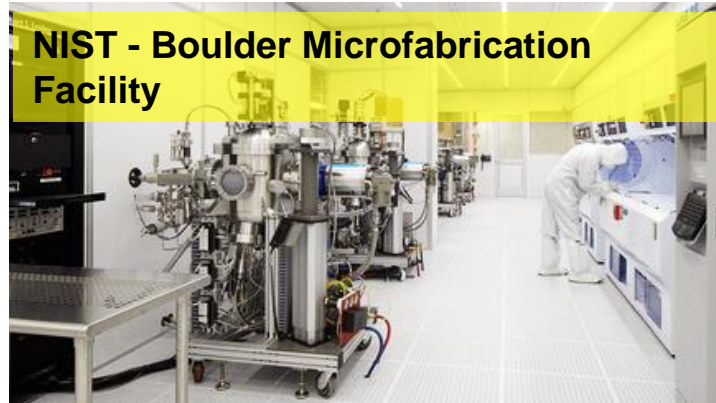
**Thin film deposition (additive):** spin coating, chemical vapor deposition, molecular beam epitaxy, sputtering, evaporation, electroplating...

**Etching (subtractive):** reactive ion etching, ion beam etching, wet chemical etching...

# Cleanroom

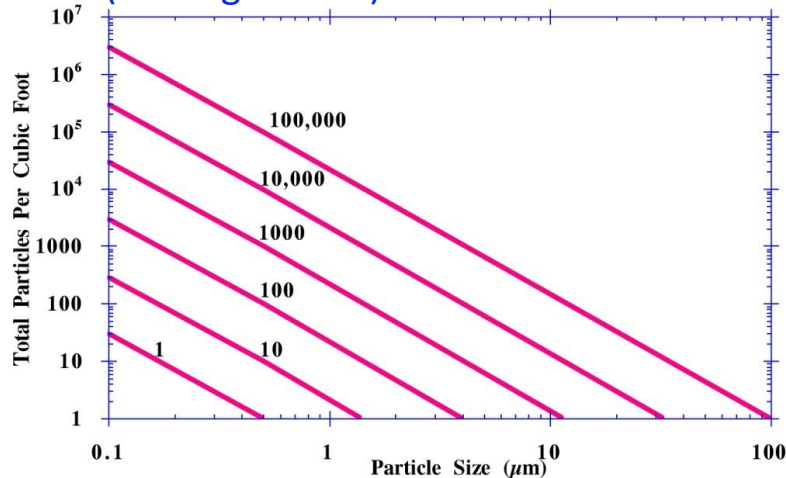
Cleanroom is cleaned by:

- HEPA filters and recirculation for the air.
- “Bunny suits” for workers.
- Filtration of chemicals and gases.
- Manufacturing protocols.



# Class of a Cleanroom

- Air quality is measured by the “class” of the facility.
- Class 1-100,000 mean number of particles, greater than  $0.5\mu\text{m}$ , in a cubic foot of air.
- A typical office building is about class 100,000.
- The particle size that is of most concern is  $10\text{nm} - 10\mu\text{m}$ . Particles  $<10\text{nm}$  tend to coagulate into large ones; those  $>10\mu\text{m}$  are heavy and precipitate quickly.
- Particles deposit on surfaces by Brownian motion (most important for those  $<0.5\mu\text{m}$ ) and gravitational sedimentation (for larger ones).



Particle diameter ( $\mu\text{m}$ )

Class	0.1	0.3	0.5	5.0
1	35	3	1	
10	350	30	10	
100		300	100	
1000			1000	7
10000			10000	70
100000			100000	700

# Cleanroom Processing

Deposition  
Tools

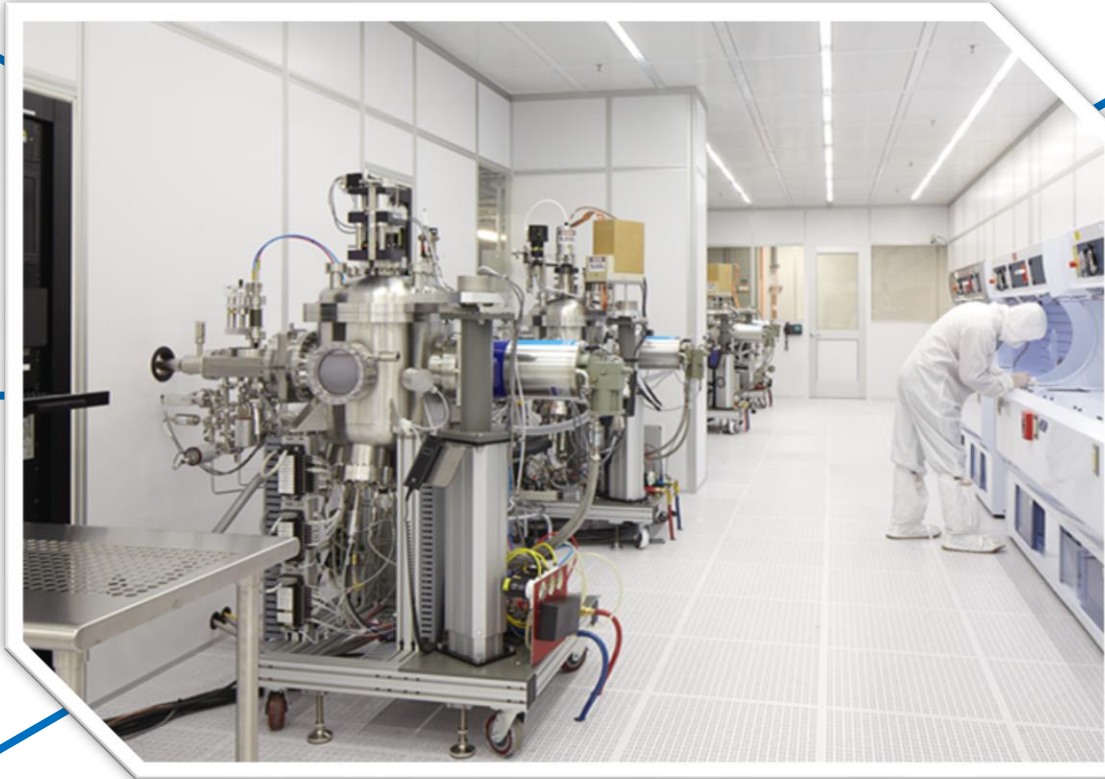
Wet Processing Benches

Etching Tools

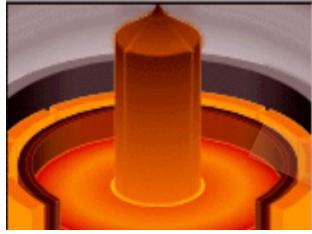
Imaging &  
Characterization  
Tools

Lithography Tools

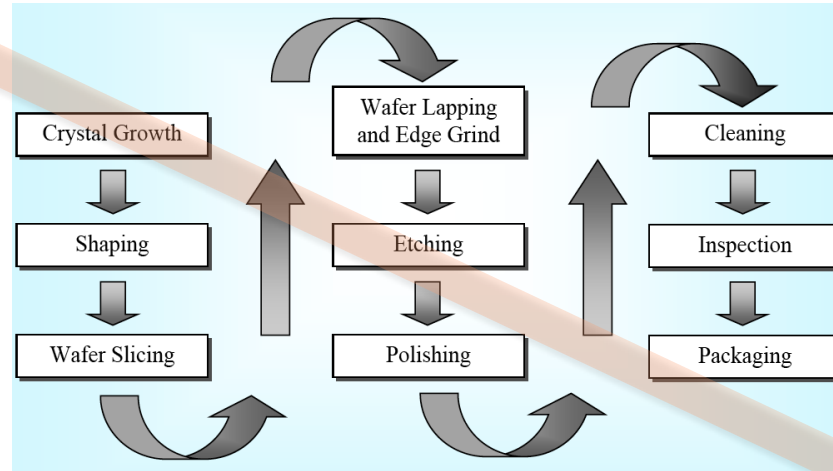
Post-processing &  
Packaging Tools



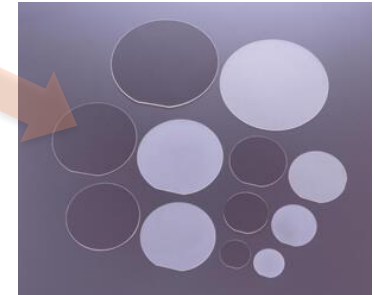
# Substrates: Si, Sapphire,...



CZ growth

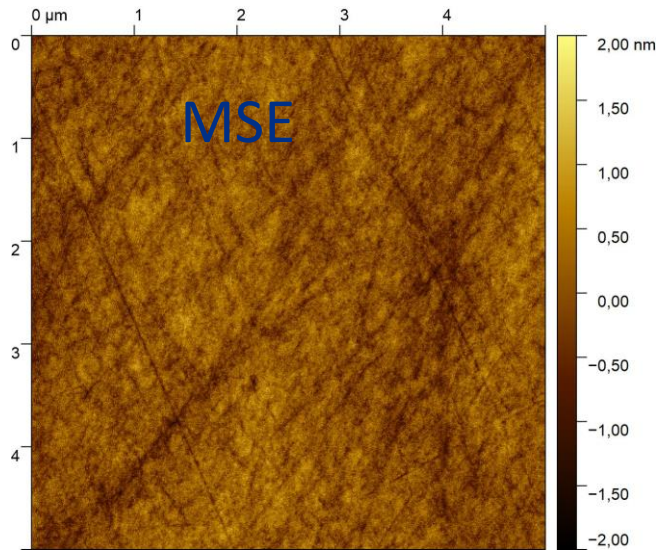


Single crystal wafers

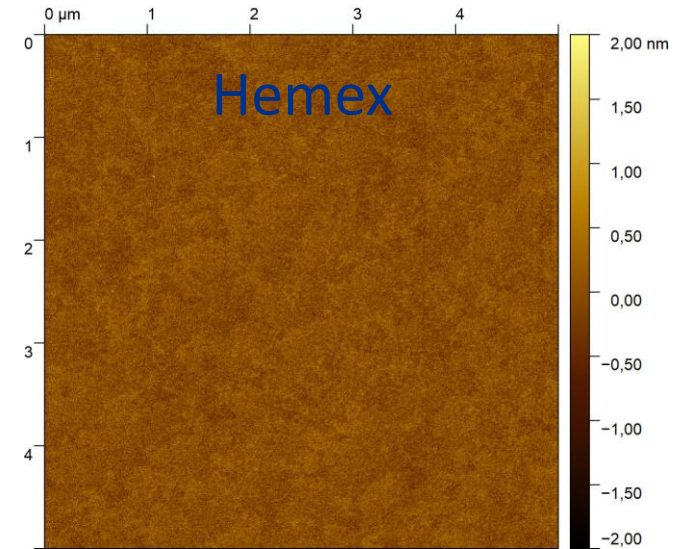


# Surface of Hemex and MSE Sapphire Substrates as received

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RMS Roughness = 0.35 nm  
Scratched surface (as much as  
~ 1nm deep)



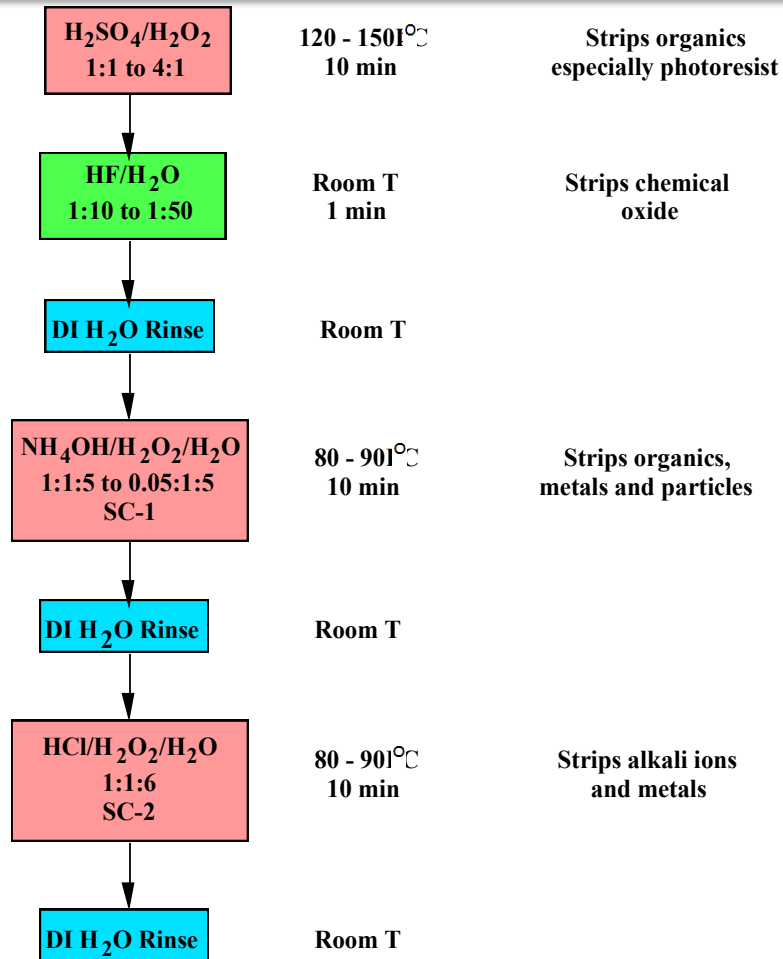
RMS Roughness = 0.21 nm  
Smooth overall

# Substrate Surface Treatment/Cleaning

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- Treatment/cleaning involves removing particles, organics, oxides, and metals from substrate surfaces.
- Particles are largely removed by ultrasonic agitation during cleaning.
- Organics (photoresist) are removed in  $O_2$  plasma or in  $H_2SO_4/H_2O_2$  (Piranha) solutions.
- The “RCA clean” is used to remove metals and any remaining organics.
- Oxides are removed by BOE, HF, or BHF solutions

# Standard RCA Cleaning Procedure for Si Substrates





# Sapphire Surface Treatment

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## RCA SC-1:

$\text{NH}_4\text{OH}(30\%):\text{H}_2\text{O}_2(30%):\text{H}_2\text{O}=1:1:5$ ; 70-80°C, 5 min, high pH.

- Oxidize organic contamination (form  $\text{CO}_2$ ,  $\text{H}_2\text{O}$ ...)
- Slowly dissolve native oxide and grow back new oxide, which removes particles on oxide.
- But  $\text{NH}_4\text{OH}$  etches Si and make the surface rough, thus less  $\text{NH}_4\text{OH}$  is used today.

## Piranha:

$\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2(30\%)=3:1$ ; 50°C; 5 min, low pH.

- Strong oxidizer, removes organics.
- Could be replaced by Nanostrip.

## Other Cleaning Methods:

Energy may come from plasma, ion beam, short-wavelength (UV) radiation or heating.

- $\text{HF}/\text{H}_2\text{O}$  vapor cleaning
- UV-ozone cleaning (UVOC)
- $\text{H}_2/\text{Ar}$  plasma cleaning
- Thermal Annealing

# Thin Film Deposition: Key Parameters & Modes of Deposition

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- Deposition rate, Film uniformity (across wafer & run-to-run), Film density, Defect density, Film texture, Grain size, Film conformality, Impurities
  - Electrical properties of film: resistivity, dielectric characteristics...
  - Mechanical properties: residual stress, adhesion...
  - Optical properties: transparency, refractive index...
- 
- Physical vapor deposition (PVD): sputtering, e-beam or thermal evaporation
  - Chemical vapor deposition (CVD): metal-organic CVD, plasma-enhanced CVD, low pressure CVD...
  - Epitaxy: molecular beam epitaxy (MBE), liquid-phase epitaxy...
  - Electrochemical deposition: electro- and electroless plating (of metals)
  - Oxidation (growth of thermal SiO<sub>2</sub>)
  - Spin-on and spray-on film coating (resist coating)

# Physical vapor deposition (PVD): evaporation and sputtering

## Evaporation:

- Material source is heated to sublimation temperature in vacuum either by thermal or e-beam methods.
- Material is vapor transported to target in vacuum.
- Easier to change evaporation material than sputtering target.

EVAPORATION	SPUTTERING
low energy atoms	higher energy atoms
high vacuum path <ul style="list-style-type: none"><li>• few collisions</li><li>• line of sight deposition</li><li>• little gas in film</li></ul>	low vacuum, plasma path <ul style="list-style-type: none"><li>• many collisions</li><li>• less line of sight deposition</li><li>• gas in film</li></ul>
larger grain size	smaller grain size
fewer grain orientations	many grain orientations
poorer adhesion	better adhesion

## Sputtering:

- Material is removed from target by momentum transfer.
- Gas molecules are ionized in a glow discharge (plasma), ions strike target and remove mainly neutral atoms.
- Sputtered atoms condense on the substrate.
- Not in vacuum, gas (Ar) pressure 5-50mTorr.

Plassys MEB550S

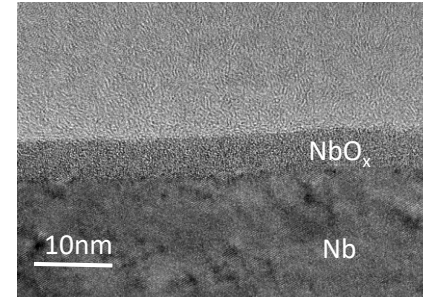


AJA ATC 2200 UHV Sputtering System

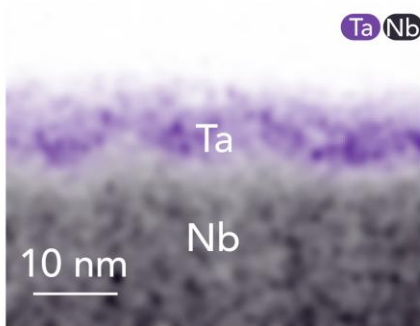


# Novel Surface Encapsulation as Mitigation Strategy to eliminate $\text{Nb}_2\text{O}_5$

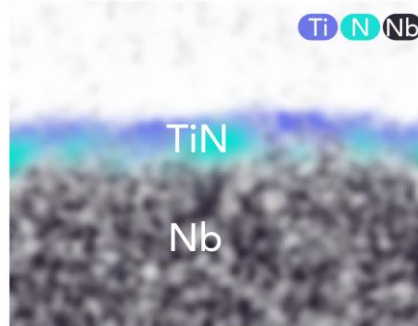
- Nb is frequently used in S.C. quantum devices. It has a surface oxide which is very lossy.
- Avoid niobium oxidation by stable surface **encapsulating layer**
  - Thin (~5-10 nm) => small contribution to conductive losses
  - But TLS-hosting dissipative surface  $\text{Nb}_2\text{O}_5$  is absent => reduction of the TLS dielectric losses => better coherence



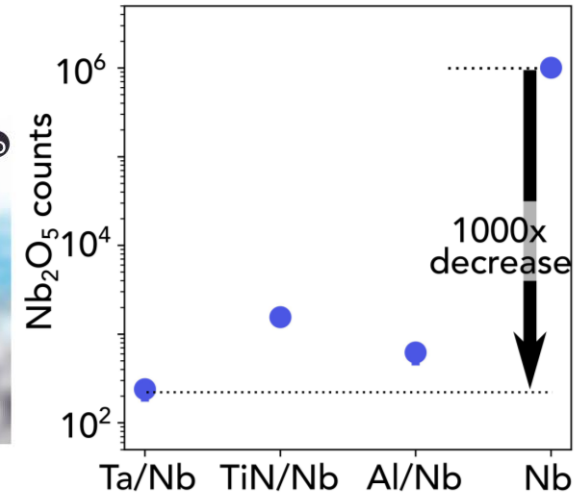
Ta Encapsulation



TiN Encapsulation



Al Encapsulation



M. Bal et al, arXiv:2304.13257

# Lithography – Patterning

## Lithography on surfaces

- Optical/UV lithography
- E-beam lithography
- FIB lithography
- X-ray lithography
- SPM-lithography
  - AFM
  - STM
  - DPN (dip-pen nanolithography)
- Imprint lithography
  - Soft lithography
  - Hot embossing
  - UV imprinting
- Stencil mask lithography

## Lithography in volume

- Two photon absorption
- Stereo-lithography

Heidelberg MLA 150  
Maskless aligner

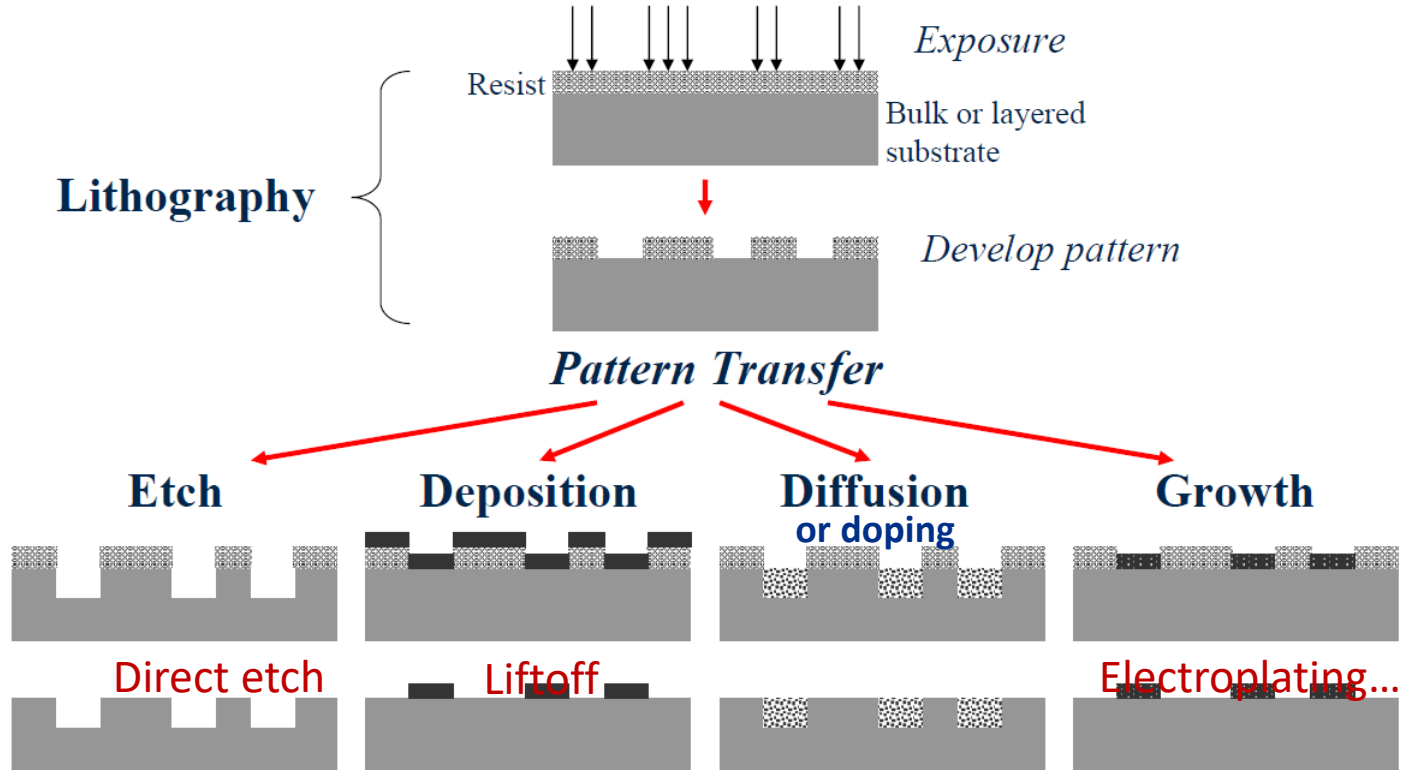


- Critical dimension (CD) control
  - Size of features must be controlled within wafer and wafer-to-wafer
- Overlay (alignment between different layers)
  - For high yield, alignment must be precisely controlled
- Defect control
  - Other than designed pattern, no additional patterns must be imaged



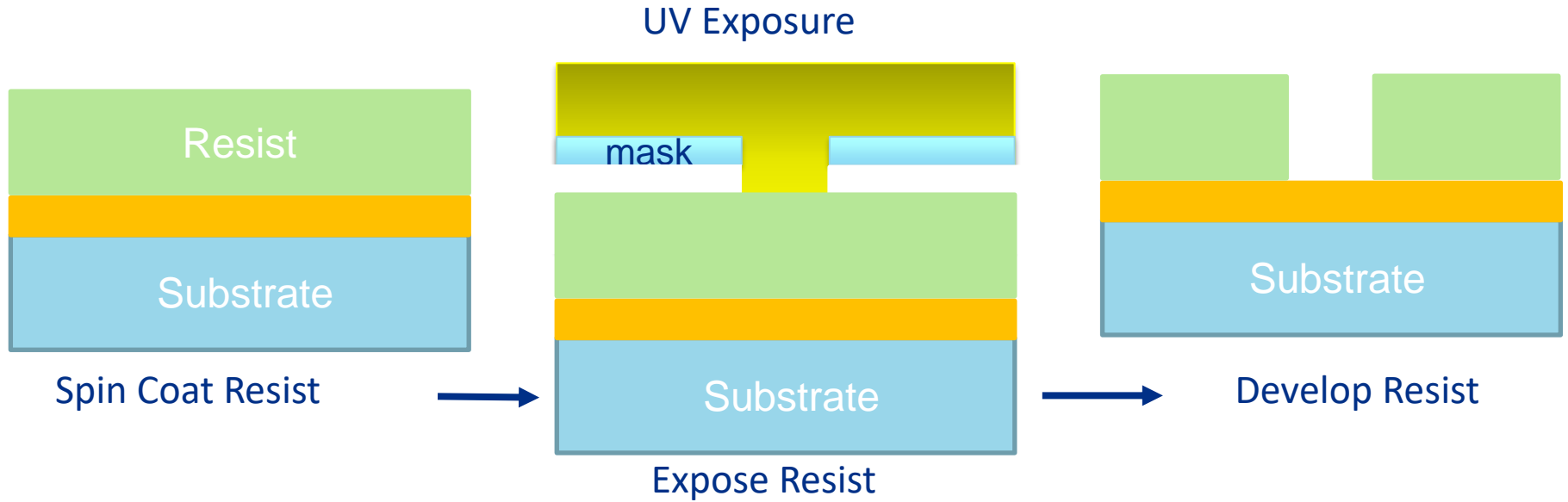
Raith EBP5200 E-Beam lithography system (100 kV)

# Pattern transfer (next step after lithography)



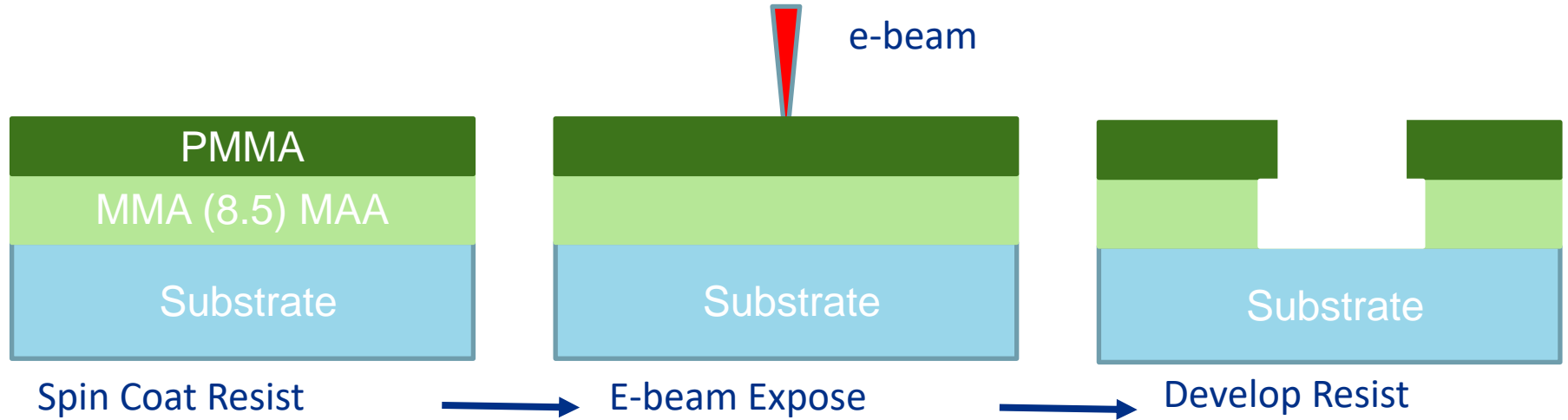
# Photolithography

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- Process used to transfer a pattern from a photomask to the surface of a substrate (Nowadays maskless aligners are widely available as an alternative)
- Formation of images with visible or ultraviolet radiation in a photoresist
- No limitation of substrate (Si, glass, metal, plastic...)
- For R&D, it is the most widely used lithography system, but with  $\sim 1\mu\text{m}$  feature size, so only for *micro*-fabrication.

# Electron Beam Lithography



- Electron beam has a wavelength so small that diffraction is insignificant.
- Tool is just like an SEM with on-off capability controlled by a “beam blanker”.
- Accurate positioning (alignment): “see” the substrate first, then expose.
- Beam spot diameter of 2nm can be achieved, at typical acceleration voltage of >20keV.
- Interaction of electrons and resist leads to beam spreading
- But typical resolution ~15nm (>> beam diameter), limited by proximity effect and lateral diffusion of secondary electrons.
- Direct write technique (no mask)



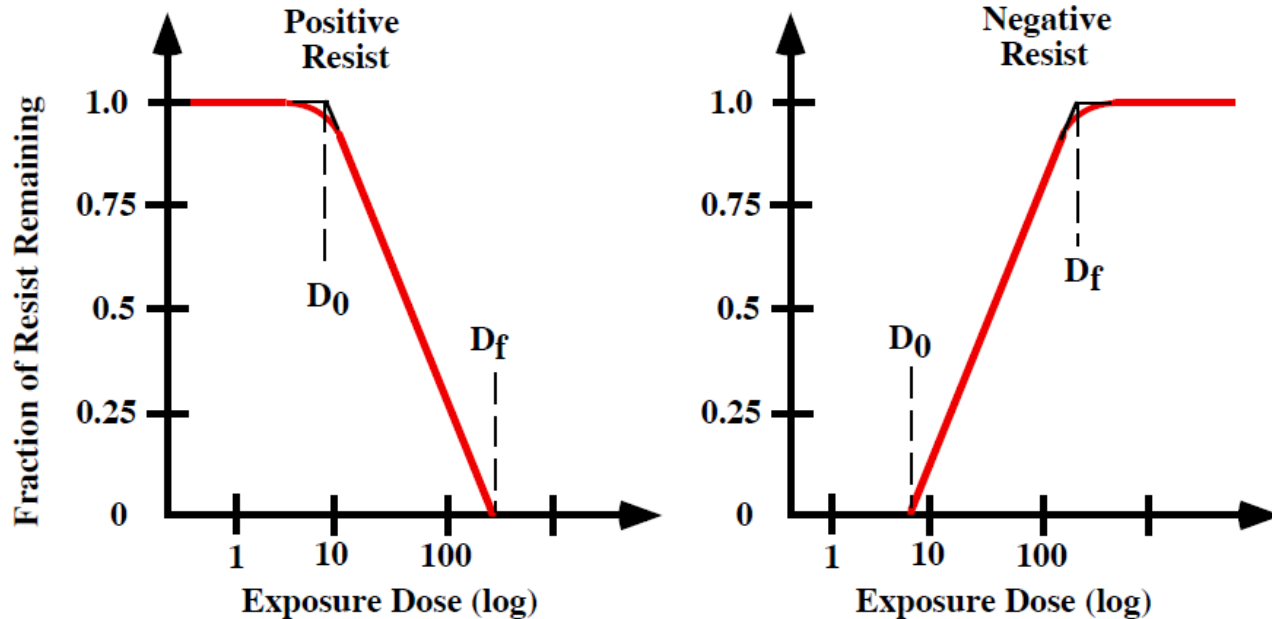
# Resist Contrast & Sensitivity

Contrast  $\gamma$  is defined as:

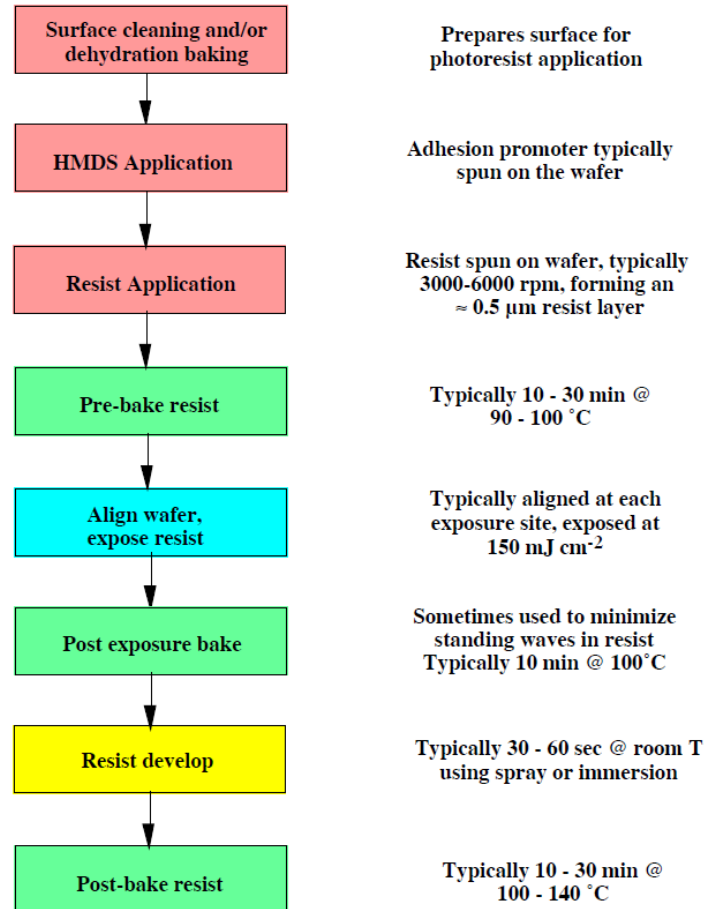
$$\gamma = \frac{1}{\log_{10} \frac{D_f}{D_0}}$$

- $\gamma$  and  $D_f$  are not intrinsic properties of the resist - they depend on process conditions (developer, development time, baking time,  $\lambda$ , substrate...).

$D_f$  is Sensitivity.



# Typical Process Flow for Photolithography



# Process Flow to Define Qubit Circuitry on Sapphire



## Substrate Preparation

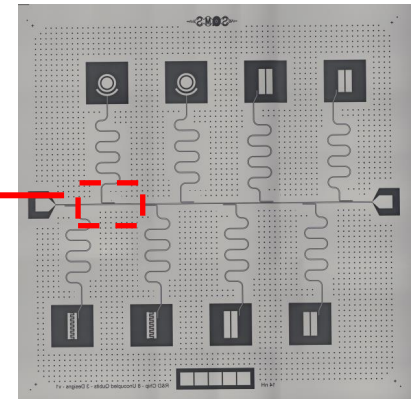
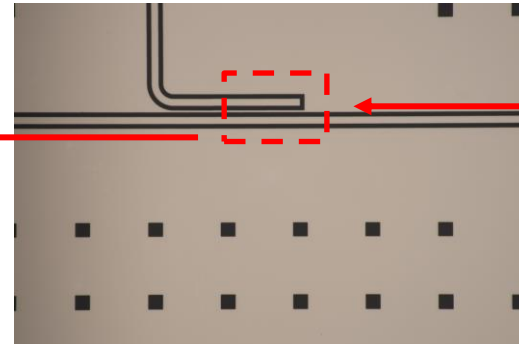
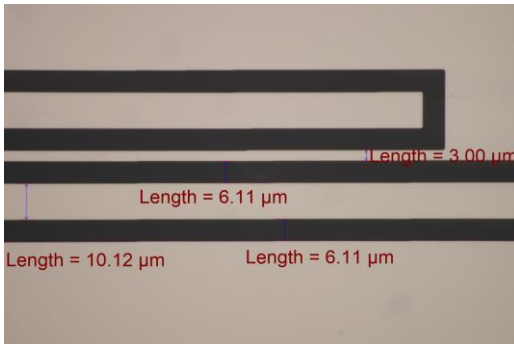
- Solvent Clean
- RCA SC-1 Clean

## Film Deposition

- Sputter Nb film
- Deposit 5-10 nm encapsulation layer
  - Ta & Al encapsulation in situ (sputter)
  - TiN encapsulation ex situ (ALD)

## Patterning Film

- Photolithography
- Dry Etch



# Subtractive Process: Etching

Etching is done either in “dry” or “wet” methods:

- Wet etching uses liquid etchants with wafers immersed in etchant solution.
- Wet etch is cheap and simple, but hard to control (not reproducible), not popular for *nanofabrication* for pattern transfer purpose.
- Dry etch uses gas phase etchants in plasma, both chemical and physical (sputtering process).
- Dry plasma etch works for many dielectric materials and some metals (Al, Ti, Cr, Ta, W...).
- For other metals, ion milling ( $Ar^+$ ) can be used, but with low etching selectivity. (as a result, for metals that cannot be dry-etched, it is better to pattern them using liftoff)

Etching is consisted of 3 processes:

- Mass transport of reactants (through a boundary layer) to the surface to be etched.
- Reaction between reactants and the film to be etched at the surface.
- Mass transport of reaction products from the surface through the surface boundary layer.

Figures of merit: etch rate, etch rate uniformity, selectivity, and anisotropy.



Plasma-Therm ICP RIE

# Advantages/Disadvantages of Dry Etching

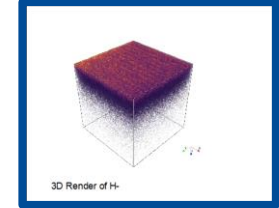
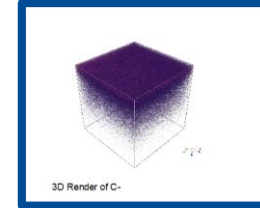
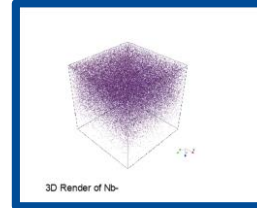
## Dry etching advantages

- Eliminates handling of dangerous acids and solvents
- Uses small amounts of chemicals
- Isotropic or anisotropic/vertical etch profiles
- Directional etching without using the crystal orientation of Si
- Faithful pattern transfer into underlying layers (little feature size loss)
- High resolution and cleanliness
- Less undercutting
- Better process control

## Dry etching disadvantages:

- Some gases are quite toxic and corrosive.
- Re-deposition of non-volatile compound on wafers.

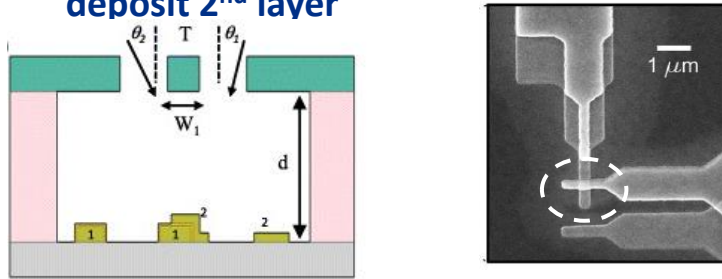
## FI-based Dry Etch Chemistry (Nb and Ta encapsulated Nb Films – 1<sup>st</sup> Round)



# Liftoff Process to Fabricate Submicron Al/AlO<sub>x</sub>/Al Junctions

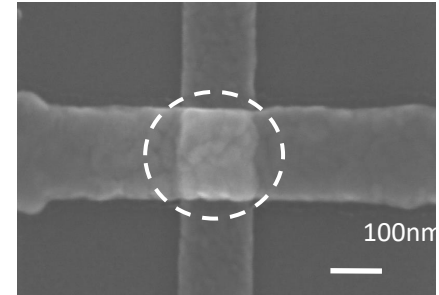
Shadow evaporation with tilt, “Dolan bridge” –  
Single pattern step, single pumpdown

- 1) Pattern, deposit 1<sup>st</sup> layer, oxidize, tilt,  
deposit 2<sup>nd</sup> layer



Overlap junction - 2 patterns, pumpdowns

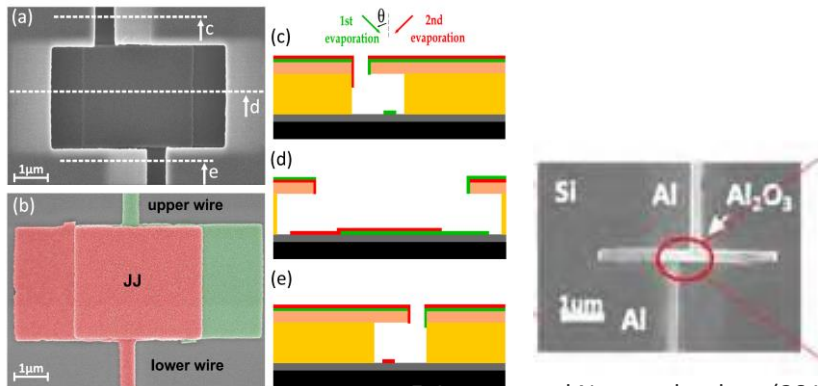
- 1) Pattern  
pumpdown  
LO BE
- 2) Pattern  
pump down  
mill BE & oxidize  
LO TE



X. Wu, et. al APL (2017)

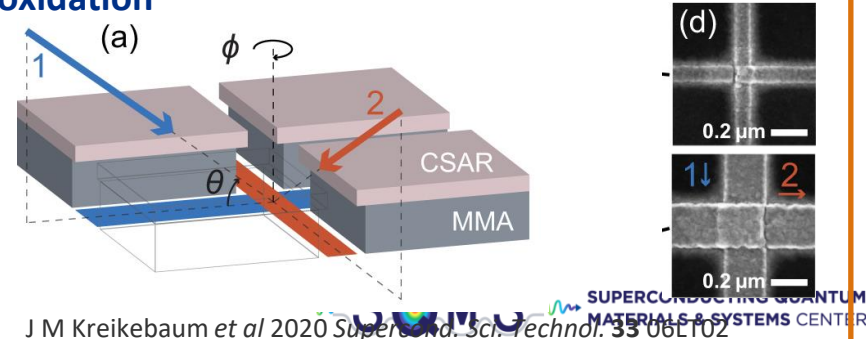
M. Steffen et. al, PRL97, 050502 (2006)

“Bridgeless” – shadow evaporation in high aspect tilt



F. Lecocq et al Nanotechnology (2011)

“Manhattan style” – shadow evaporation  
Use rotation between the two depositions and  
oxidation

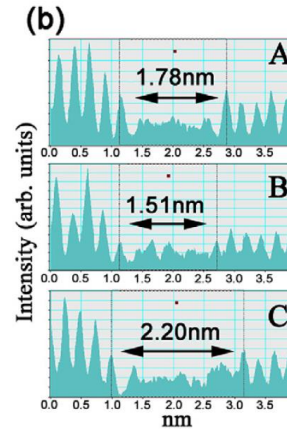
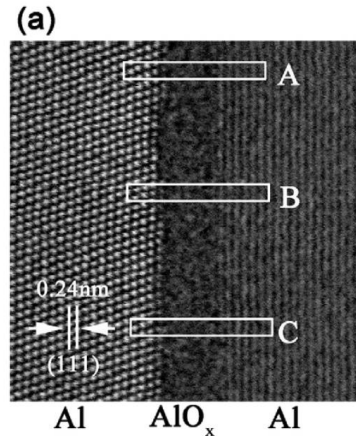
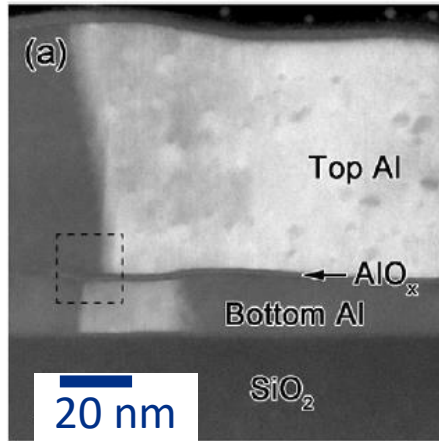


J M Kreikebaum et al 2020 Supercond. Sci. Technol. 33 06LT02

# Josephson junctions - sensitive to atomic-level defects

- Aluminum oxidation is conformal,  $\sim 1.8$  nm thick Al/AlO<sub>x</sub>/Al
- Thickness variations with exponential dependence of current
  - Less than 10% of total barrier active
  - Strong inhomogeneity of tunnel current across junction
- Amorphous materials are lossy – make junctions small

Cross-section TEM



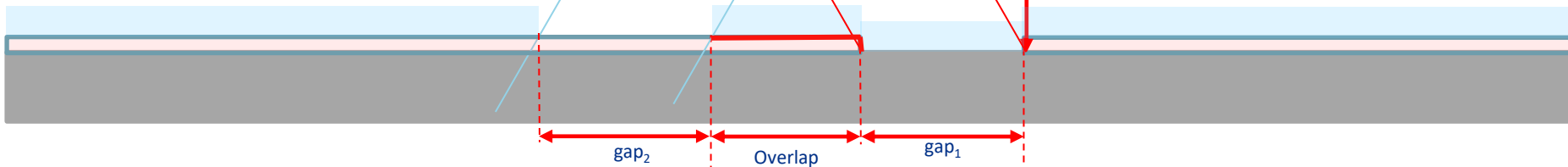
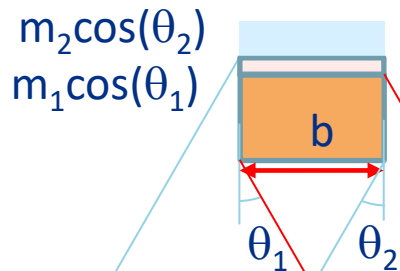
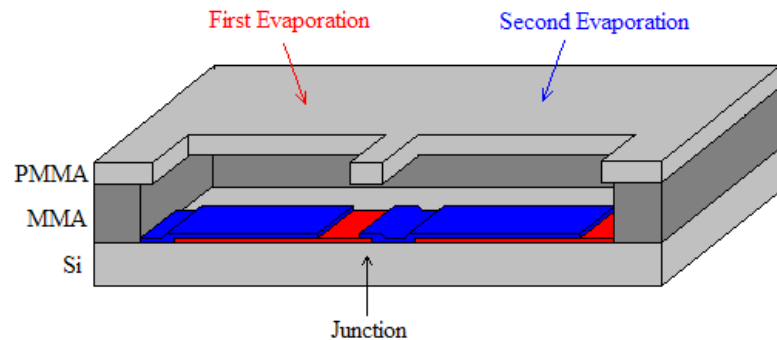
Zeng, J. Phys. D: Appl. Phys. **48** (2015) 395308

# Dolan Bridge Double Angle Shadow Evaporation



Raith EBP5200 E-Beam lithography system (100 kV)

- t1: thickness of 1<sup>st</sup> resist layer
- t2: thickness of 2<sup>nd</sup> resist layer
- m1: 1<sup>st</sup> metal deposition thickness
- m2: 2<sup>nd</sup> metal deposition thickness
- $\theta_1$ : 1<sup>st</sup> deposition angle
- $\theta_2$ : 2<sup>nd</sup> deposition angle
- b: bridge width

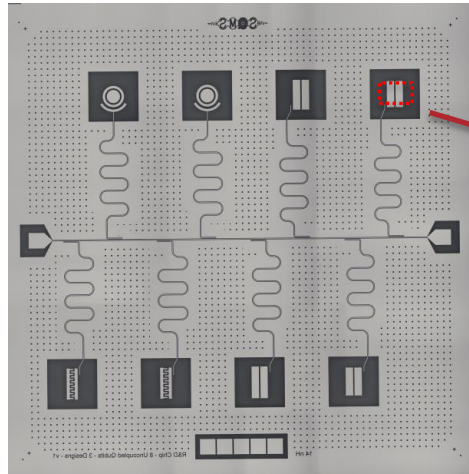




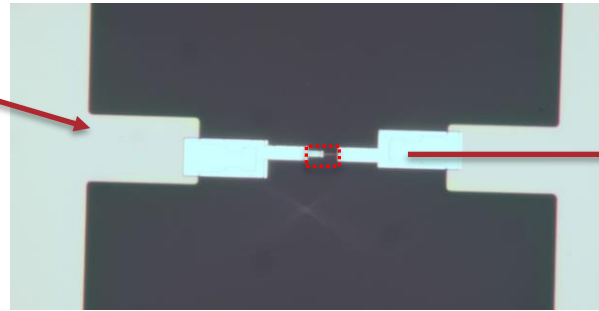
# Josephson Junction Deposition at FNAL

- Al/AIOx/Al Junctions are deposited at +22 / -22 degree angles relative to the normal of the substrate.
- 2'15" (45"/45"/45" at +60/0/-60 degree) Ar ion milling to remove oxide on Nb.
- Bottom/Top electrode thicknesses are 40 nm/90 nm.
- The Oxidation is 20 mBar for 12 minutes (Ar/O2 (85/15) mixture)
- Typical Junction area is approximately 200 nm x 200 nm

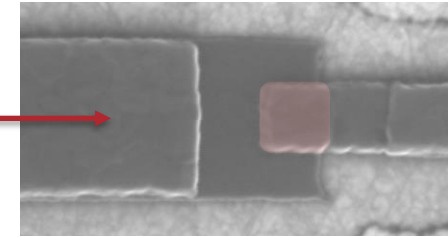
Plassys MEB550S



7.5 mm



20  $\mu\text{m}$

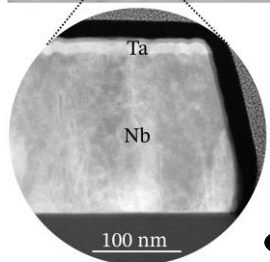
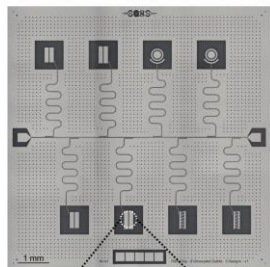


500 nm

# SQMS is at the Forefront of Qubit Coherence

## Top published transmon qubit coherence

Group	Best $T_1$ ( $\mu\text{s}$ )	Freq. (GHz)	Substrate	Primary Material	Publication Year
Yu	503	3.8-4.7	Sapphire	Ta, dry etch	2022
<b>SQMS</b>	<b>451</b>	<b>4.5-5</b>	<b>Silicon</b>	<b>Ta/Nb, dry etch</b>	<b>2023</b>
Houck	360	3.1-5.5	Sapphire	Ta, wet etch	2021
IBM	340	~4	Silicon	Nb, dry etch	2022
IBM	234	3.808	Silicon	Al, dry etch	2021
<b>SQMS</b>	<b>198</b>	<b>4.5-5</b>	<b>Sapphire</b>	<b>Ta/Nb, dry etch</b>	<b>2023</b>



### FNAL/UCicago - Pritzker Nanofabrication Facility



### NIST - Boulder Microfabrication Facility



### Rigetti - Fab-1 Integrated Circuit Foundry, Fremont CA

