

# Development of a Digital Electromagnetic Calorimeter Based on MAPS for Future Collider Detectors

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A collaborative effort on MAPS devices for future colliders strives to achieve sensors that meet the challenging requirements for both tracking and electromagnetic calorimetry. The effort is being pursued along with the CERN DRD 7.6 project and the DRD 6.1 project. SLAC leads the US role in sensor development, engaging with international efforts led by CERN and ALICE in the 65 nm development with a submission of a pixel sensor prototype in the ER1 run (within the CERN WP1.2 collaboration) and contributing effort to the ALICE ITS3 testing team [3]. Oregon supports the SLAC effort with simulation and testing contributions.

This project builds on SLAC's previously developed MAPS in several technologies, both for high-energy physics applications [1] as well as ultra-fast photon science [2]. SLAC is now investigating challenges of wafer-scale designs optimized for detectors at future e+e-machines, focusing in particular on Si Tracker and ECal [4]. This is a general challenge for MAPS application at any of the future Higgs Factories. This effort will help identify the risks that wafer-scale MAPS pose at system-level, with the goal to retire the high-risk technological challenges of such developments.

Participation in the CERN DRD 7.6 collaboration, that currently organizes the European led efforts on MAPS developments, is critical to maintain US presence in this effort and secure future leadership opportunities. Participating in the DRD7.6 collaboration is a key step for future MAPS developments, as it guarantees extensive technology transfer with several European partners. This will lead to reduced costs for future R&D endeavors in the United States.

Likewise, the DRD 6.1 collaboration provides the opportunities for applications in the calorimetry realm.

SLAC will design, simulate and integrate two critical components for MAPS at future detectors. The technology chosen for such developments is a 65nm CMOS imaging technology from TowerJazz Panasonic Semiconductor Co. The two blocks are:

- A Time to Digital Converter (TDC) circuit, with low-power consumption and a resolution compatible with the timing performance of the sensor (~100 ps).

- A Voltage Regulator which will address two critical issues which prevent the implementation of large area devices: voltage drop on the ASIC interconnections, and segmentation of the power domains to increase yield.

SLAC ASIC design efforts specialize in LDO, and serial powering. It is expected that collaborators, including students, will participate in dedicated testing campaigns at CERN to verify the performance of the current and future ASIC designs.

Simulation, led by Oregon, will advance the understanding of the ECal MAPS application, with impact of design choices and optimization made by the SLAC group. Early results of this simulation effort were presented at CALOR 2022 [4].

The next simulation efforts will include the following aspects:

- Optimization of energy measurement, including application of machine learning;
- Evaluation of ECal design choices (longitudinal and transverse segmentation, depth, and timing) to enable cost/performance trade-off studies;
- Support of SLAC device testing.

## References

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[2] L. Rota *et al.*, "Design of ePixM, a fully-depleted monolithic CMOS active pixel sensor for soft X-ray experiments at LCLS-II" <https://doi.org/10.1088/1748-0221/14/12/C12014>

[3] Rinella, Gianluca et al. "Digital Pixel Test Structures implemented in a 65 nm CMOS process" e-Print: 2212.08621 [physics.ins-det] <https://arxiv.org/abs/2212.08621>

[4] Brau, James E. and others, "The SiD Digital ECal Based on Monolithic Active Pixel Sensors", 10.3390/instruments6040051, Instruments, 6, 51 (2022)