OSU CDRD Optical Link Update

D. Shane Smith, K.K. Gan

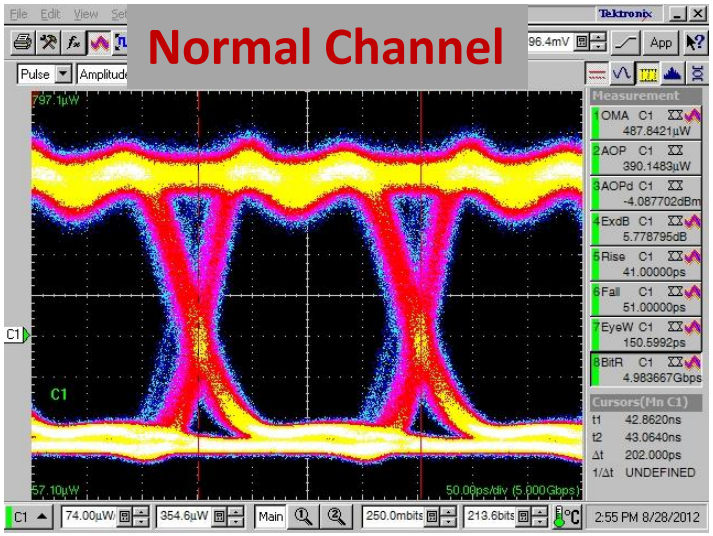
Overview

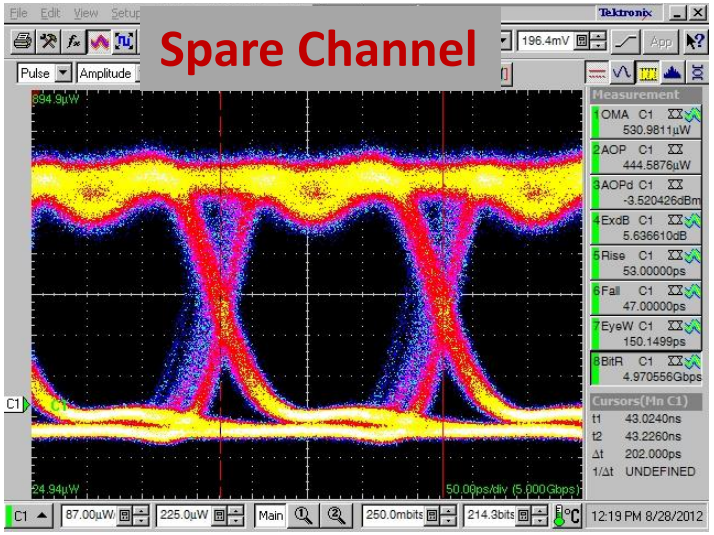
- 5 Gb/s VCSEL Array Driver Results
- Thoughts on 10 Gb/s VCSEL Driver Design
- Status of OSU 10 Gb/s VCSEL Driver Design

OSU 5Gb/s VCSEL Array Driver

- 130 nm CMOS
- 8 Channels + 4 optionally used spares
  - Works like a crosspoint switch: an input signal from any of the 8 inner channels can be routed to any of the spare VCSEL channels
- All channels including re-routed channels work at 5 Gb/s

5 Gb/s optical eyes, measured at Fermilab (thanks to Alan and John!)

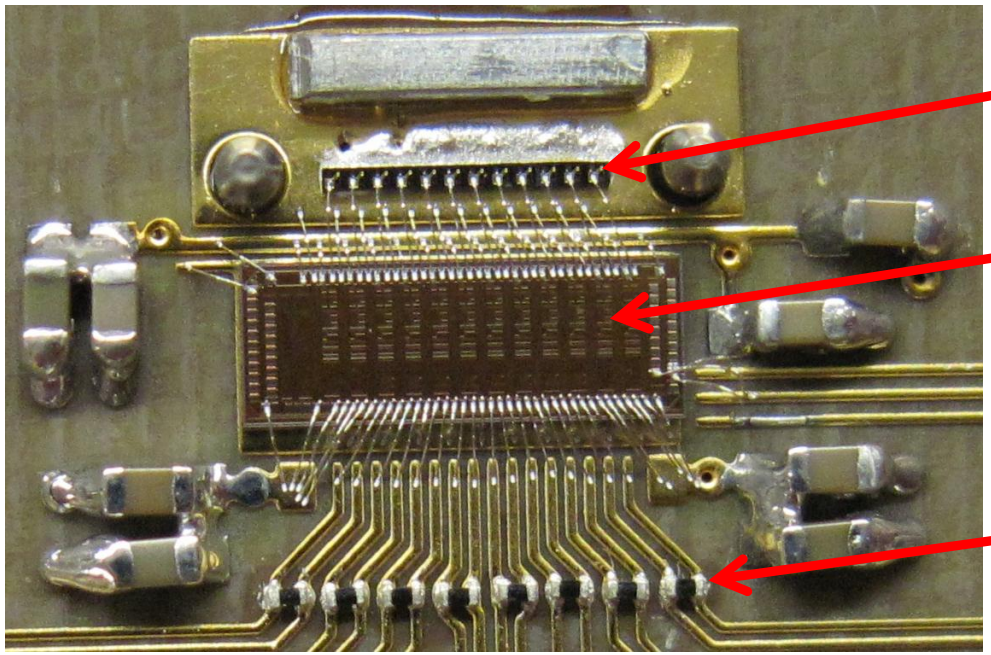




THE OHIO STATE UNIVERSITY DEPARTMENT OF PHYSICS

OSU 5Gb/s VCSEL Array Driver

- 2 irradiated array drivers + ULM 10Gb/s VCSELs (like shown below) at OSU awaiting measurement
  - Dose = 1.51×10^{15} 24 GeV protons / cm^2 (33 Mrad in GaAs)



10 Gb/s VCSEL Array Driver

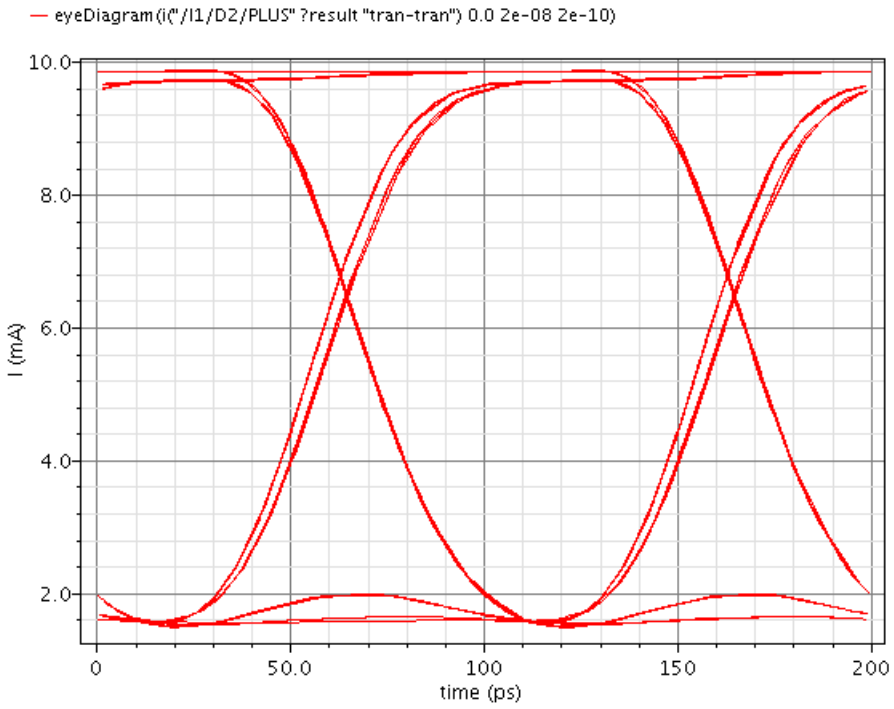
- From the literature and from commercial products, we know that a 10 Gb/s VCSEL driver is possible using:
  - 180 nm CMOS
  - 130 nm BiCMOS
  - 130 nm CMOS
  - 90 nm CMOS
  - …
- From our preliminary work, it seems that we can achieve 10 Gb/s in 130 nm CMOS
- If we can achieve this, great!
  - Low cost compared to BiCMOS or 65 nm

10 Gb/s Driver in 130 nm CMOS?

- To be possible, need different architecture than our present array driver ASIC (designed to be compatible with the present pixel system)
- Differential receiver
  - Use CML / LVPECL / ECL like receiver
    - LVDS or LVDS like above 4 Gb/s is not commercially available
  - Incorporate termination resistors
- VCSEL driver
  - Switch to using negative cathode bias allowing use of minimum size transistors (no thick oxide enclosed layout transistors)

10 Gb/s Driver Design Status

- Near final version of the driver stage layout completed
  - Works well at 10 Gb/s but plan to optimize further
- Currently focusing design efforts on differential receiver
- Plan to complete the design / layout before the next proposal renewal



Simulated VCSEL current eye driven by the VCSEL driver stage. This simulation uses the extracted layout (including bond pads) and also includes proven models of the VCSEL parasitics.

THE OHIO STATE UNIVERSITY DEPARTMENT OF PHYSICS

Summary

- Our 5 Gb/s VCSEL array driver works well
  - first demonstration of high-speed VCSEL array driver in HEP
- We believe a 10 Gb/s VCSEL driver is possible in 130nm CMOS and are working towards completing a prototype design