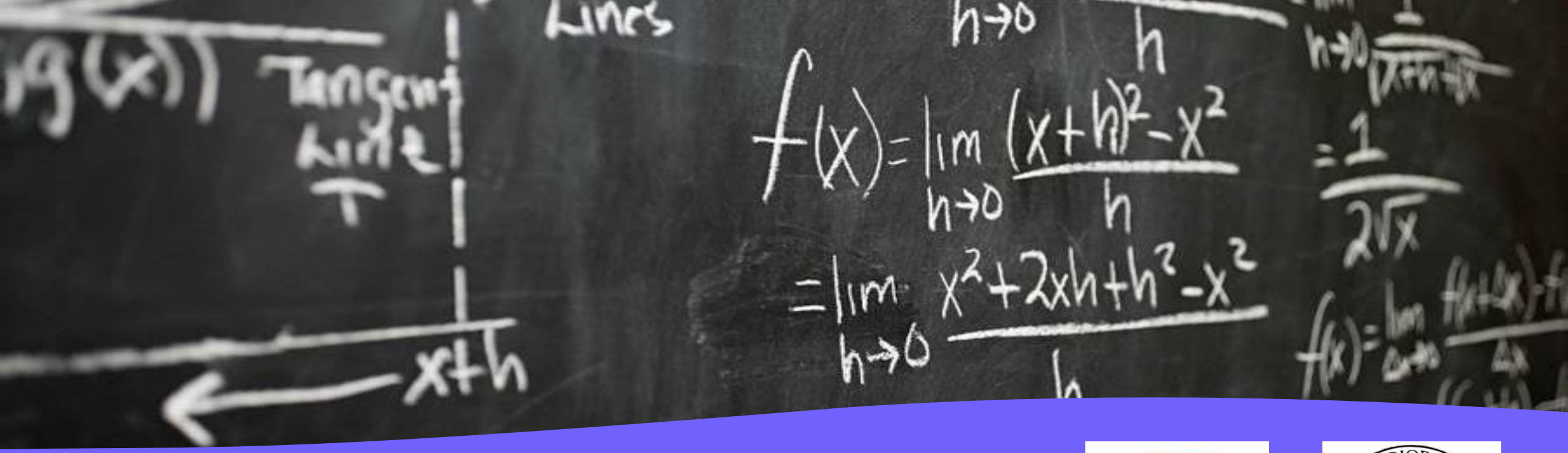


SRF Cavities Parasitic Modes Suppresion System

Helen Edwards intern: Matija Tomić

Supervisor: Alexander Netepenko

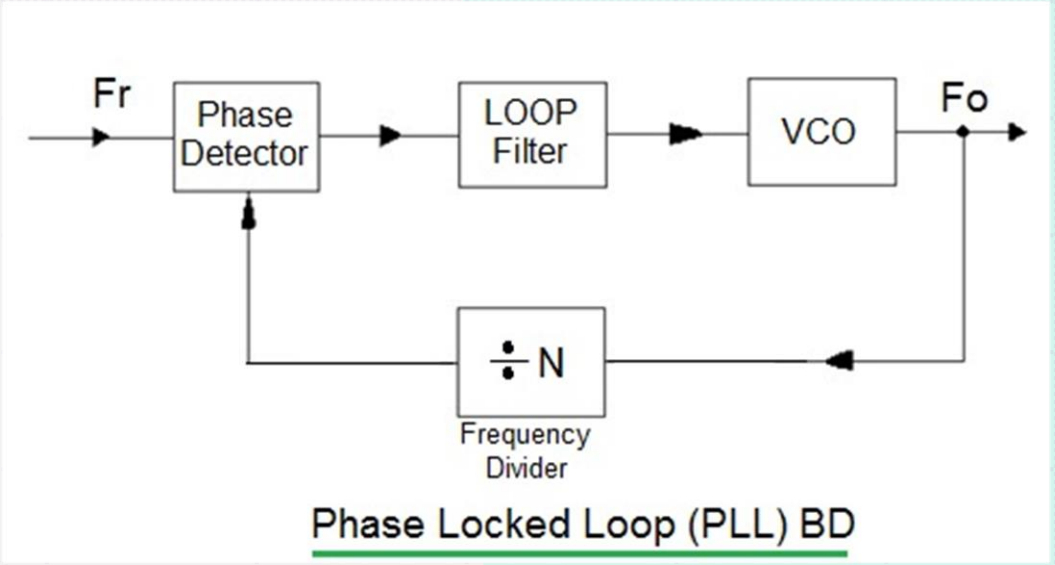
Problem

- 650MHz low-beta cavities – mode mixing behaviour which impedes the testing of their performance
- Capacitor and waveguide
- π and $\frac{4}{5}\pi$
- 650MHz and 649.5MHz

Goals

1. Phase Lock Loop implementation on FPGA
- PID controller
- Mixer – 1.3MHz and 0.8MHz
2. Digital filter
- FIR with N = 20
- Convolution - time – $y[n] = \sum_{i=0}^{N} f[i]x[n-i]$

  - frequency domain - $Y(w) = \mathrm{F(w)X(w)}$



Phase Locked Loop (PLL) BD

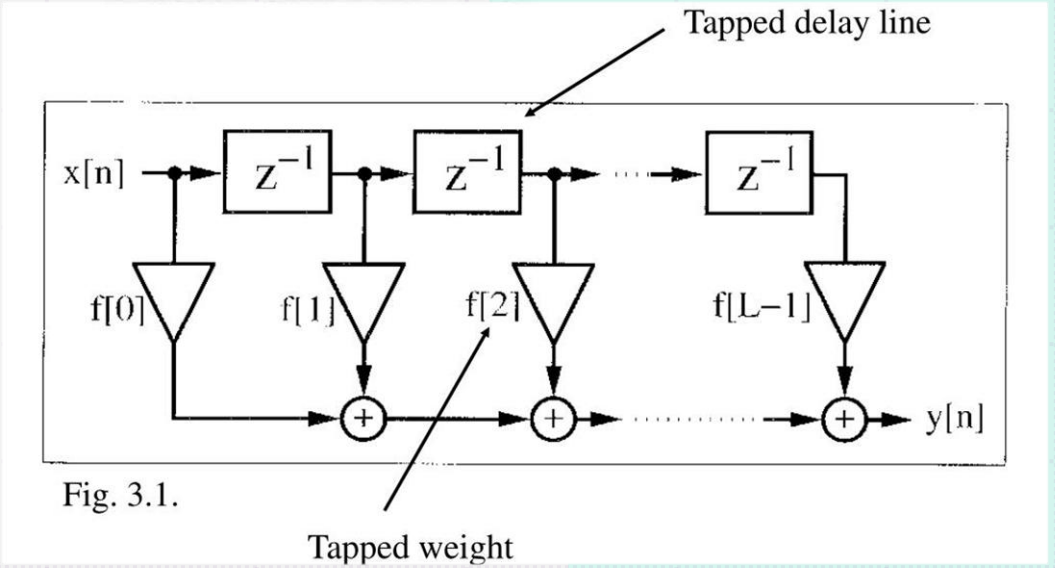


Fig. 3.1.

Thank you