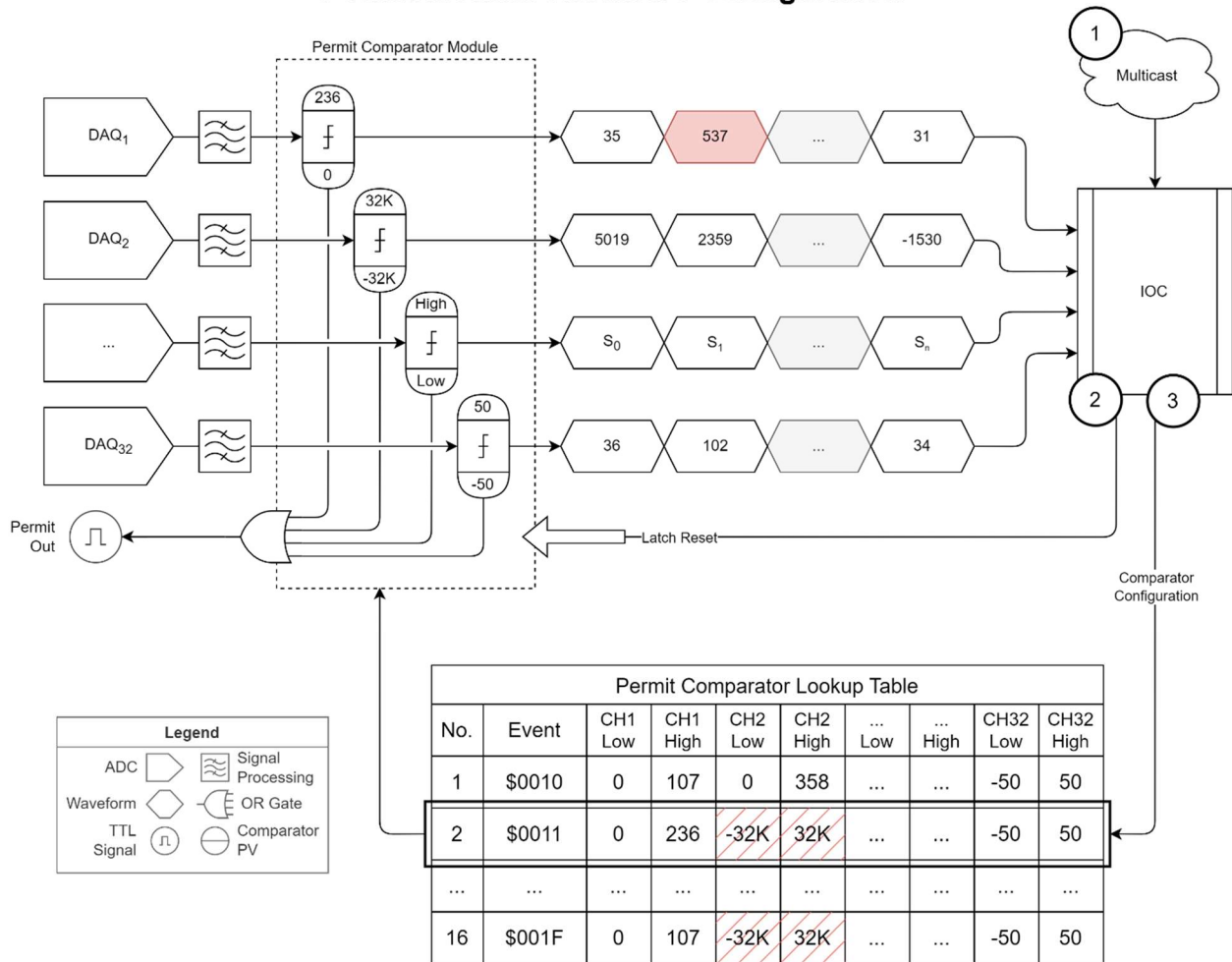


Permit Monitor Functional Specifications

The following *suggested implementation* outlines real-time Permit Monitoring functionality (the CAMAC C204 card equivalent) for the XRM. This functionality allows for dynamic monitoring of waveforms for accelerator fault or other abnormal condition. This functionality updates on Multicast event, offset by a Permit Update Timer, initiated by the Cycle Trigger. See diagrams.

1. The XRM shall have access to the Fermilab Multicast Table (FMT).
 - a. The FMT shall be transmitted at a minimum of 120~160Hz (8x the cycle rate).
 - b. The FMT shall be transmitted asynchronously to the actual machine cycles.
 - c. The FMT shall contain events to update the machine run mode
 - d. The FMT shall contain events to reset all permits.
2. The XRM shall have a Permit Lookup Table (LUT) to configure comparator parameters
 - a. The LUT shall have a minimum 16 run-mode configuration options available.
 - b. The LUT shall have a high and low parameter for each ADC channel on the device.
 - c. The LUT shall utilize 16b signed integers corresponding to the raw ADC values.
 - d. The LUT shall utilize +32768 or -32767 to indicate channels to be ignored (masked).
 - e. The LUT shall have a 'OK' parameter for each GPIO channel on the device.
 - f. The LUT shall utilize 1 or 0 to indicate the GPIO channel is in an allowed state.
 - g. The LUT shall utilize -1 to indicate GPIO channels to be ignored (masked).
 - h. The LUT shall be configured entirely by the consumer.
3. The XRM shall have Permit Comparator Module (PCM) embedded in the FPGA
 - a. The PCM shall be placed directly after the final processing stage of the ADC/ GPI.
 - b. The PCM shall have a comparator for all ADC/GPI channels present on the device
 - c. The PCM shall have an over/under threshold or 'OK' setting for each channel.
 - d. The PCM shall 'OR' all comparator signals to a single logic level.
 - e. The PCM shall utilize logic low to indicate one or more channels are out of range.
 - f. The PCM shall latch the permit, until reset by the IOC.
 - g. The PCM shall initialize to all zeros/ permit low on startup.
 - h. The PCM shall be configured by the LUT from the IOC at the end of each cycle.
 - i. The PCM shall have a watchdog timer that resets after each IOC update.
 - j. The PCM shall drop the permit if it does not update after 100ms (software fault).
 - k. The PCM shall present a status readback (high/low) for each channel to the IOC.
 - l. The PCM shall 'block' all permit transitions during the IOC update period.
4. The XRM shall configure the PCM with each Multicast Run Mode update.
 - a. The XRM shall have a Cycle Trigger designating in real time the start of each cycle.
 - b. The XRM shall have a Permit Update Timer at a set interval after the Cycle Trigger.
 - c. The XRM shall have variable delays from 0~49mS (1ms inc.) for the Permit Timer.
 - d. The XRM shall update the PCM from the LUT within 100uS of Permit Update Timer.
 - e. The XRM shall monitor the FMT for permit reset events, and reset on event.

Permit Monitor Hardware Configuration



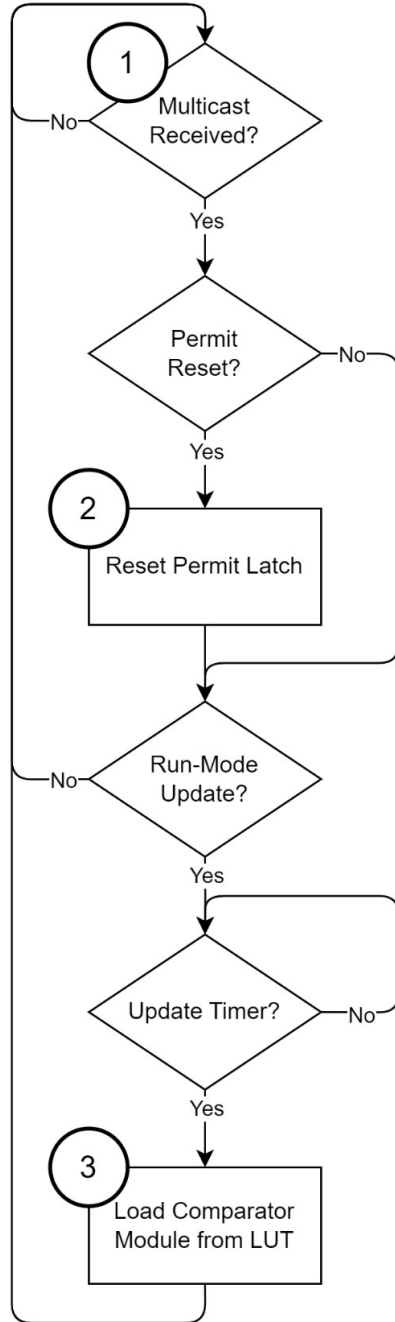
Graphical Depiction of Permit Monitor Functional Specifications.

Permit Monitor Functional Description

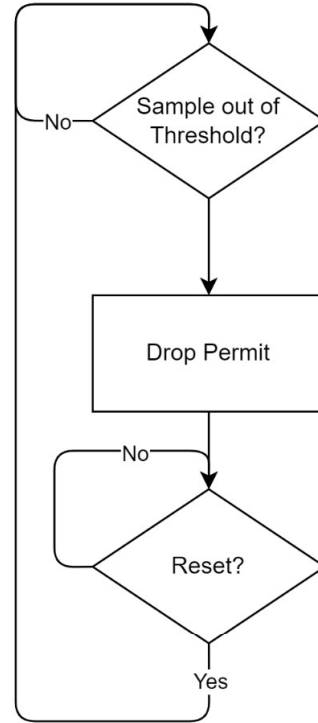
The above scenario operates as follows:

1. On Multicast Update, the IOC scans for permit resets, and run-mode updates.
2. If a 'permit reset event' is received the IOC unlatches the Permit Comparator Module (if set).
3. If a 'run-mode update event' is received, the IOC loads the PCM from the lookup table.
4. In parallel: when an out of threshold sample is received, the permit drops and is latched.

IOC



FPGA



Logical Depiction of Permit Monitor Functional Specifications