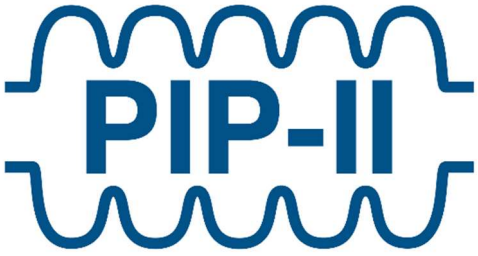

DAQ / XRM

Technical Requirements Specification

Document Number ED0013500-REVB

Evan Milton
January 15, 2024

Approvals

Role	Name	Method	Date
Originator	Michael Kucera		10/31/21
Originator	Evan Milton		12/31/24
Reviewer		Checker in TC	
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Approver		Approved TC	
Stakeholder		Dataset in TC	

Revision History

Rev	Description	Date
REVA	Original document for PDR	10/31/21
REVB	Updated document for FDR	12/31/24

Supporting Documents

No.	Reference	Doc. Number
1	PIP-II Requirements Management Plan	ED0008235
2	PIP-II Doc Management and Control Procedure	PIP-II Doc-DB-2946
3	PIP-II Quality Assurance Plan	PIP-II Doc-DB-142
4	PIP-II Controls L3 FRS	ED0008101
5	PIP-II Accelerator Systems QA Plan	PIP-II Doc-DB-4805
6	PIP-II Global Requirements Document	ED0001222
7	PIP-II Control System PRD	ED0010225
8	C204 Beam Permit Module Specifications	N/A
9	Permit Monitor Functional Specifications	N/A
10	Sample on Event Functional Specifications	N/A
11	PIP-II DAQ/XRM First Article Test Plan	TBD
12	PIP-II DAQ/XRM Incoming Inspection Traveler	TBD

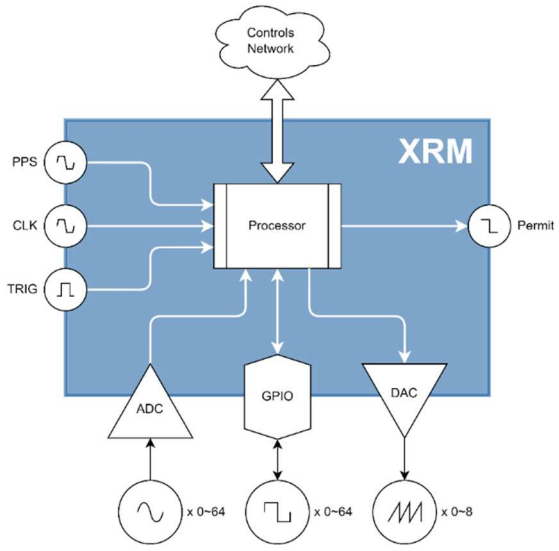
Contents

Overview

The following document outlines a set of requirements for Rack Monitors (RM) intended for deployment with the PIPII accelerator. The Rack Monitor has been given the designation 'XRM' to distinguish it from previous 'PIRM, IRM, HRM, and MADC' hardware modules. The requirements are to be finalized after vendor selection. Please see internal document TRS ED0013500 for the original requirement set.

System Definition

Rack monitors are a vital component of the Fermilab accelerator complex, enabling real-time data acquisition, monitoring, and control. Developed for the PIP-II project at Fermilab, the XRM enhances this functionality and standardizes interfaces across data acquisition platforms. With modular I/O, time synchronization, and high-speed analog capabilities, it supports both the flexibility needed for commissioning and the reliability required for long-term operation. Its EPICS-based software ensures real-time monitoring, dynamic reconfiguration, and secure communication meet PIP-II's stringent performance demands.



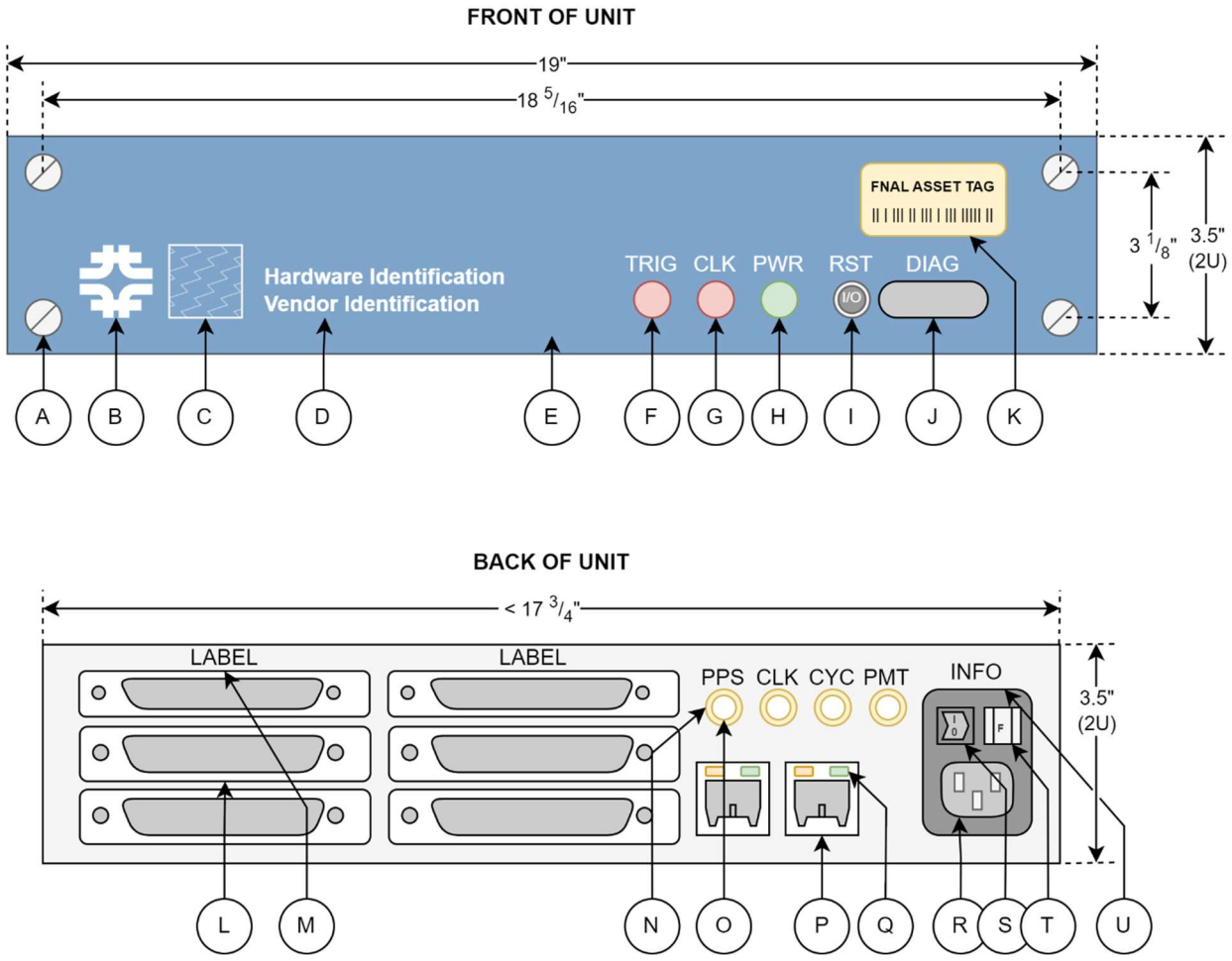
Relevance to the PiRM

The XRM is the latest in a long lineage of voltage readback devices at Fermilab, following the PiRM, IRM, HRM, and MADC, all of which have supported critical systems since 1975. This history underscores the need for a stable, long-term rack monitor platform. These XRM requirements aim to establish reliable hardware that can adapt to future applications. By leveraging tools like EPICS to abstract the hardware interface, a consistent platform can be maintained, simplifying future upgrades and reducing associated labor demands.

Specifications

Physical Specifications [T-ED0013500-Pxxx]

The following requirements are intended to support safe installation and maintenance of the XRM unit. Please Reference the diagram for all callouts. EIA-310 and connector datasheets supersede all dimensions shown. This drawing is not to scale, and no layout is specified for front and back panels. Final article subject to Fermilab approval.



XRM Physical Specifications

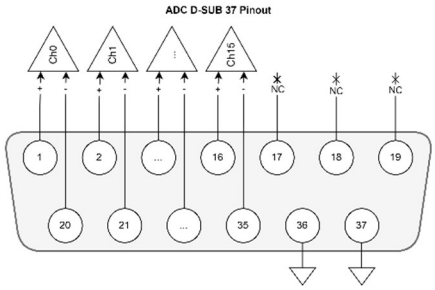
Physical Specifications (Continued)

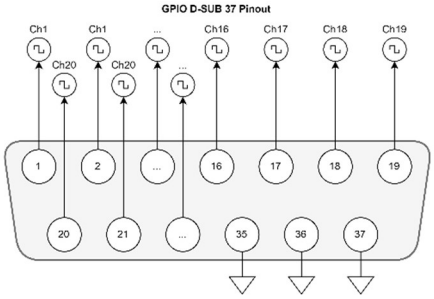
1. The XRM shall comply to the EIA-310 form factor for 19” rack units (A)
2. The XRM shall be no taller than 2U (3.5”) high, <27” deep. (A)
3. The XRM shall display vendor and Fermilab logos for order quantities greater than 10 (B/C)
4. The XRM shall display hardware and vendor identification on the front panel (D)
   (See: Fermilab | Graphics Standards at Fermilab | Logo and usage)
5. The XRM shall have a NAL Blue panel w/ white text for order quantities greater than 10 (E)
   (See: Fermilab | Graphics Standards at Fermilab | Color palette)
6. The XRM shall have a red status indicator (LED) for when the Cycle Trigger is active (F)
7. The XRM shall have a red status indicator (LED) for when the ADC Clock is active (G)
8. The XRM shall have a green status indicator (LED) on the front when operational (H)
9. The XRM shall have a physical momentary reset switch, located at the front of the unit (I)
10. The XRM shall have a diagnostic interface via USB connector on the front of the unit (J)
    a. The connector *should* be USB-C to facilitate forward compatibility.
11. The XRM shall have an Asset Tag, to be applied by Fermilab at time of acceptance (K)
12. The XRM shall place all connectorization (excepting diagnostic) at the back of the unit (L)
13. The XRM shall utilize panel mount connectors for all external interfaces (L)
14. The XRM shall support the general I/O and Analog connector options listed below (L)
    Only one connector type is utilized for a given module, to be identified at procurement.
    a. DB-37, see separate pinout
    b. DB-9, see separate pinout
    c. Coaxial connector for high-speed analog signals
    d. (Future versions of the XRM may utilize Mil-Spec circular connectors)
15. The XRM shall clearly identify all connectors on the front and back of unit (M)
16. The XRM shall have TTL I/O for Pulse Per Second, ADC Clock, Cycle Trigger, and Permit (N)
17. The XRM shall utilize BNC, SMA, or LEMO connectors for all dedicated TTL inputs (O)
18. The XRM shall have a network interface(s) via RJ-45 and SFP connector (P)
19. The XRM shall have status indicator LEDs near the network ports to indicate connectivity (Q)
20. The XRM shall utilize standard NEMA 5-15P to C13/14 power cabling (R)
21. The XRM shall have a physical on/off power switch, located near the power connector (S)
22. The XRM shall have a physical fuse, located near the power connector (T)
    (See: Power Entry Modules (PEM) | AC Power Connectors | Electronic Components)
23. The XRM shall have external labeling for *all* electrical constraints (voltage, current req’s) (U)

Interfaces [T-ED0013500-Ixxx]

The following requirements are intended to standardize interfaces across Fermilab Rack Monitor devices and support backwards compatibility. Some high speed (>1MHz) applications may require alternate connector pinouts.

1. The XRM shall support a Reset Switch (RST) to power cycle or restart the device.
2. The XRM shall support a Power Switch (PWR) to physically enable power to the device.
3. The XRM shall support a Pulse Per Second (PPS) interface for synchronization of time.
4. The XRM shall support an ADC Clock (CLK) interface for synchronous data acquisition.
5. The XRM shall support a Cycle Trigger (CYC) interface to instigate data acquisition periods.
6. The XRM shall support a Beam Permit interface (PMT) to transmit permit information.
7. The XRM shall support a Diagnostic Interface (DIAG) through a USB port.
8. The XRM shall support configuration and data transmission via ethernet.
9. The XRM shall use a standard connector for 120V power (see physical spec)
10. The XRM shall have a coaxial option for high speed (>1MHz) ADC/DAC channels.
11. The XRM shall use a standard connector for GPIO and Analog functions (see physical spec).
12. The XRM shall use a standard pinout for general ADC and GPIO channels (see below).





ADC Pinout (DB37)			
Signal	Pin		Signal
CH1 +	1	20	CH1 -
CH2 +	2	21	CH2 -
CH3 +	3	22	CH3 -
CH4 +	4	23	CH4 -
CH5 +	5	24	CH5 -
CH6 +	6	25	CH6 -
CH7 +	7	26	CH7 -
CH8 +	8	27	CH8 -
CH9 +	9	28	CH9 -
CH10 +	10	29	CH10 -
CH11 +	11	30	CH11 -
CH12 +	12	31	CH12 -
CH13 +	13	32	CH13 -
CH14 +	14	33	CH14 -
CH15 +	15	34	CH15 -
CH16 +	16	35	CH16 -
NC	17	36	GND
NC	18	37	GND
NC	19		

Digital Pinout (DB37)			
Signal	Pin		Signal
CH1	1	20	CH20
CH2	2	21	CH21
CH3	3	22	CH22
CH4	4	23	CH23
CH5	5	24	CH24
CH6	6	25	CH25
CH7	7	26	CH26
CH8	8	27	CH27
CH9	9	28	CH28
CH10	10	29	CH29
CH11	11	30	CH30
CH12	12	31	CH31
CH13	13	32	CH32
CH14	14	33	GND
CH15	15	34	GND
CH16	16	35	GND
CH17	17	36	GND
CH18	18	37	GND
CH19	19		

Present DB-37 definition, subject to change at contract approval.

Compliance [T-ED0013500-Cxxxx]

The following requirements are intended to facilitate acceptable quality and safety standards for the unit upon receipt. These standards address the variety of environmental and handling conditions to which the XRM will be subjected. Fermilab reserves the right to independently test first article units against the conditions listed below.

1. The XRM shall have an estimated MTTF in excess of 100,000 hours (>11years).
2. The XRM shall comply with IEC 61010 safety standards for Inst. & Control hardware
    a. Comparable IEC standards / EU standards may be applied herein.
3. The XRM shall have a UL listed 120V power conversion stage, located internal to the unit
4. The XRM shall have a Category II over-voltage rated power conversion stage per IEC 61010.
5. The XRM shall recover gracefully from under-voltage scenarios after manual reset.
6. The XRM shall have a grounded chassis.
7. The XRM shall be RoHS compliant.
8. The XRM shall have overvoltage protection for all inputs and outputs.
9. The XRM shall comply with IEC 61000-4-2 standards for electrostatic discharge immunity
10. The XRM shall comply with IEC 61000-4-3 standards for radiated electromagnetic fields
11. The XRM shall be installable by a single individual without lift or rigging.
12. The XRM shall maintain functionality in a commercial operating range per IEC 60068
    a. The XRM shall operate from 0~50°C
    b. The XRM shall operate from 5~95%RH (non-condensing)
    c. The XRM shall operate with vibrations from 15~60Hz, 0.15~0.5mm displacement
    d. The XRM shall be subject to drop (100mm) and impact (5g) during normal handling.
    e. The XRM shall have airflow from the front to the back of the rack enclosure.
    f. The XRM shall be IP50 rated for dust ingress.

    (The XRM *need not* be independently certified to the above standards)

Documentation/ Appearance [T-ED0013500-Dxxx]

1. The XRM shall have comprehensive documentation for all hardware and software features.
2. The XRM shall be maintained in a version-controlled software repository by the vendor. (The XRM need not have an open software or hardware documentation).
3. The XRM shall have a troubleshooting procedure for basic functionality including:
    a. Initial startup and network connectivity
    b. Configuration of startup scripts
    c. Loading and navigation of the engineering page
    d. Identity and function of available PV's
4. The XRM shall have a partial schematic of all I/O ports to ensure electrical compliance.
5. The XRM shall have a Fermilab applied Asset Tag, linked to an internal database.

Performance Agreement [T-ED0013500-Exxx]

The following requirements are intended to facilitate acceptable support levels for the duration of the XRM service life. As controls infrastructure in the PIP-II accelerator

1. The XRM shall arrive fully tested, qualified, and ready for installation.
2. The XRM shall have a manufacturer-supported service life in excess of 10 years.
3. The XRM shall have post-commissioning support for firmware or security patches.
4. The XRM shall maintain compliance with the active safety standards at time of purchase.
5. The XRM shall have service availability via email or phone within 24 hours of request.
6. The XRM shall have a backwards-compatible form factor for inter-lifecycle updates.
7. The XRM shall have a hardware warranty period of one year from date of receival.
8. The XRM shall have an extended warranty period option.
9. The XRM shall have a procurement time less than 6 months, batch shipments acceptable.
10. The XRM shall have pricing valid from 90 days of quote during procurement.
11. The XRM shall have vendor support for NRE required to modify functional requirements.
12. The XRM shall have vendor support for NRE required to modify software requirements.
13. The XRM shall have an IP transfer agreement in the event of manufacturer default.

Software Interface Requirements [T-ED0013500-Sxxx]

1. The XRM shall utilize EPICS for all software configuration and readback on request.
2. The XRM shall interface with Fermilab operator interface via EPICS-based Phoebus.
3. The XRM shall interface with Fermilab's EPICS archiving tools (Archiver Appliance).
4. The XRM shall support EPICS PV Access (PVA) protocols for network data exchange.
5. The XRM shall provision for migration to the excessively named PVXS implementation.
6. The XRM shall support EPICS Channel Finder functionality.
7. The XRM shall provide a template startup script for the base vendor configuration.
8. The XRM shall utilize a version controlled Fermilab startup script post installation.
9. The XRM shall support dynamic startup script configuration through SSH (push).
10. The XRM shall have internal diagnostic logs accessible via network or local diagnostic port.
11. The XRM shall have vendor-provided engineering screens to verify basic functionality.
12. The XRM shall allow reconfiguration of parameters via GUI or command-line without reboot.
13. The XRM shall provide configurable save/restore functionality, and power failure recovery.
14. The XRM shall support network power-off or restart commands.
15. The XRM shall have root privilege for Fermilab to administer certificates and security config.
16. The XRM shall adhere to site-specific security policies and DOE regulations.
17. The XRM shall have Kerberos-based authentication for all client access to the processor. (Fermilab shall provide Kerberos configuration files)

Functional Requirements

Hardware Requirements [T-ED0013500-Hxxx]

1. The XRM shall have variable configurations, to be selected at time of procurement.
2. The XRM shall have a minimum of 6 slots, each with one of the following options:

	Unit			Spec's					
	Type	Rate (sps)	Range	Channel	Res. (bits)	-3dB (Hz)	Term. (Ω)	Cur. (mA)	Conn.
3	GPIO	1M	5V (TTL)	32	-	-	4.7K Dn	64/32mA	DB-37
4	Relay	20	5V	4	-	-	-	100mA	DB-9
5	DAC	100K	±10V	4	≥16	~10K	1M	10mA	DB-9
6	ADC	100K	±10V	16	16	~50K	1M	-	DB-37
7	ADC	100K	±5V	16	16	~50K	1M	-	DB-37
8	ADC	100K	±2.5V	16	16	~50K	1M	-	DB-37
9	ADC	≥2M	±10V	16	≥16	~500K	1M	-	COAX
10	ADC	≥2M	±2.5V	16	≥16	~500K	1M	-	COAX
11	ADC	≥2M	±1V	16	≥16	~500K	1M	-	COAX

General Functionality [F-ED0013500-Fxxx]

1. The XRM shall have local time with an accuracy of 1uS against a global clock (PPS Input).
2. The XRM shall have a Cycle Trigger designating the start of each machine cycle (CYC Input).
3. The XRM shall be capable of functioning at both 15Hz and 20Hz machine cycle rates.
4. The XRM shall update status PV's at twice the machine cycle rate (30Hz or 40Hz).
5. The XRM shall have an internal Return Timer designating the middle of each cycle.
6. The XRM shall have an internal Permit Timer designating the end of each cycle.
7. The XRM shall have a Clock Input to synchronize various internal functions (CLK Input).
8. The XRM shall have a Permit Output to alert external systems (PMT Output).
9. The XRM shall have permit monitoring functionality for all DAC/GPIO channels (see below)
10. The XRM shall have Postmortem Capture functionality (see separate document).
11. The XRM shall have software alarms for over-temperature conditions of the hardware.
12. The XRM shall have settable software alarm thresholds on all DAC/GPIO channels.
13. The XRM shall have remote power off/ power cycle functionality.
14. The XRM shall power down when the reset button is pressed for more than 5 seconds.
15. The XRM shall otherwise perform a soft power cycle when the reset button is pressed once.

GPIO Functionality [T-ED0013500-Gxxx]

1. The XRM shall update General Purpose Outputs on Cycle Trigger event only.
2. The XRM shall support GPO updates triggered externally at 15Hz or 20Hz (CYC input)
3. The XRM shall support GPO updates triggered internally at 15Hz or 20Hz
4. The XRM shall support GPO update delays from 0~49ms at 1uS intervals.
5. The XRM shall support GPI sample rates from an external trigger (CLK input).
6. The XRM shall support GPI sample rates from an internal clock.
7. The XRM shall utilize the same sample rate for all GPI's installed in a given unit.
8. The XRM shall support GPI state(s) as Time/Value pairs for each channel.
9. The XRM shall capture the state of an input on change (high to low, or low to high).
10. The XRM shall capture the state of *all* inputs at Cycle Trigger and Return Timer (30Hz/40Hz).
11. The XRM shall update the Return PV at Cycle Trigger and Return Timer with all captures.
12. The XRM shall retain the preceding 1 second (30 or 40) of Return PV's internally.
13. The XRM shall make any of the available return PV's available upon request.
14. The XRM shall index return PV's from 0 to -39, with 0 being the most recent PV.

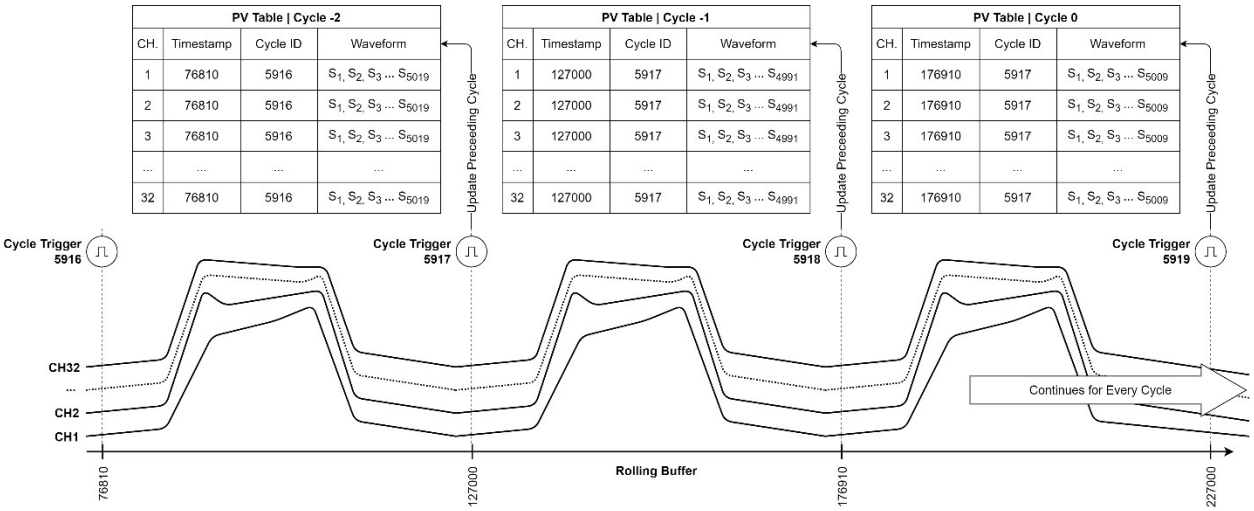
DAC Functionality [T-ED0013500-Jxxx]

1. The XRM shall support DAC's with continuous waveform generation functionality.
2. The XRM shall support DAC waveform generation rates from an external trigger (CLK input).
3. The XRM shall support DAC waveform generation rates from an internal clock.
4. The XRM shall utilize the same generation rate for all DAC's installed in a given unit.
5. The XRM shall support waveforms of variable length from 1~100K samples.
6. The XRM shall support the following waveform configuration options:
    a. User provided waveform, ±10V, cycle-by-cycle repetition, provided via PV
    b. User provided voltage (DC setting), ±10V, configured via PV.
    c. User selectable SIN or COS, 1~5000Hz, ±10V, 1Hz repetition, configured via PV.
    d. User selectable Pulse, 0~49ms width, ±10V, cycle-by-cycle rep, configured via PV.
7. The XRM shall support waveform generation triggered externally at 15Hz or 20Hz (CYC).
8. The XRM shall support waveform generation triggered internally at 1Hz, 15Hz or 20Hz.
9. The XRM shall support waveform generation delays from 0~49ms at 1uS intervals.
10. The XRM shall support continuous generation cycles up to 1s, utilizing an internal trigger.
11. The XRM shall support segmented generation cycles up to 49ms at 20Hz or 65ms at 15Hz.
12. The XRM shall hold the value of the last sample between waveform generation cycles.
13. The XRM shall update the waveforms to be played out at Cycle Trigger only.
    (The XRM DAC shall have a 10KHz LPF to limit step noise in downstream systems, per spec)
14. The XRM shall have factory calibrated DAC settings that are in units of Volts (1% tolerance).
15. The XRM shall have configurable raw DAC binary to Volt scaling factors, accessible via PV.

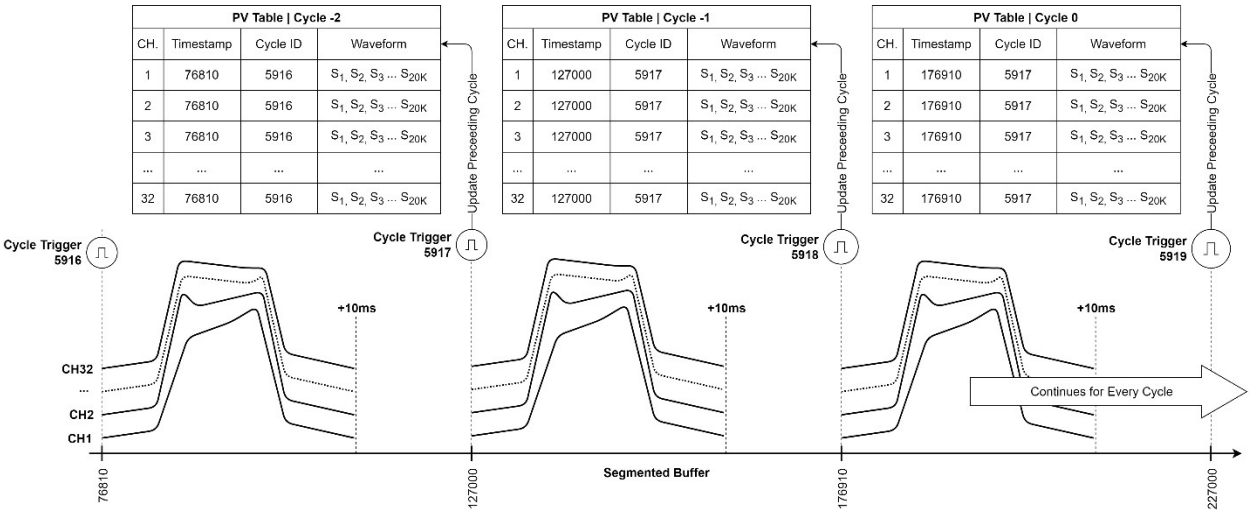
ADC Functional Requirements [T-ED0013500-Axxx]

The following requirements outline the base functionality required by XRM users. This functionality is to be facilitated through EPICS

1. The XRM shall support ADC's with continuous sampling functionality.
2. The XRM shall support continuous acquisition for 64ch x 100Ksps configurations
3. The XRM shall support segmented acquisition for 16ch x 2Msps @20% duty factor.
4. The XRM shall support ADC sample rates from an external trigger (CLK input).
5. The XRM shall support ADC sample rates from an internal clock.
6. The XRM shall utilize the same sample rate for all ADC's installed in a given unit.
7. The XRM shall support acquisition cycles of dynamic length.
8. The XRM shall support acquisition cycles of fixed length, up to 49ms/20Hz or 65ms/15Hz.
9. The XRM shall delineate acquisition cycles according to an acquisition cycle trigger.
10. The XRM shall support variable acquisition cycle trigger delays at 1uS increments.
11. The XRM shall support acquisition cycles triggered externally at 15Hz or 20Hz (CYC input).
12. The XRM shall support acquisition cycles triggered internally at 15Hz or 20Hz
13. The XRM shall utilize the same acquisition cycle trigger for all ADC's installed in a given unit.
14. The XRM shall tag the resultant waveform with the time at sample 0.
15. The XRM shall tag the resultant waveform with the active cycle number (Pulse ID).
16. The XRM shall obtain the Pulse ID and other information from the Fermilab Multicast Table.
17. The XRM shall update the resultant waveform PV at the start of the succeeding cycle.
18. The XRM shall retain the preceding one second of data (15 or 20 waveforms) internally.
19. The XRM shall make any of the available waveforms PV's available upon request.
20. The XRM shall index waveforms from 0 to -19, with 0 being the most recent waveform.
21. The XRM shall support Sample on Event functionality for 100Ksps fixed rate ADC



Rolling buffer of waveforms ~ dynamic length



Segmented buffer of waveforms ~ fixed length