Timing Distribution Test for Mu2e Experiment

Brianna Dewey – SIST Intern, Saint Mary's College

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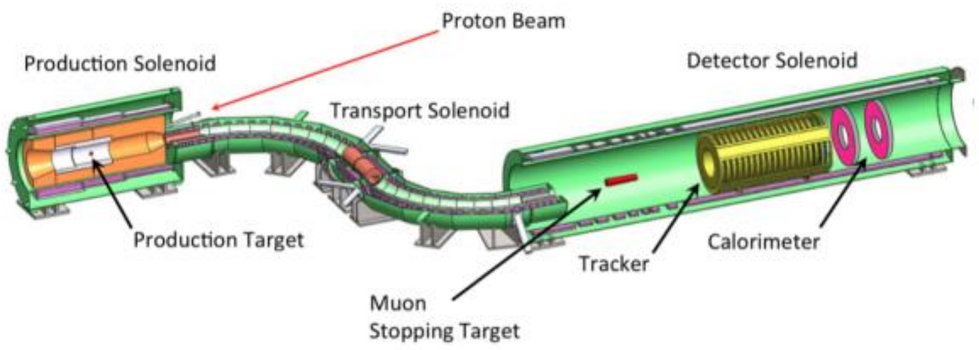
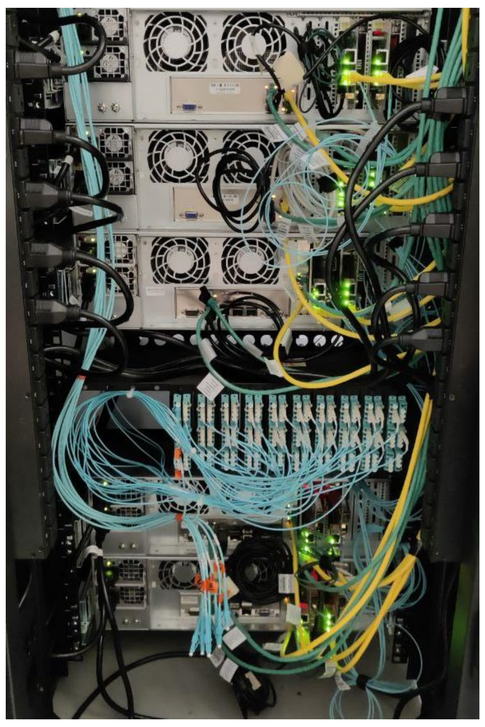
Mu2e Experiment

The purpose of the Mu2e experiment is to research the neutrino-less conversion of the muon into an electron in the field of an aluminum nucleus. Further, Mu2e aims to demonstrate the existence of physics beyond the Standard Model through this process due to the charged lepton flavor violation. The experimental technique employed by Mu2e experiment is designed to improve the sensitivity by 10^4 compared to similar experiments.



Mu2e apparatus is shown in the image above.

TDAQ – Trigger and Data Acquisition



TDAQ server located in the DAQ room of the Mu2e building.

The TDAQ is a subsystem of the Mu2e experiment implemented for collecting digitized data and delivering that data to online and offline processing for analysis. It is also responsible for detector synchronization, control, monitoring, and operator interfaces. It provides a timing and control network for precise synchronization and control of the data sources and readout, along with a Detector Control System (DCS) for operational control and monitoring of all Mu2e subsystems.

Purpose

The goals of the summer internship were to:

- Gain a working understanding of VHDL for use in FPGA firmware design.
- Assist in testing of the timing system of the TDAQ.
- Assist in testing the DIRAC board (Digitizer Readout Controller).
- Design and program a Raspberry Pi to allow remote access to the DIRAC board.

Thank you to my SIST project supervisor, Micol Rigatti, for an interesting and immersive internship.

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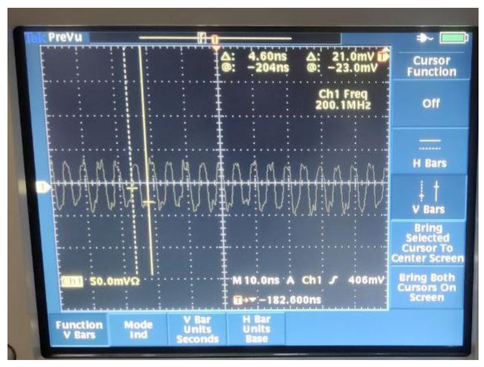
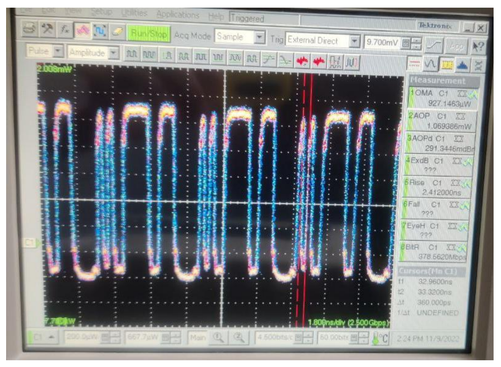
Mu2e Timing Distribution

The Mu2e timing distribution is based on contiguous Mu2e Event Windows synchronized across all the front ends. The FEs extract a system clock from a Command Fan-Out Module (CFO). The quality of the clock signal spread from the CFO has been tested to prove the accuracy of this configuration and find and test alternative solutions, e.g. the use of an RJ45 Timing Fanout (RTF).



RTF 200 MHz reference clock signal.

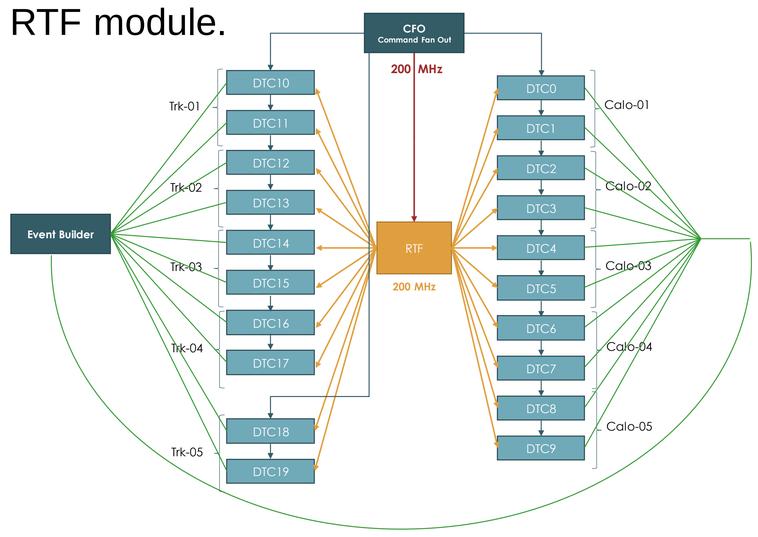


CFO optical signal (20x200MHz).

Timing Synchronization

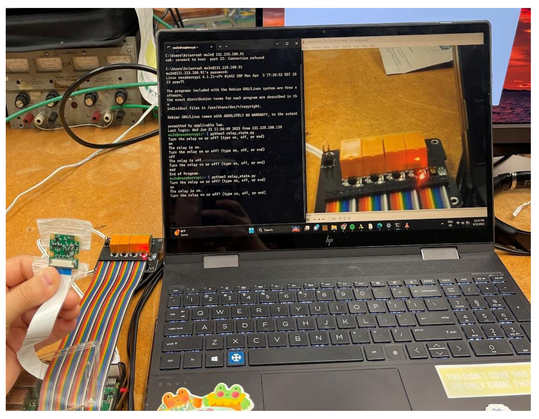
The CFO spreads the clock first to the Data Transfer Controller (DTC) boards. The DTCs are configured in a chain: the first one extracts the 200 MHz clock and passes it to the next one. To prevent jitter accumulation, all the DTCs are also receiving a 200 MHz Reference Clock from the RTF module.

The current DAQ Room Configuration shows the RTF sending the clock signal in parallel to all DTCs to mitigate the problem of propagation delay.

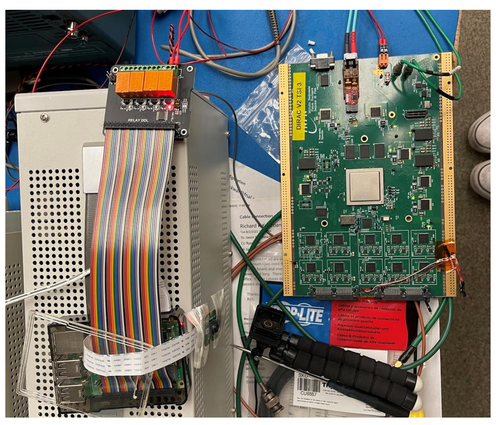


Raspberry Pi for Remote Access to the DIRAC

To allow remote access to the DIRAC board to the various teams involved in the development and testing, a Raspberry Pi has been programmed to control a relay managing the power down/up of the board. Video streaming has also been developed to observe the state of the board.



Shows the Raspberry Pi and relay setup used to remotely control the FPGA. Computer screen is used to display a livestream of the working board and allow the user to change the state of the board.



Shows the FPGA connected to the Raspberry Pi and relay setup.