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The SiD Digital ECal Based on Monolithic Active Pixel Sensors

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on behalf of
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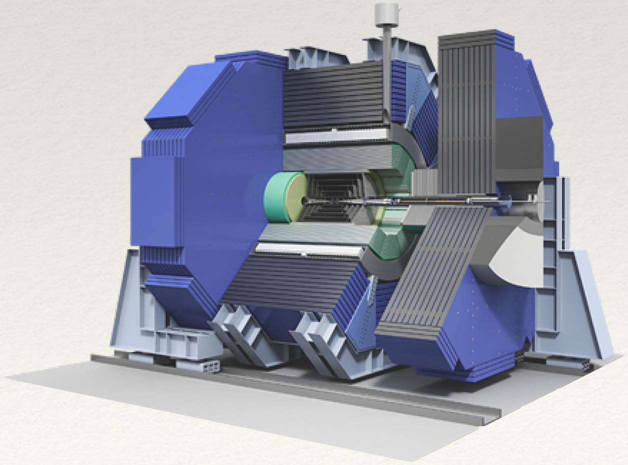
Introduction - MAPS for Linear Higgs factory ECal

- Higgs factory detectors need unprecedented precision.
- Ambitious physics goals demand challenging detector requirements on tracking and calorimetry.
  - High precision and low mass trackers,
  - Highly granular calorimeters.
- Monolithic Active Pixel Sensor (MAPS) technology offers needed advances.
- Sensors and readout circuitry are combined in pixels,
  - Fabricated with commercial CMOS processes.
- Currently MAPS widely used in HEP, astronomy and photonics,
  - Inner Tracking System Upgrade (ITS2) of ALICE at LHC.



Potential Attributes - MAPS for Linear Higgs factory

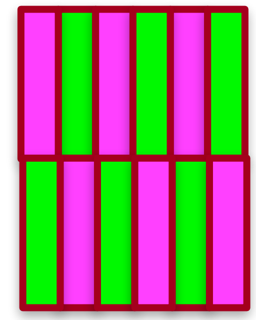
- Small pixel (down to ~ 10 μm) → High Granularity
- Small sensor capacitance (few fF)→ better performance for lower power consumption than hybrid detectors
- Low material budget → The wafer can be thinned (<100 μm)
- Fast production → no bump bonding necessary
- Relatively cheap solution, using commercial CMOS imaging technologies
- Possibility of large stitched sensor → up to 30 cm x 10 cm
- Timing to < ns-rms (with <115 mW/cm^2 × DutyFactor; DutyFactor<1% for LC)

Noise ⇩ Power ⇩ Cost ⇩

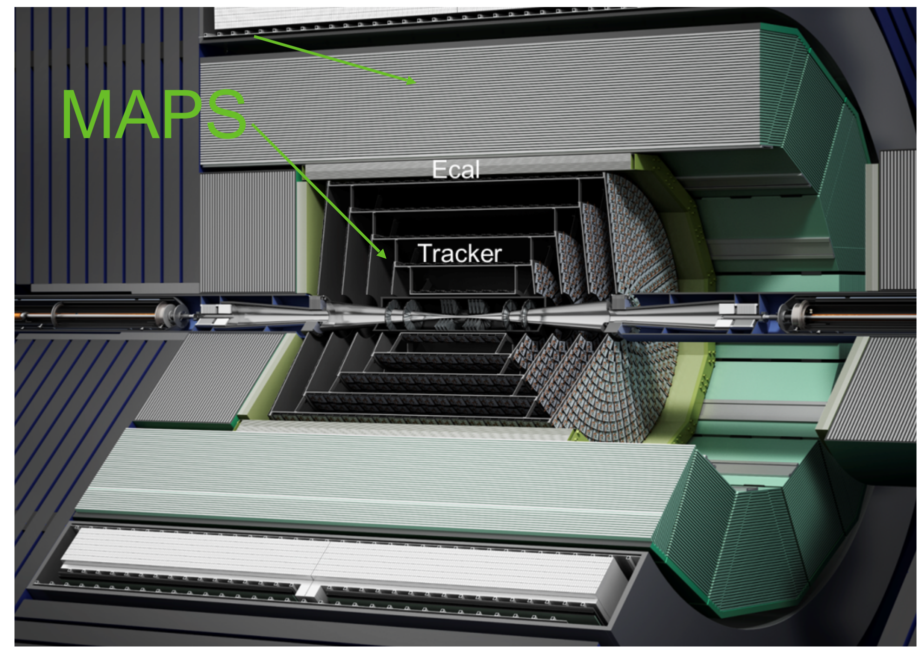
Main specifications for Large Area MAPS development

TID-AIR SLAC

Parameter	Value	Notes
Min Threshold	140 e^-	0.25*MIP with 10 μm thick epi layer
Spatial resolution	7 μm	In bend plane, based on SiD tracker specs
Pixel size	25 x 100 μm^2	Optimized for tracking
Chip size	10 x 10 cm^2	Requires stitching on 4 sides
Chip thickness	300 μm	<200 μm for tracker. Could be 300 μm for EMCal to improve yield.
Timing resolution (pixel)	~ ns	Bunch spacing: C^3 strictest with 5.3->3.5 ns; ILC is 554 ns
Total Ionizing Dose	100 kRads	Total lifetime dose, not a concern
Hit density / train	1000 hits / cm^2	
Hits spatial distribution	Clusters	Due to jets
Balcony size	1 mm	Only on one side, where wire-bonding pads will be located.
Power density	20 mW / cm^2	Based on SiD tracker power consumption: 400W over $67m^2$

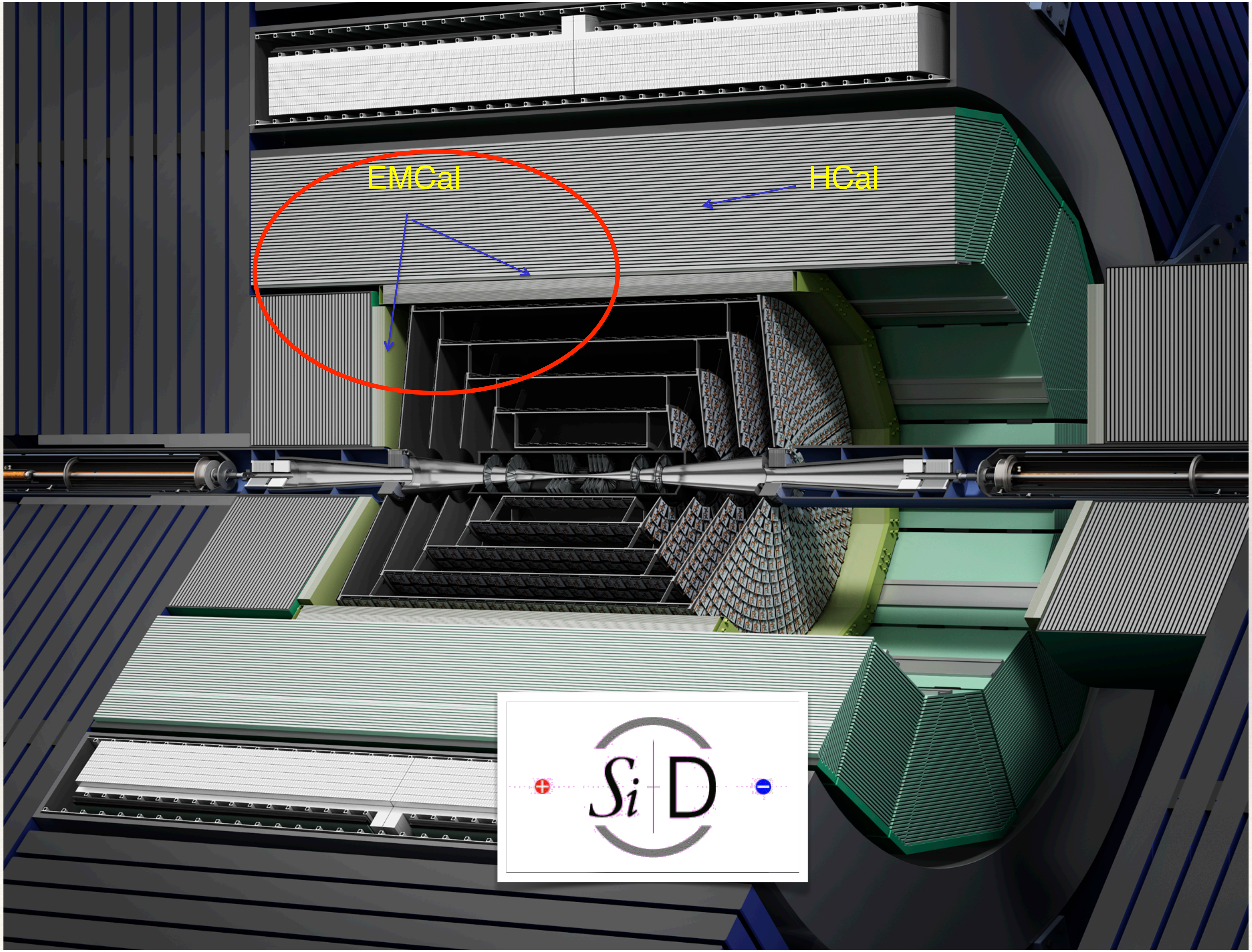


25 x 100 μm^2
ECal performance
same as
50 x 50 μm^2



SiD Tracker and the ECal

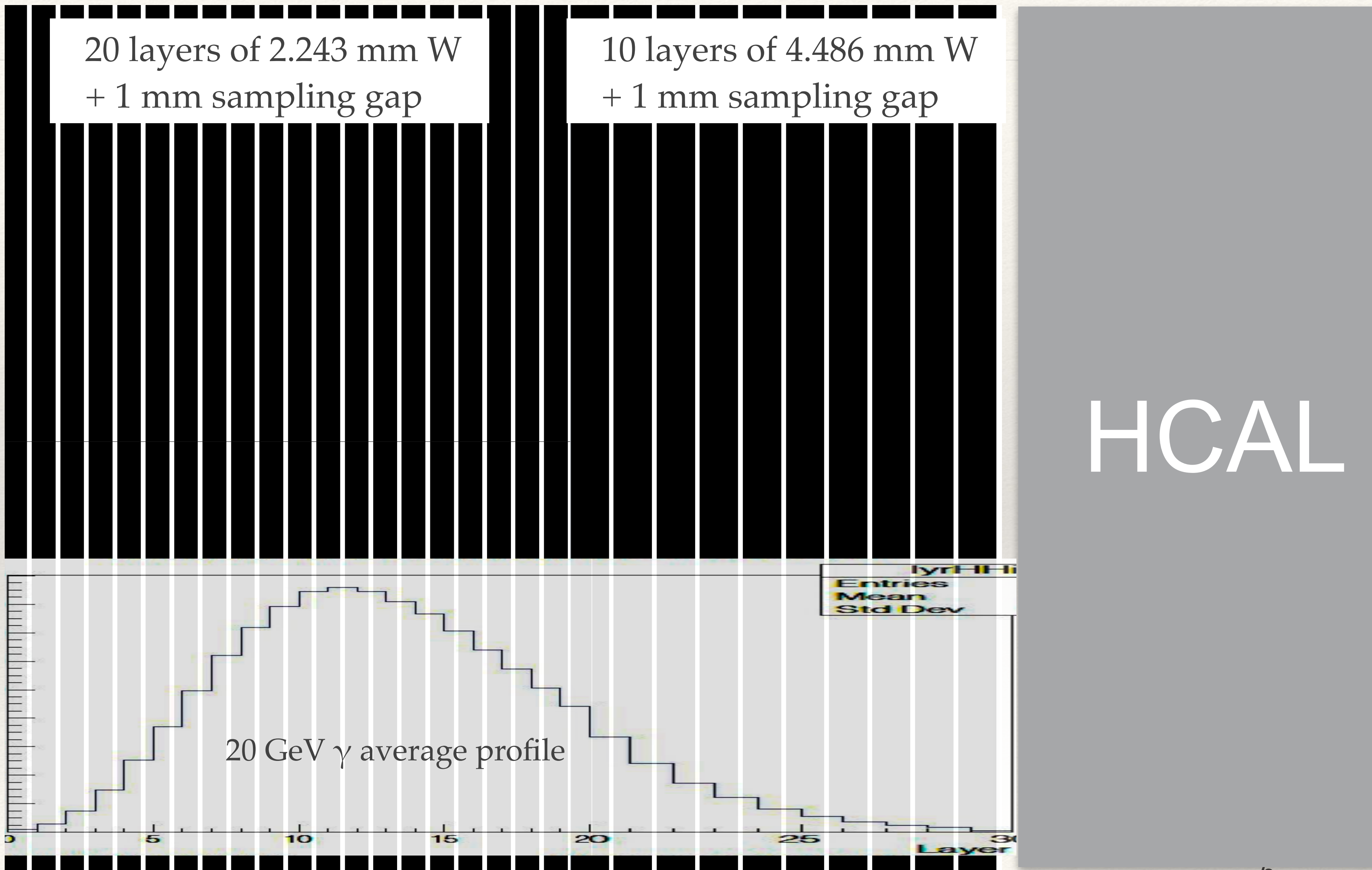
L. Rota


EMCal
HCal

Longitudinal structure of SiD ECal

Total = 27 X_O

Incident Particle



Minimize sampling gap to achieve optimal Moliere radius and shower separation

Power during integration phase

Phase:

- Avg power reduced by power-cycling … but **peak** current draw is not! current draw ~16 A
  - → significant voltage drop

Possible strategies:
- Bypass caps; EMCal flat cable distributes power; Re-distribution layer; more/thicker metal layers.

Need to investigate strategies on how to cope with shorts:

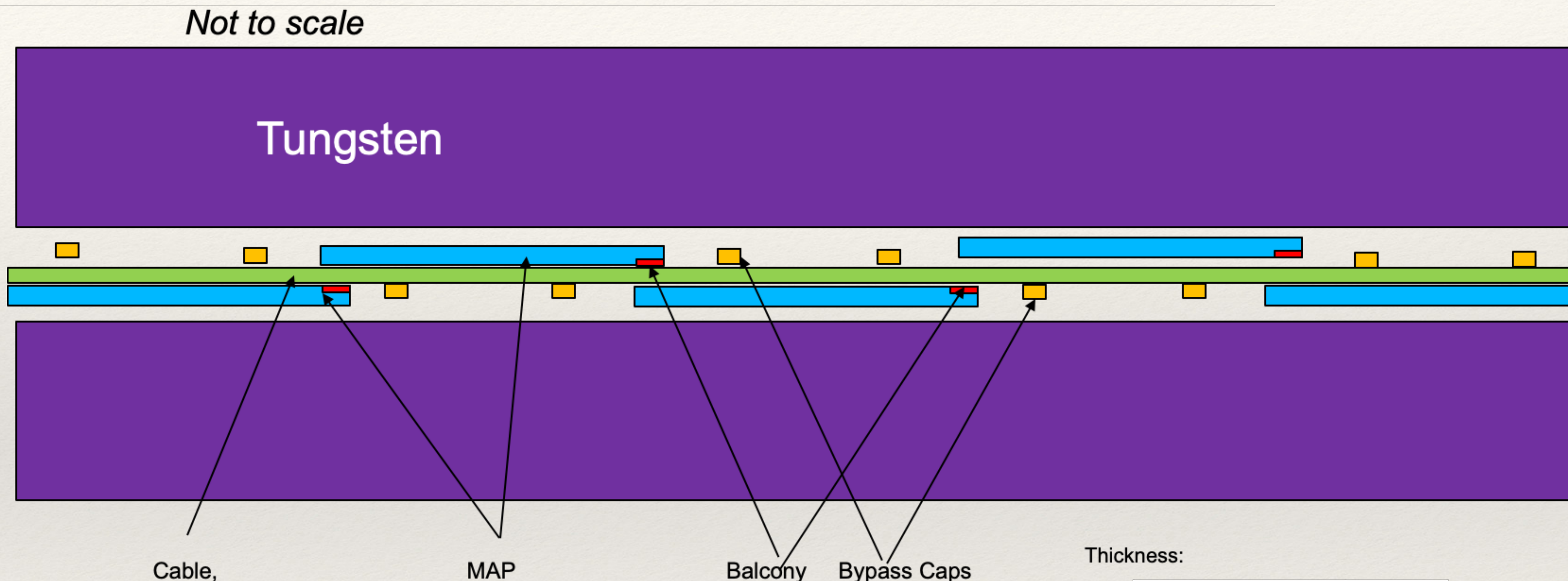
L. Rota

Power during readout phase

Asynchronous readout logic with **zero-suppression:**

- Only pixels with HIT information read out. **power ⇩**
- Remove clock → **power ⇩**

Gap Structure with MAPS



Thickness:

Middle Cable	400 μ
Top Sensor	200
Bottom Sensor	200
Bottom Cable	0
Total	800
Clearance with 1 mm gap	200

ONE CABLE IN GAP DESIGN

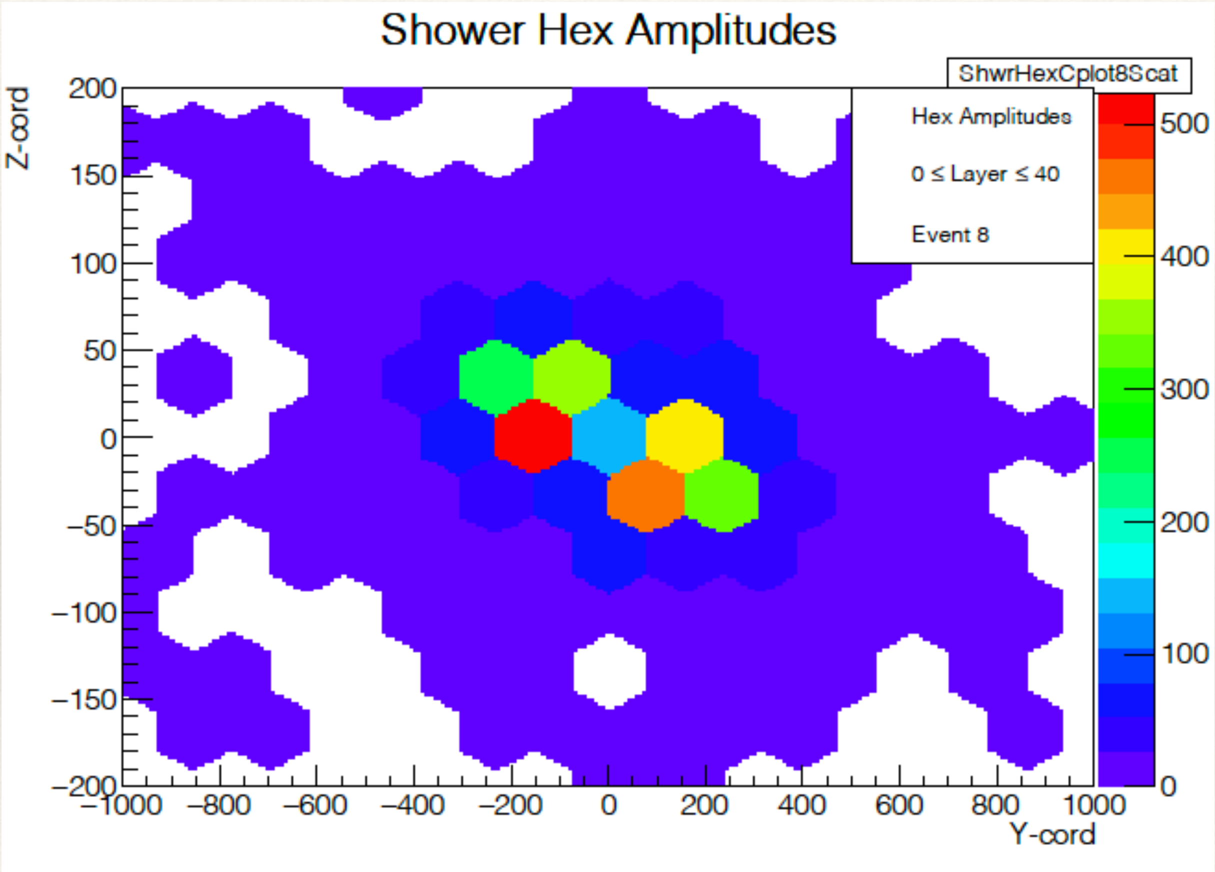
Gap structure with MAPs on one cable (or pcb). Requires bump bonding

This may well need adjustment following more cable design

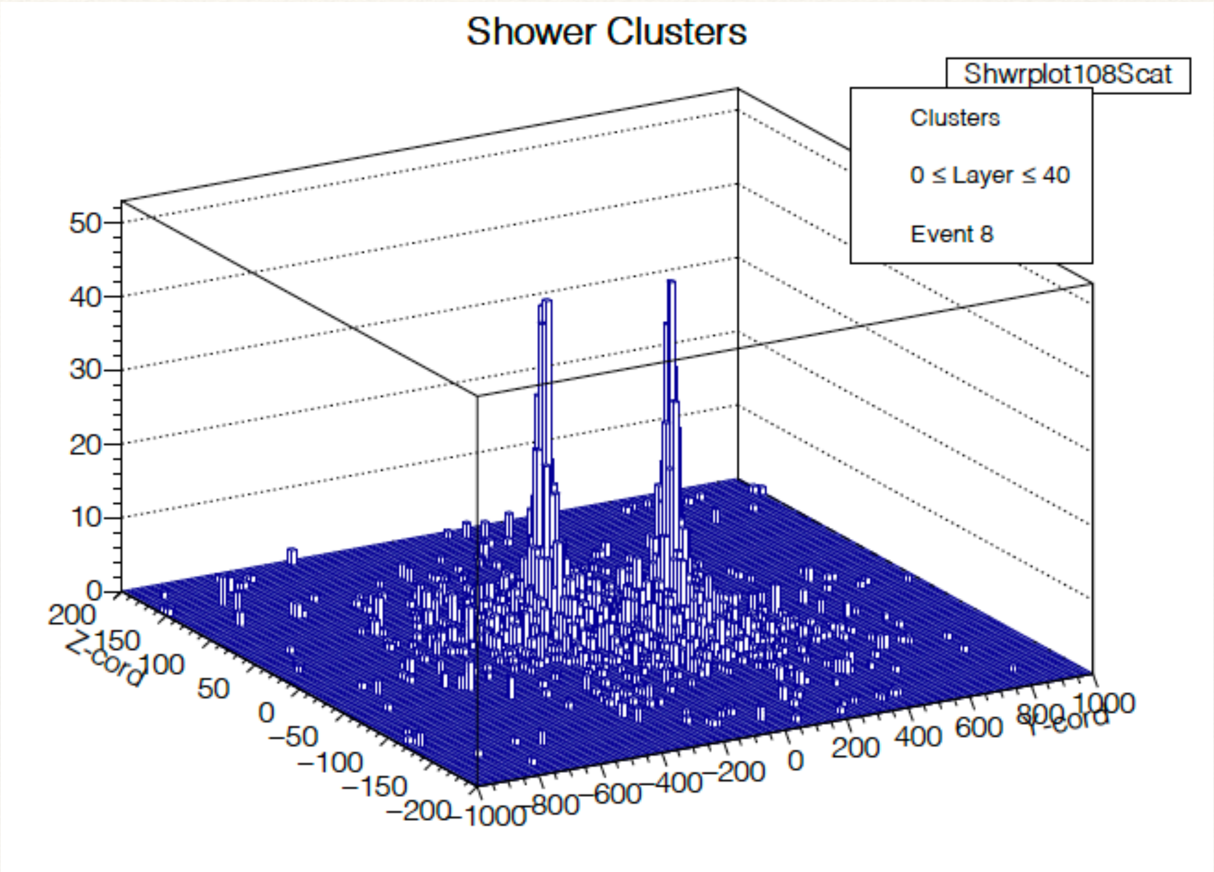
M. Breidenbach

Multi-shower of SiD MAPS compared to SiD TDR

40 GeV $\pi^0 \rightarrow$ two 20 GeV γ's



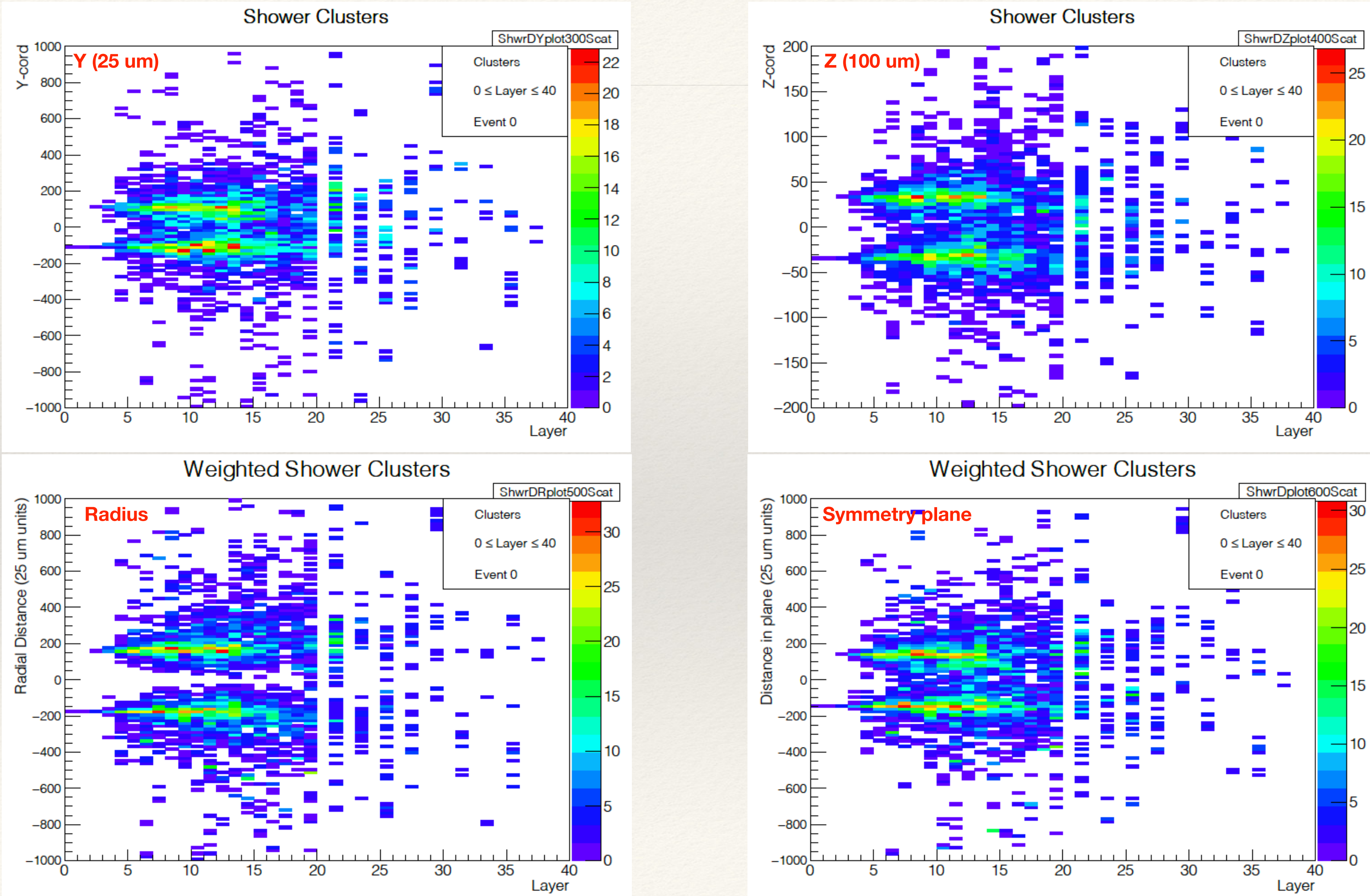
SiD TDR {arXiv:1306.6329 [physics.ins-det]}
hexagonal sensors - 13 mm² pixels



New SiD fine MAPS pixel sensors
25 μm x 100 μm pixels

40 GeV $\pi^0 \rightarrow$ two 20 GeV γ's

Vertical bin
400 um



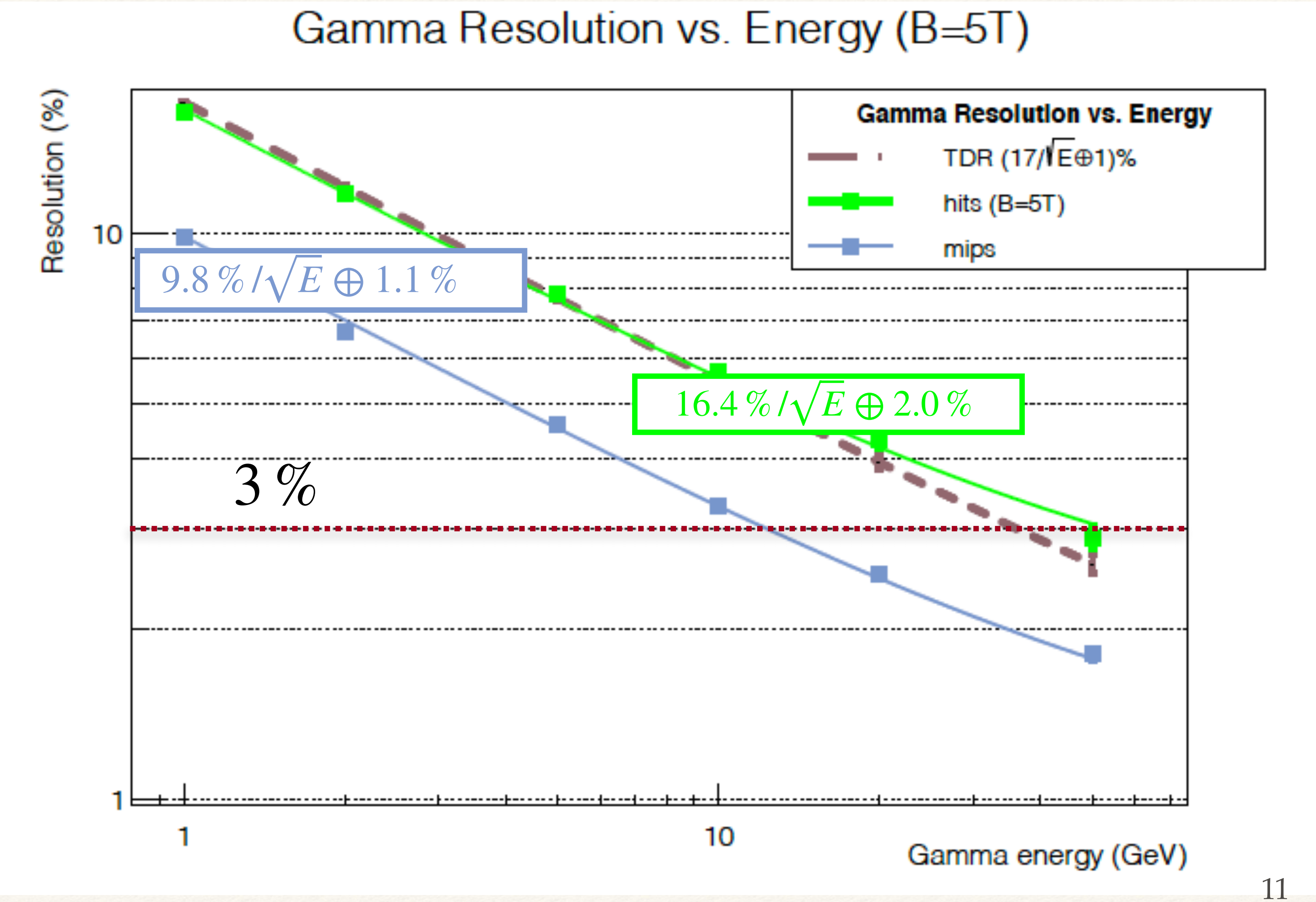
Resolution vs. Energy (hits and mips)

Resolution vs. Energy (hits and mips)

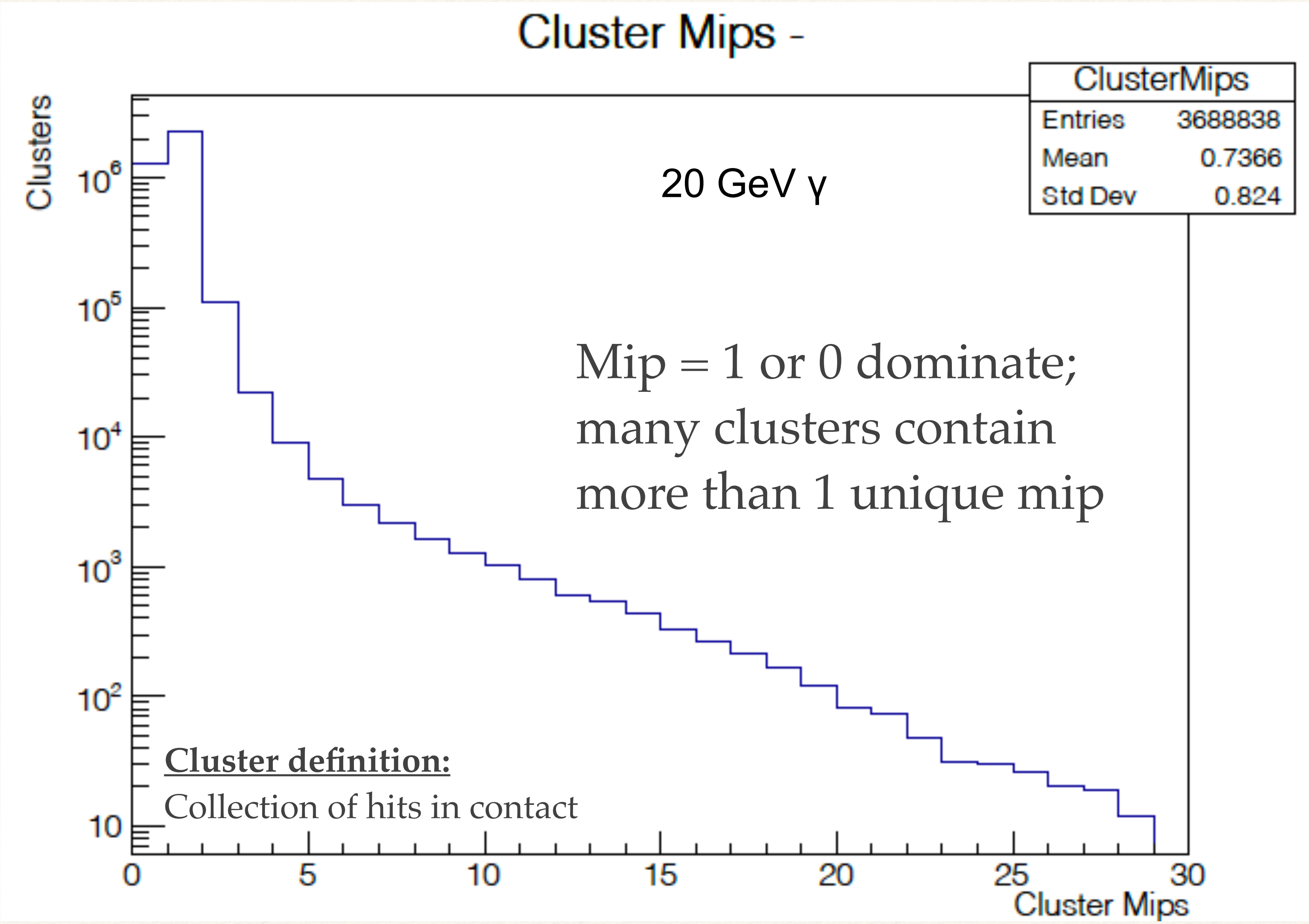
Hits are active pixels & **Mips** count each charged particle in sampling gap just once (truth).

Resolution can be improved!

TDR = arXiv:1306.6329 [physics.ins-det]

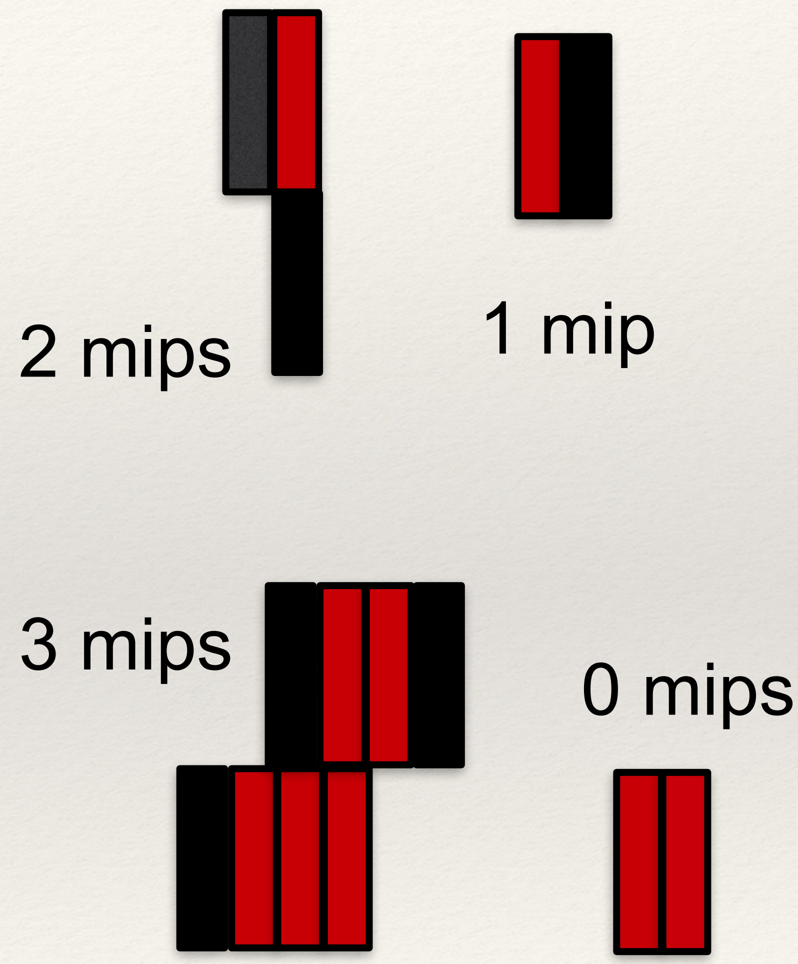


Mips per cluster

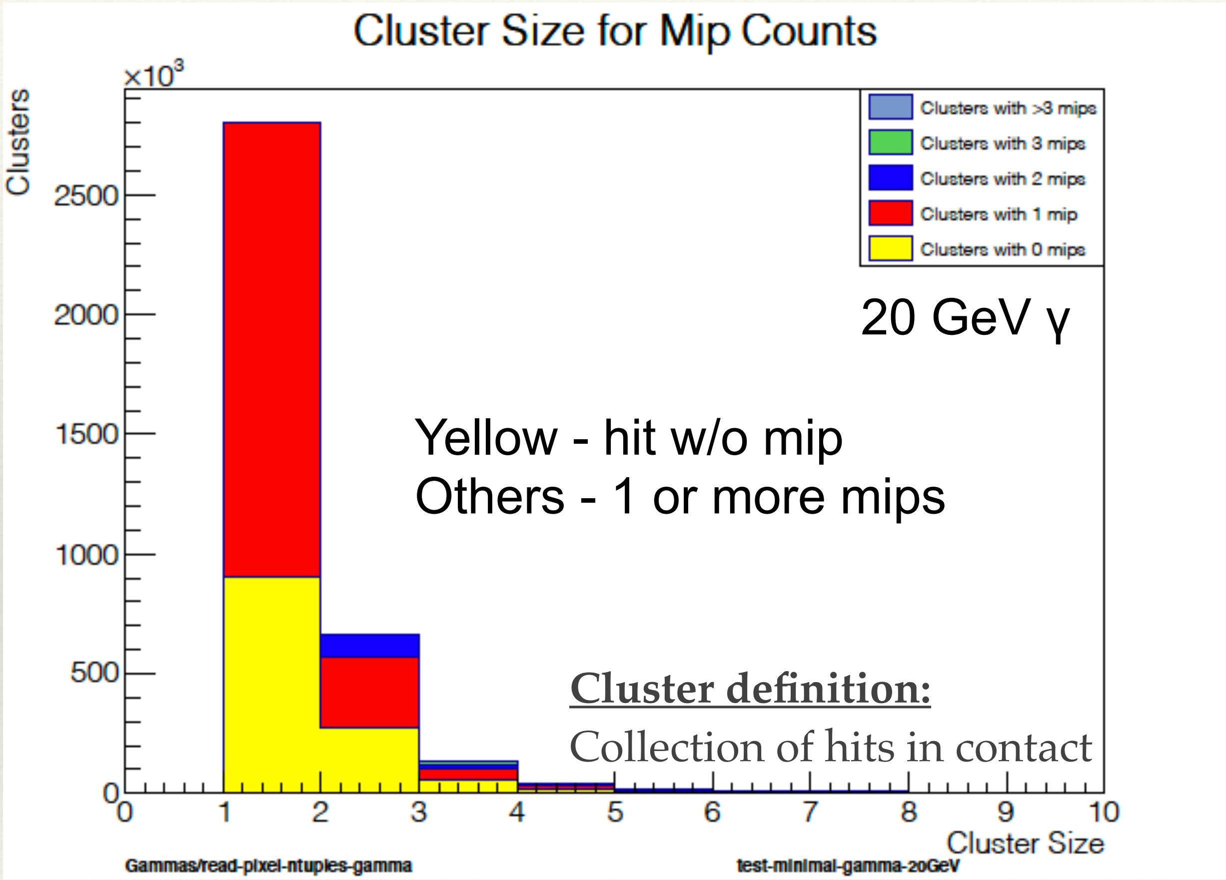


Mip = 1 or 0 dominate; many clusters contain more than 1 unique mip

Cluster definition:
Collection of hits in contact

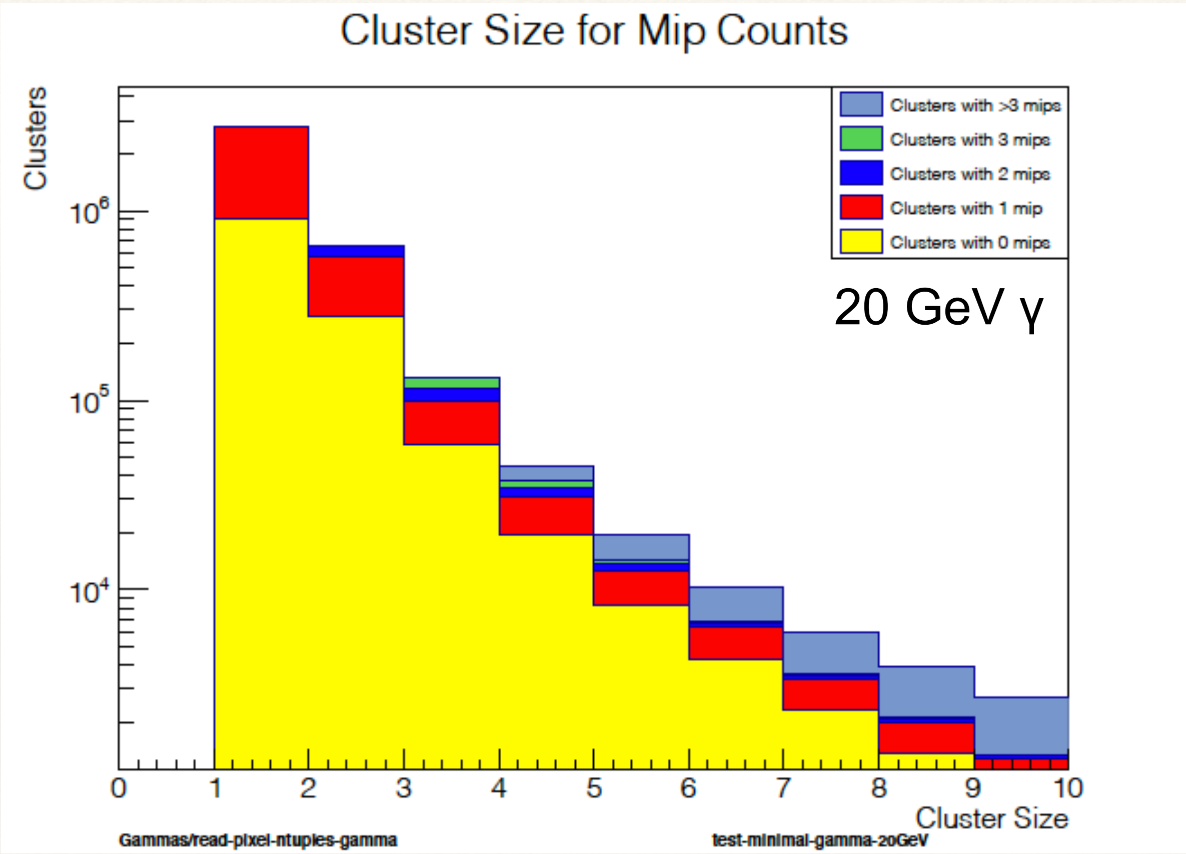


Cluster summary (20 GeV γ)



Cluster definition:

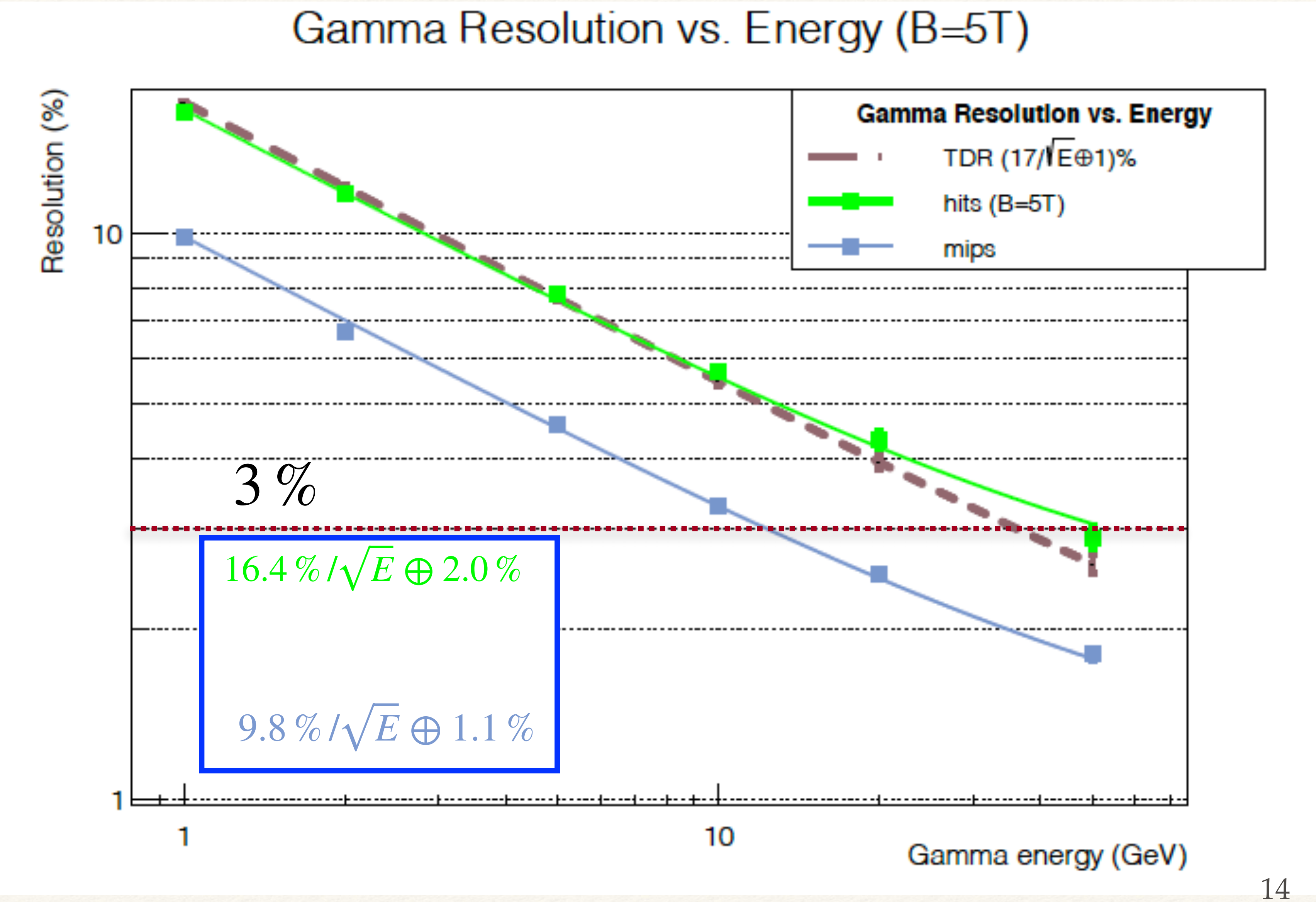
Collection of hits in contact



Cluster count is closer to mip count, reducing fluctuations from multiple hits.

Resolution vs. Energy (hits/clusters/mips)

Resolution vs. Energy
(hits and mips)



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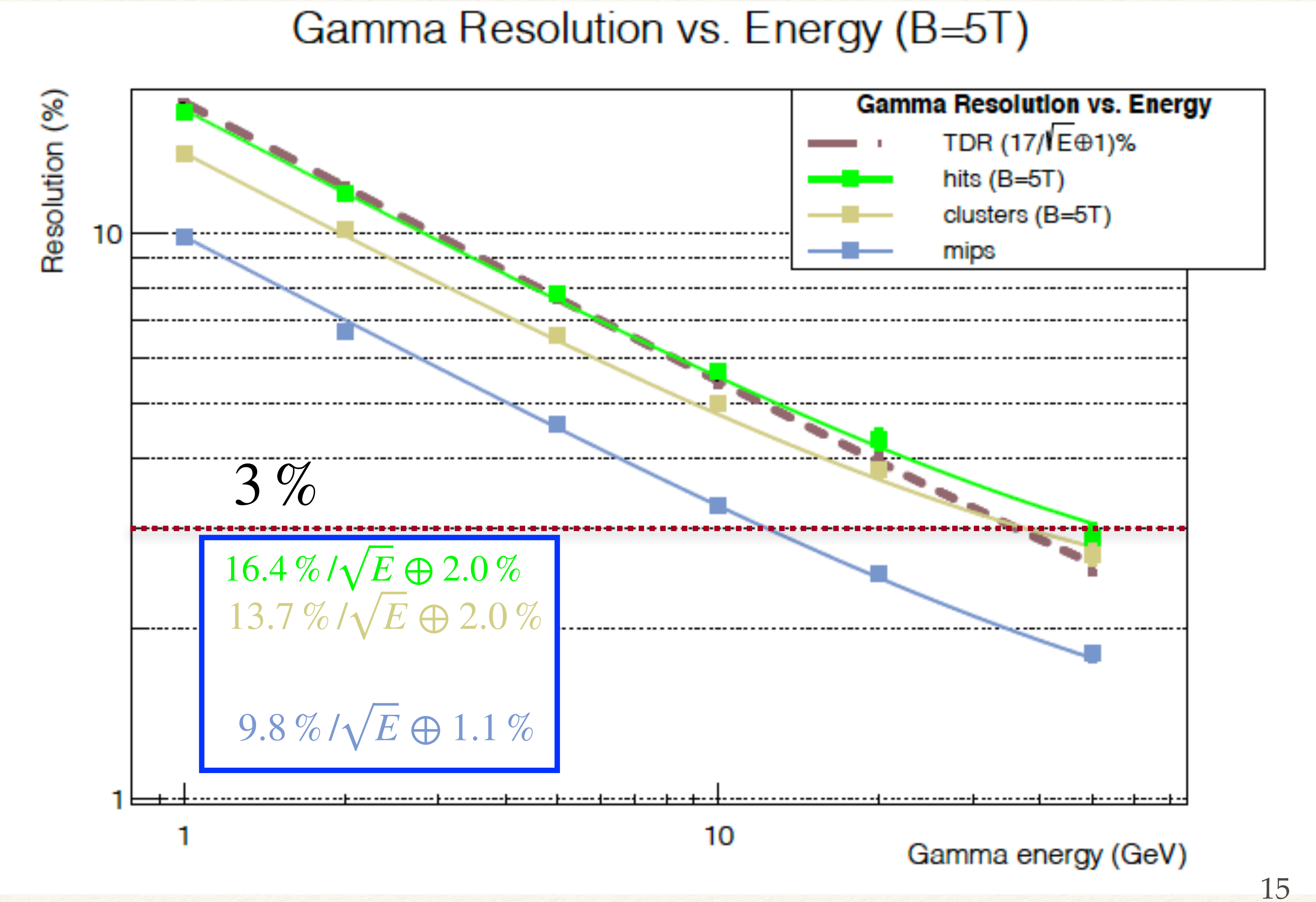
arXiv:1306.6329 [physics.ins-det]

Resolution vs. Energy (hits/clusters/mips)

Resolution vs. Energy (hits/clusters/mips)

Simple cluster performance is better than hit counting.



TDR = arXiv:1306.6329 [physics.ins-det]

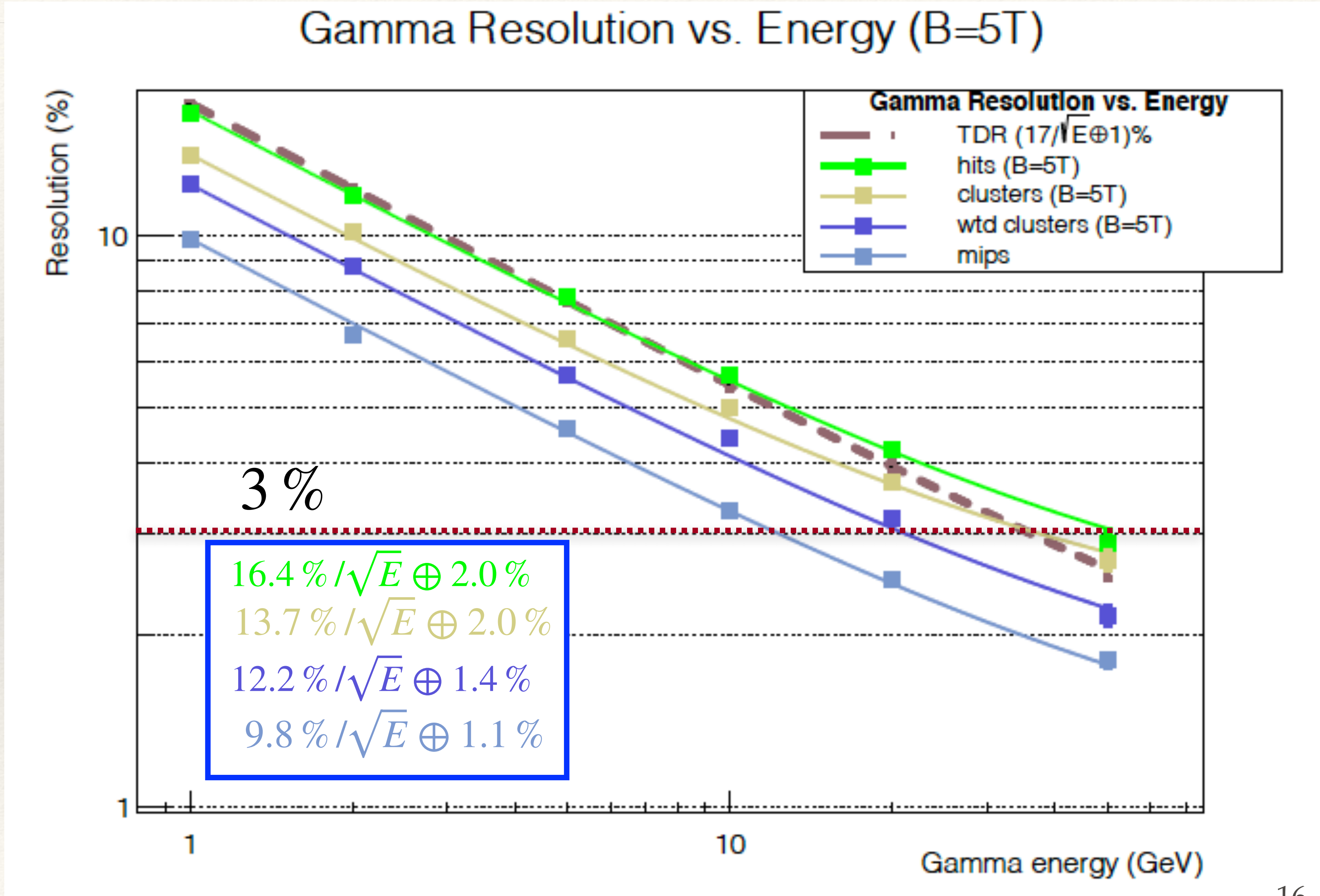
Resolution vs. Energy (hits/clusters/mips)

Resolution vs. Energy (hits/clusters/mips) & **weighted clusters.**

Simple cluster performance is better than hit counting.

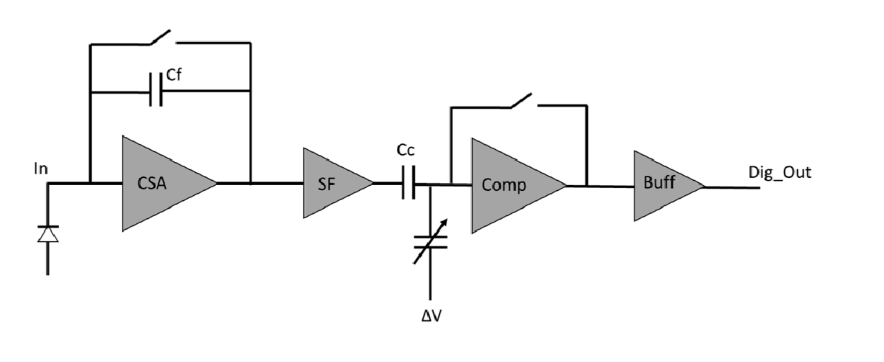
When cluster properties are taken into account with weighting, performance improves.

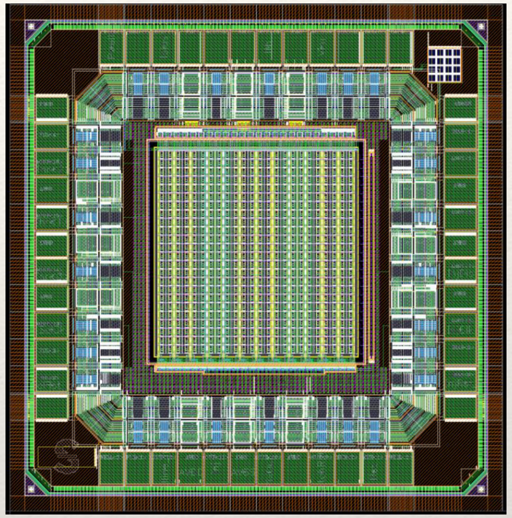
TDR = arXiv:1306.6329 [physics.ins-det]



NAPA_p1: NAnosecond Pixel for large Area sensors – Prototype 1

- Design in Tower Semiconductor 65 nm imaging technology, capitalizing on the CERN WP1.2 efforts over a decade of sensor optimization.
- The prototype design submitted with a total area 5 mm x 5 mm and a pixel of 25 µm × 25 µm, to serve as a baseline for sensor and pixel performance.





Layout of MAPS SLAC prototype for WP1.2 shared submission

Key pixel elements

- Charge Sensitive Amplifier (CSA) with a synchronous reset, which can be powered down during inactive time
- A comparator with auto-zero technique, removing the need for per-pixel threshold calibration

Summary

- MAPS has great a potential for the Higgs factory linear collider requirements
  - for ECal, as well as vertex detector and tracking.
- Simulation studies of the ECal performance demonstrates better than ILC TDR specs, achieving

$$12.2\,\%/\sqrt{E} \oplus 1.4\,\%$$

- High granularity and timing adds to the performance.
- Low sensor capacitance of 2-3 fF in Tower Semiconductor 65nm technology, improving power efficiency by at least 2 order of magnitude with respect to hybrid detectors.
- Simulations of NAPA_p1 show that it is possible to achieve a time resolution ~ 1 ns-rms with reasonably low power consumption of 115 mW / cm^2 × DutyCycle, where DutyCycle for linear colliders $< 1\%$
- NAPA-p1 characterization is underway. Results should be available soon.
- Support needed to continue this promising development effort.