IIFC C&I - Present Status

Electronics Division

BARC

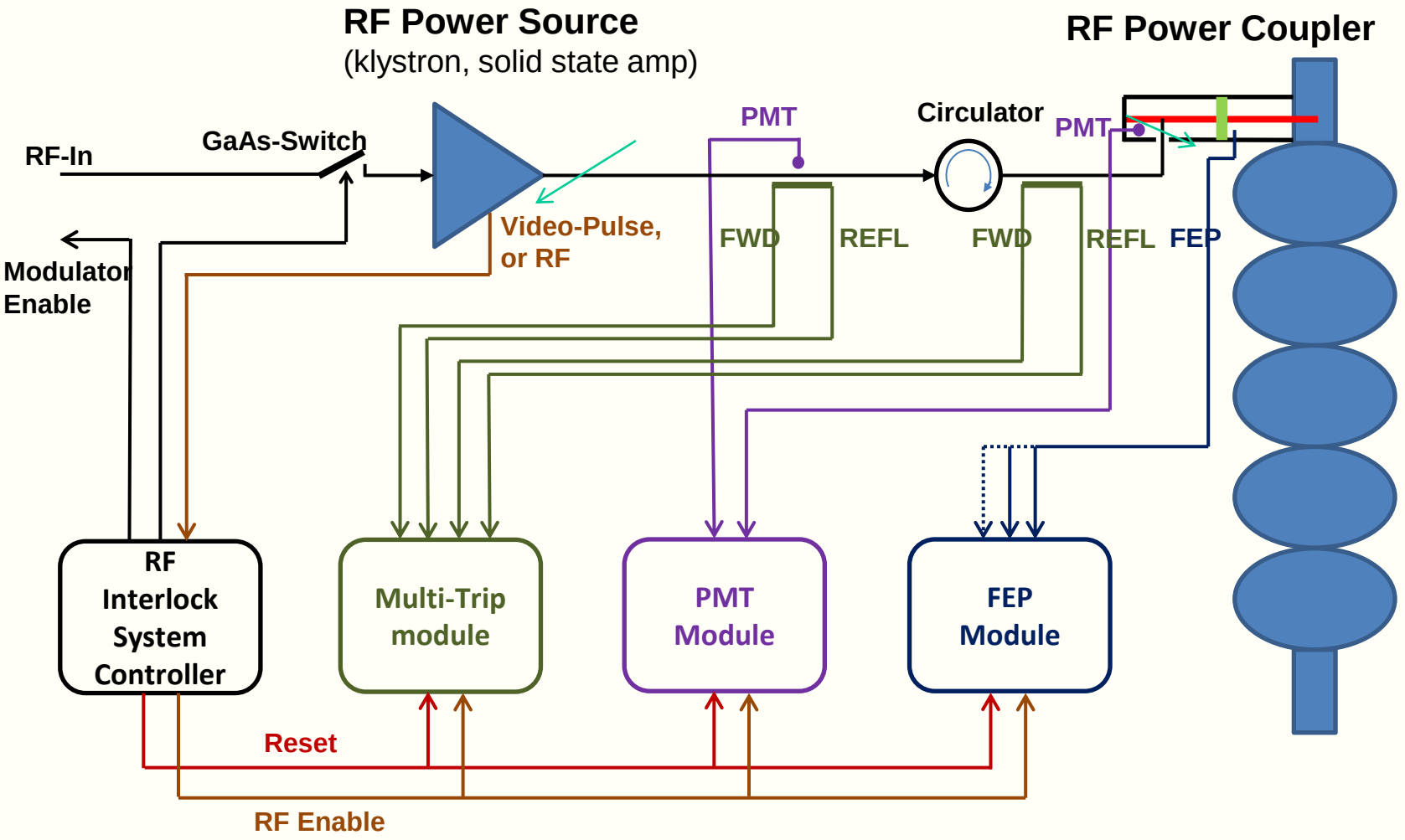
IIFC: Areas of C&I Collaboration

- **C&I for CMTS**
  - **RF Protection Interlock System**
  - **LLRF**
  - **Cryogenic Temperature Monitoring System**
  - **Software for the integrated operation of the CMTF**
- **Beam Position Monitor (BPM)**

RF Protection Interlock System

- Received schematics and other technical literature during Gopal's Visit to Fermilab during Oct -Nov 2011
- Detailed technical discussions with Peter and Manfred during their visit to BARC in April 2012
- Improvements in the existing systems were also discussed during this visit

RF Protection Interlock System



RFPI - functions

The RF Protection Interlock (RFPI) system continues to monitor the high power RF (HPRF) system during the entire power ON period and protects it by opening the fast switch at the output of LLRF within 1-2 microseconds of detection of any fault condition.

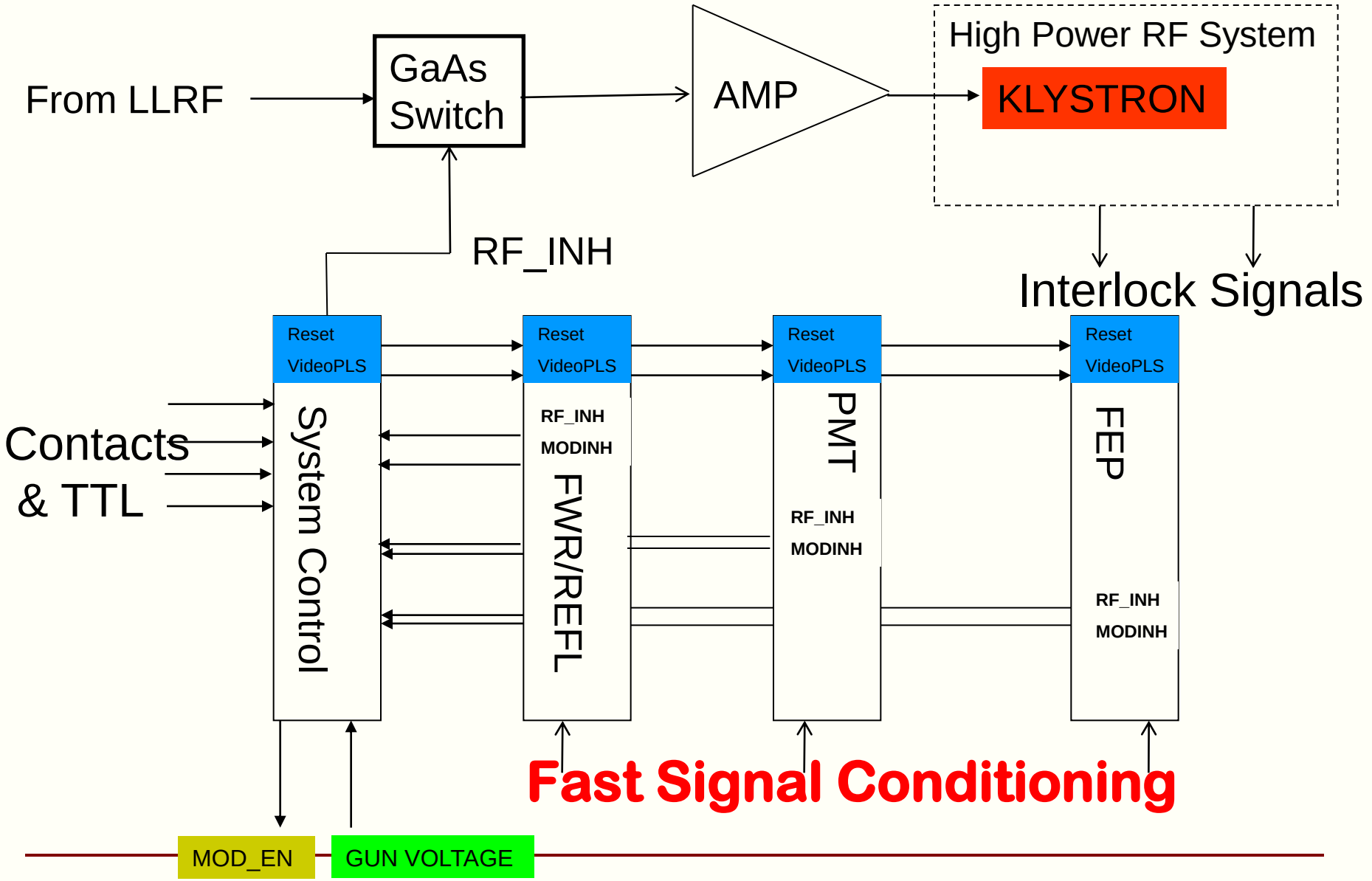
The RFPI system inhibits the modulator in case the same fault is observed on three consecutive pulses, thereby removing the DC power source to the klystron.

The existing RFPI system at Fermilab

RFPI - subsystems

- PMT Trip Module
- FEP Trip Module
- Multi-Trip Module
- Relay /Contact Module
- System Control Module
- Digitiser Module
- EPICS based IOC MVME5500 controller running VxWorks RTOS

RFPI – System Architecture



RFPI - Features

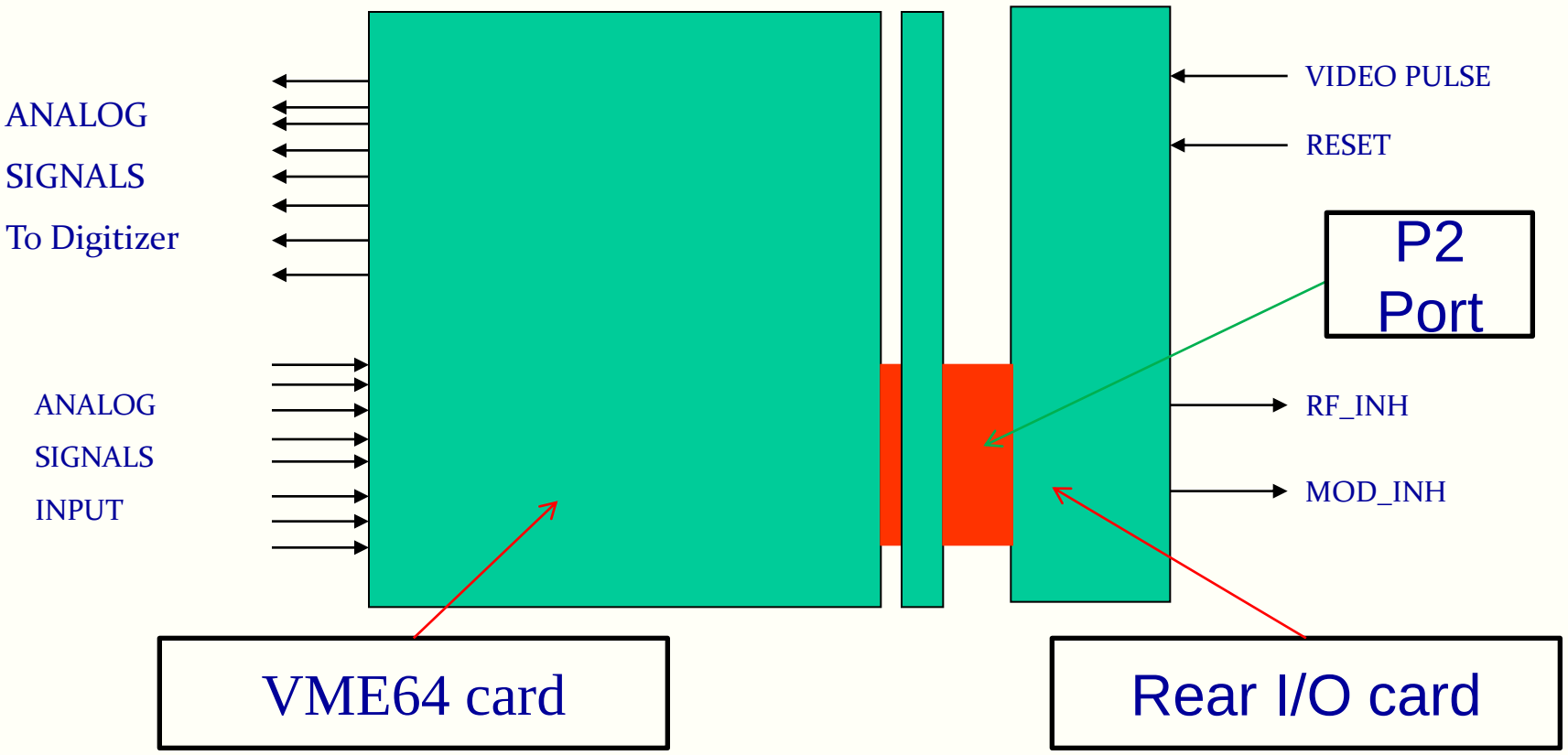
- RFPI operations are independent of VME64 bus activity.
- Programmable trip limits
- The Set point and other control actions are dependent on VME Interface. In case of a link failure, interlock operations will continue as on board FPGA stores the DAC reference Value.
- Fail-safe mode of operation is built into the design
- Fast and deterministic response
- Cable connect detection on all analog signals
- Analog signals digitized and displayed through control system.

RFPI - Low Speed signals

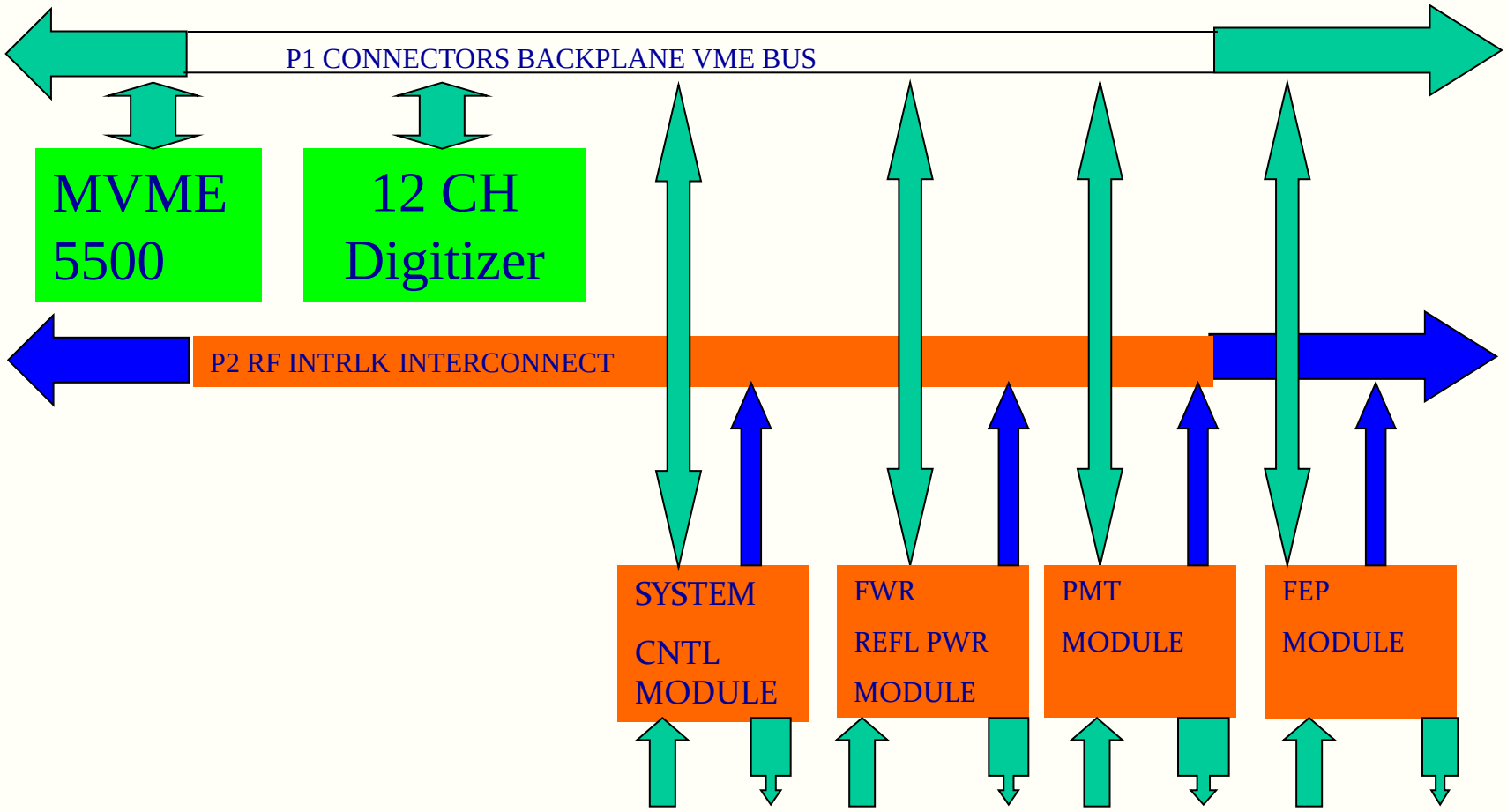
- Waveguide Pressure
- Coupler Temperature
- Coupler and Cavity Ion gauge controller
- Coupler and Cavity Vacuum pump controller
- Klystron parameters

These signals are handled through a PLC which sends a TTL active low level to the RFPI system to inhibit RF

VME64 -TRANSITION BOARD ARCHITECTURE



VME64 BACKPLANE INTERCONNECT SCHEME



New proposed RFPI system

Proposed Modifications

- **Provision of on-board digitiser- Eight channels of 14bit, 10-80MHz ADC and 64 MWord DDR2 RAM on each board will eliminate the need of a separate digitiser card and allow capture of longer duration events.**
- **Remote update of FPGA via VME Bus**
- **VME64X slave interface: Full feature VME64X slave interface supporting multiple interrupts, DMA, block transfer**
- **Modifications in analog sections-**
  - **FEP Trip Module: use of higher supply voltage JFET amplifier thereby eliminating DC/DC convertor stage.**
  - **PMT Trip Module: Dark current detection stage is used only for cable connect confirmation. Can it be removed if a reliable cable sense mechanism is developed?**
- **No of input channels to be increased to sixteen in Relay /Contact Module**

Proposed Modifications cont.

- **Mezzanine board approach-**
  - **Common VME64X carrier Board: One carrier board for all modules, handling VME64X interface and digital logic common to all cards.**
  - **Analog section unique to each module can be on Mezzanine board**
  - **The challenge here is accommodating RF connectors on Mezzanine card facia and shielding within one slot width of card.**
  - **Feasibility of integrating Relay/ contact module with System Control Module to be studied.**

- **Mechanical arrangement for cable sense logic: The mechanical arrangement for cable connect detection logic to be improved for more reliable operation.**

Proposed Modifications Cont.

- **VME64X /VXS: All the boards will be VME64X compliant. The FPGA selection and board layout will be done keeping in VXS requirement, allowing VXS interface to be added in future.**
- **General purpose analog signal conditioning modules and low speed ADC are required for eliminating the PLCs.**
- **Eliminating interconnect cables among module: Open collector logic based FRC cable interconnect on the rear I/O card for additional functionality. Can be used for adding more signals to the Interlock.**

  Eliminates cable and expensive LEMO connector?

Progress so far

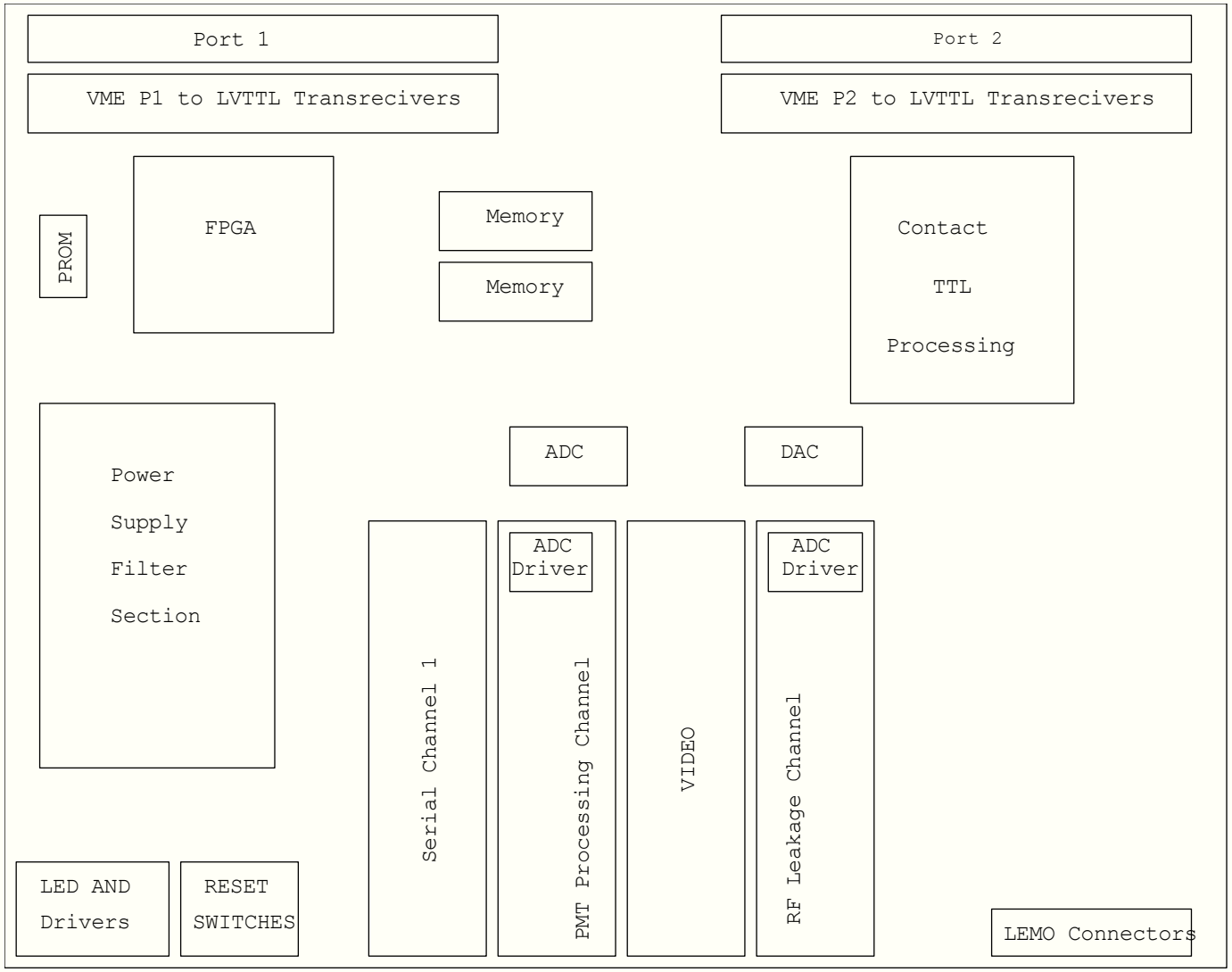
Peter has advised to take up the development of new System Control board with all the features of the existing board with additional PMT channel, ADC and memory, in the first phase.

- **A brief design report showing block diagram of the same was submitted to Fermi Lab and was approved by them.**
- **The detailed schematics of the new system control board is in final stage of preparation. The same will be sent to Fermilab for review before fabrication.**
- **The mechanical arrangement of cable connect detection assembly has been finalised.**
- **Development of Multi-trip board based on the mezzanine board approach has been initiated.**

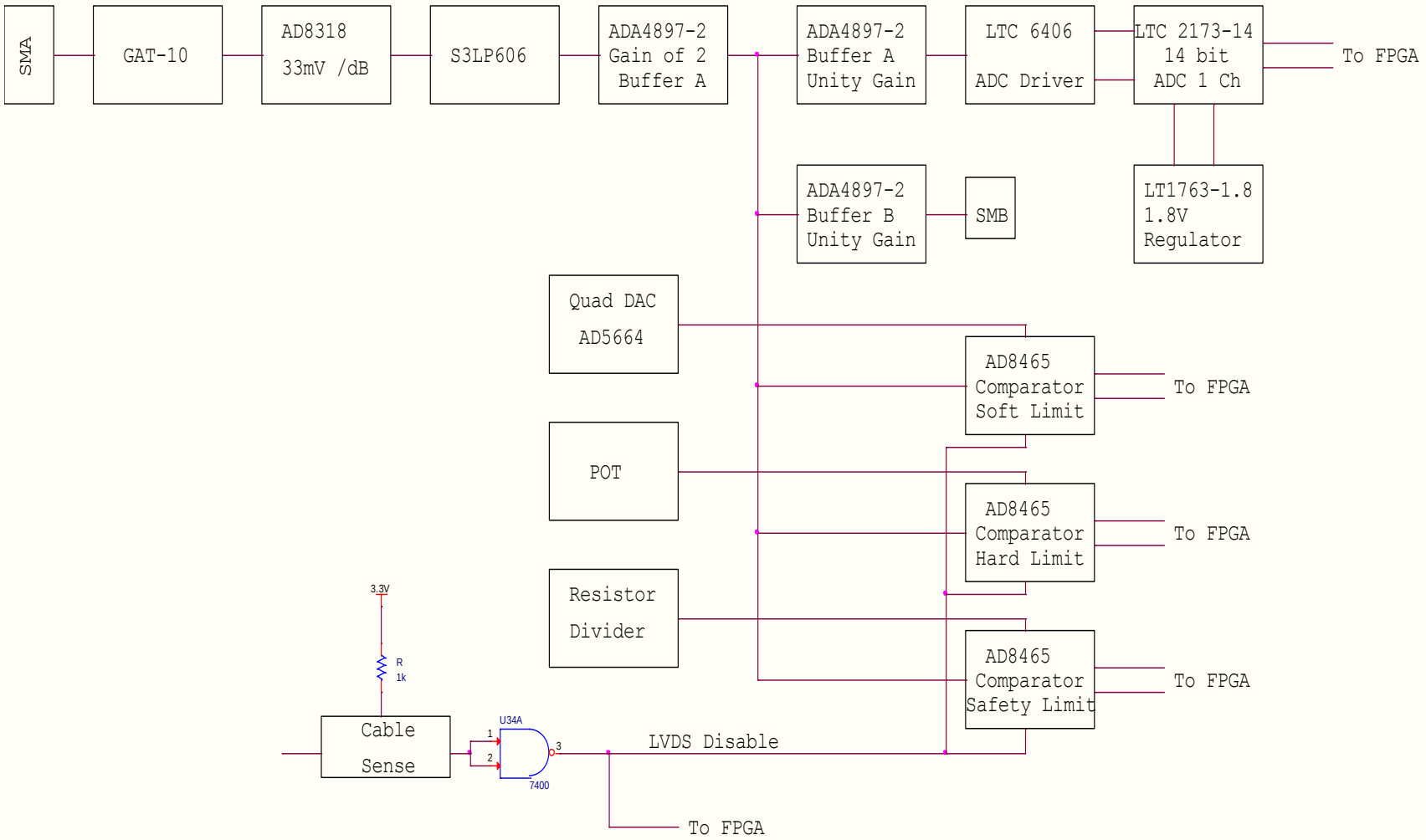
On Board Digitizer

- LTC 2173-14 four channel 14 bit 80MSPS ADC
- ADC provides 2 LVDS output per channel
- LTC6406 single ended to differential driver
- FPGA de-serializes the ADC Data
- 128 MB of DDR2 memory Interfaced to FPGA
- 8M word per channel: stores 100mS @ full speed
- Pre trigger and post trigger information is available
- The pre trigger to post trigger ratio can be adjusted using software

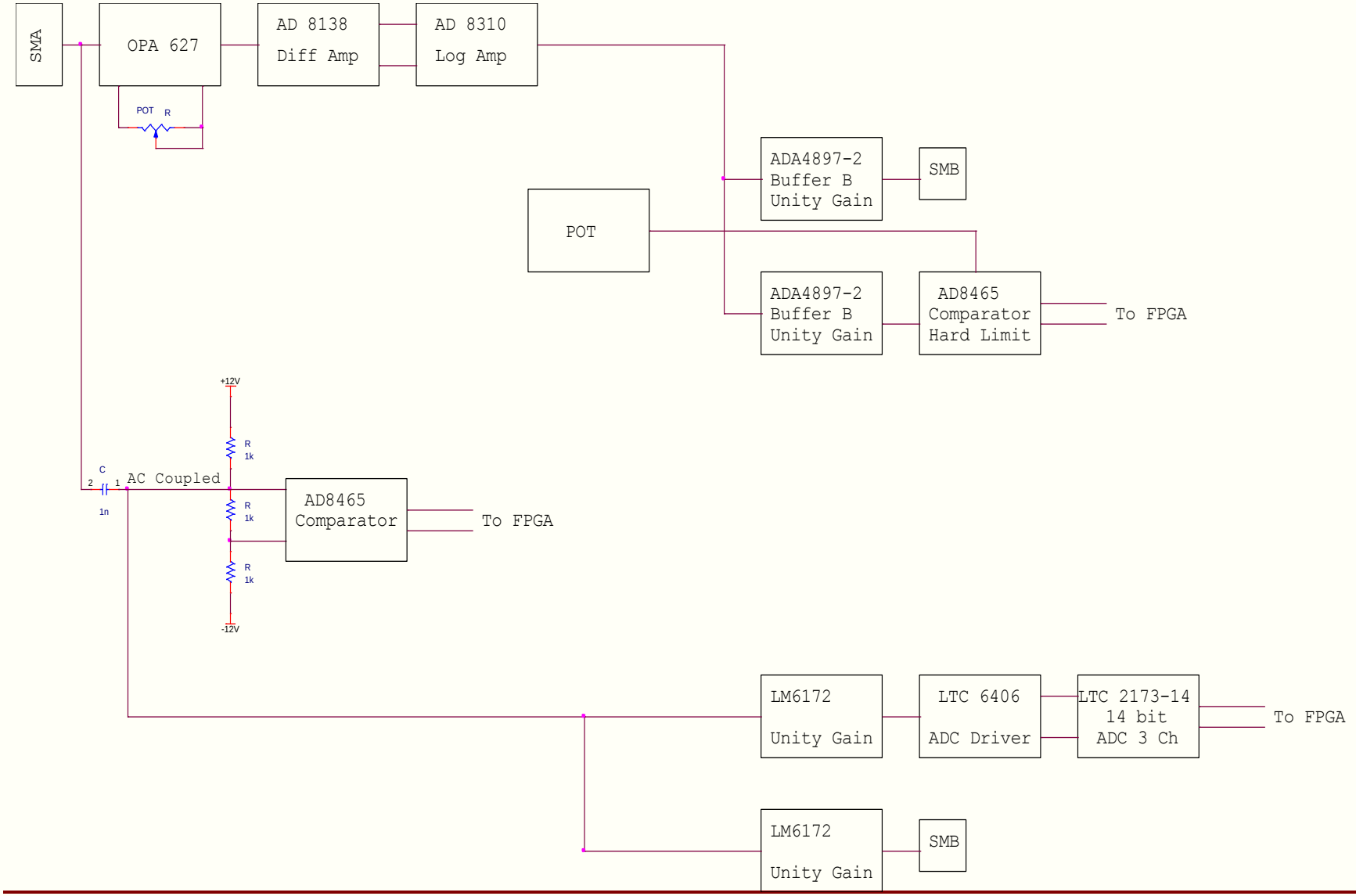
Modified System Control Board



RF leakage channel



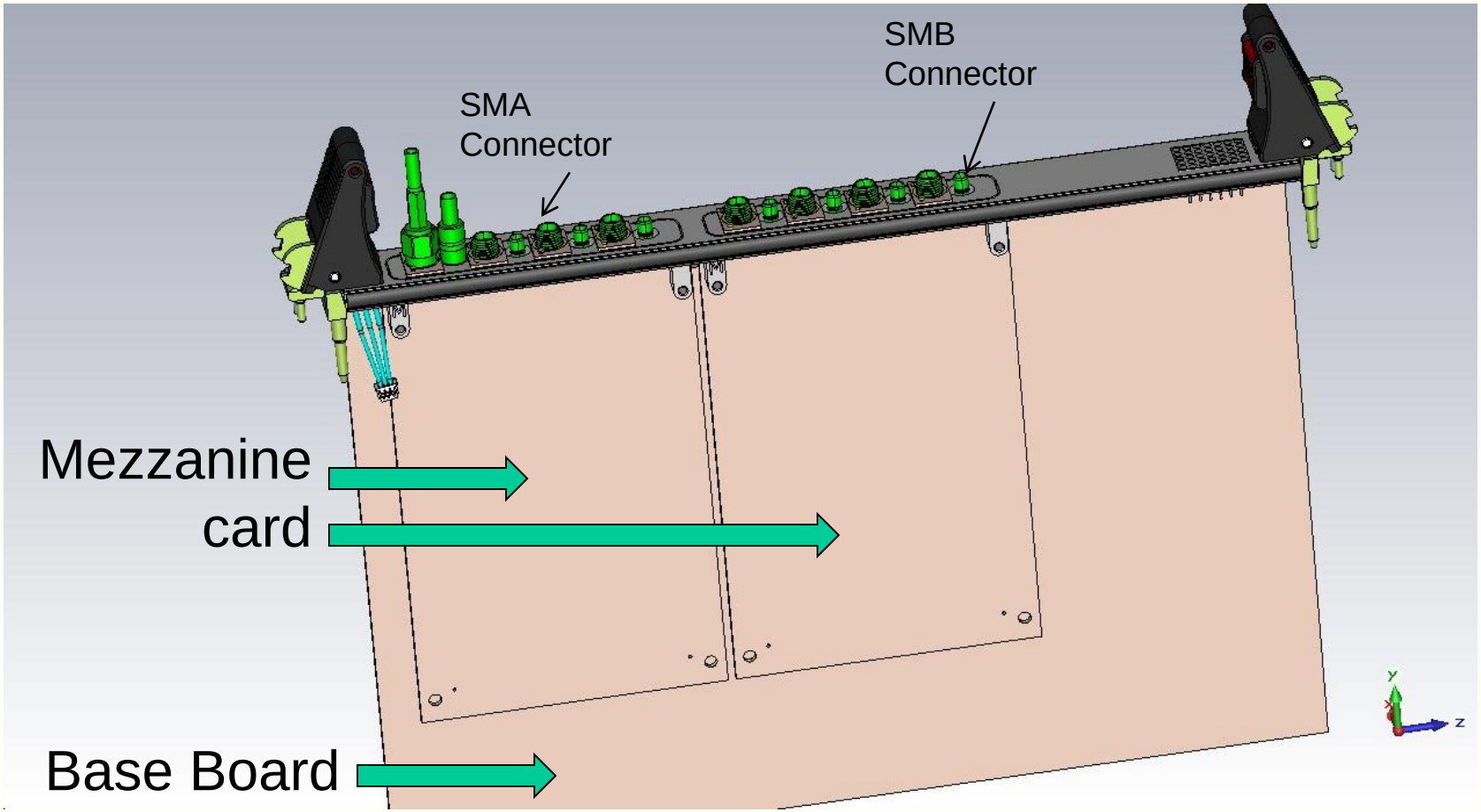
PMT output processing channel



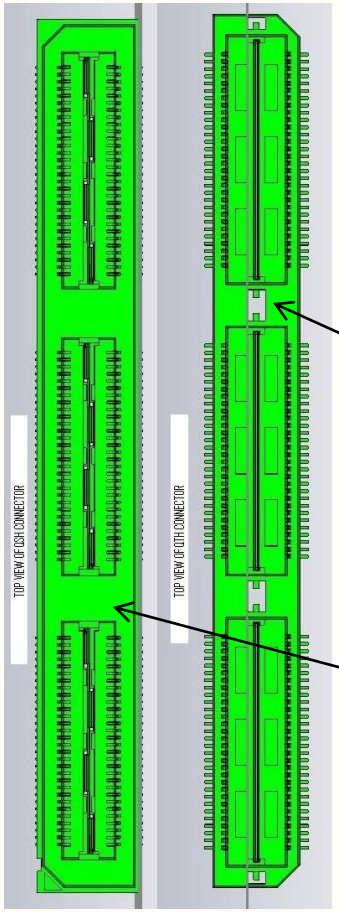
Why Mezzanine card?

- The VME board is common, once proven, it can be used with all mezzanine modules.
- Migration to VXS or cPCI platform is very easy, we need to develop new base board only.
- Mix and match approach can improve board utilization – cost saving
- Maintenance is easy, module level replacement at site
- ADC can be tailored as per application requirements as it is located on Mezzanine card
- Noise mitigation more convenient

Mechanical details of Mezzanine card

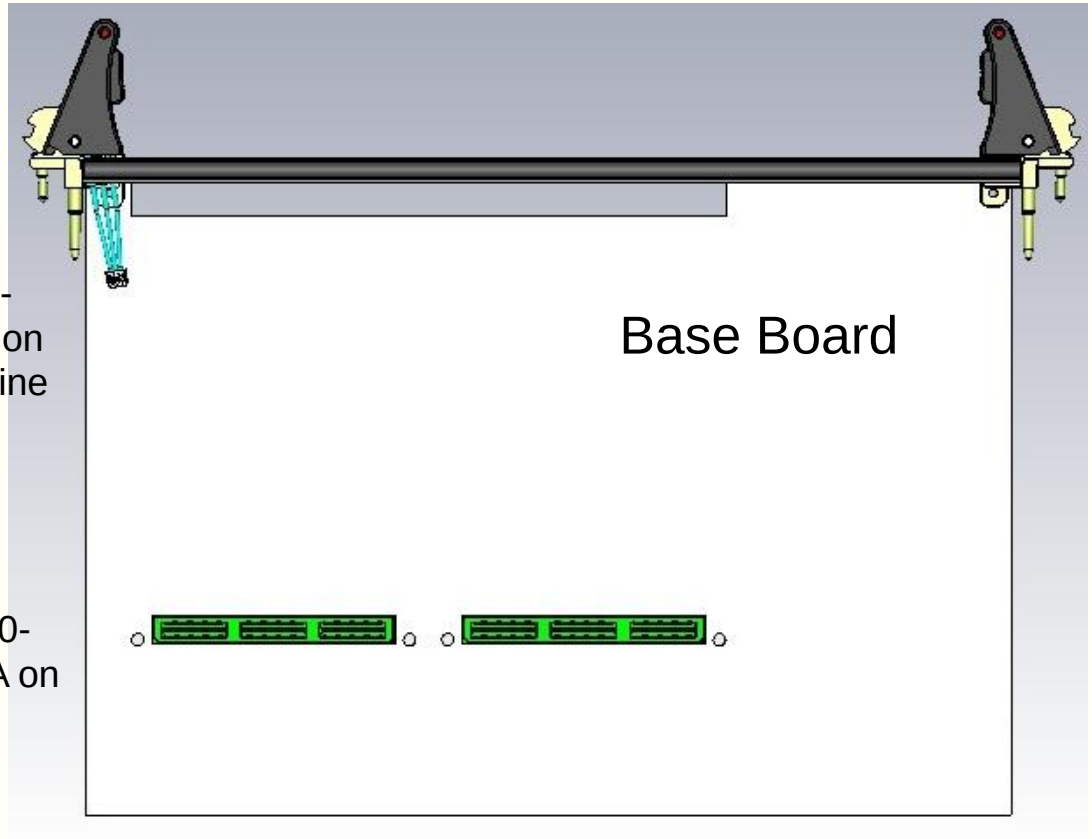


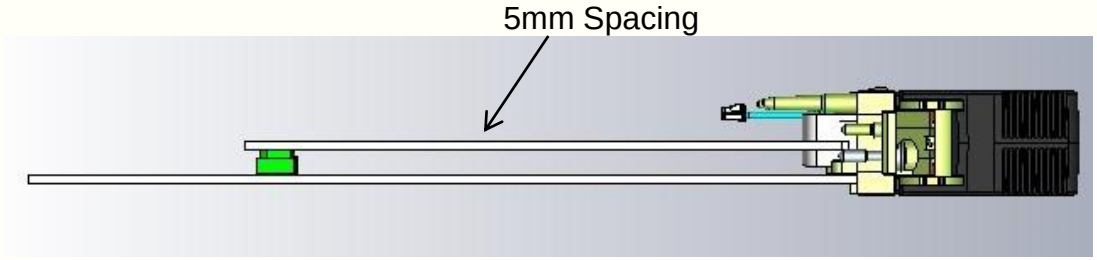
Various views of Mezzanine card



QTH-90-01-LDA on mezzanine board

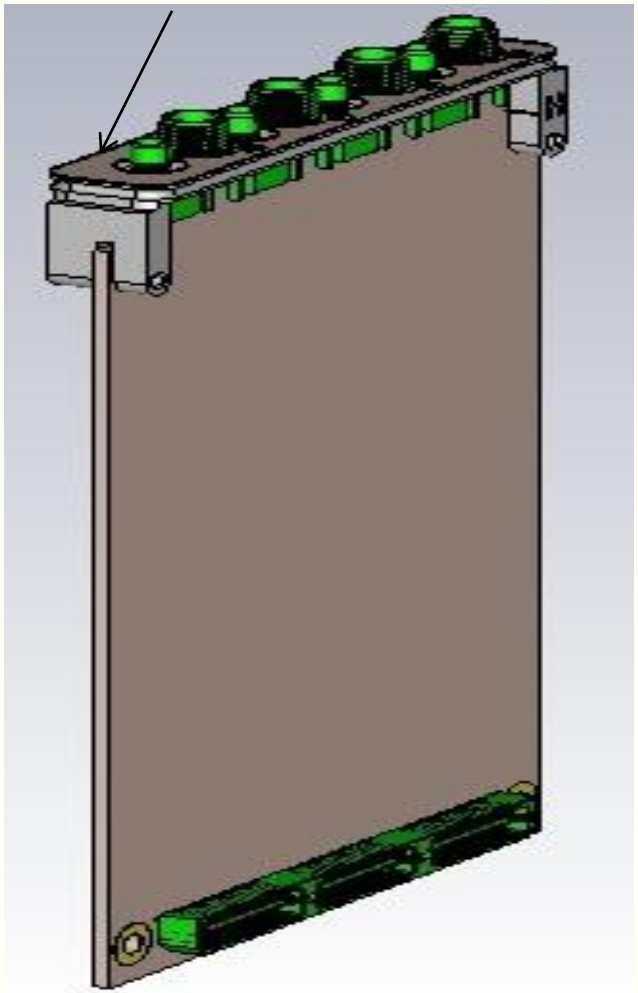
QSH-90-01-LDA on Base Board

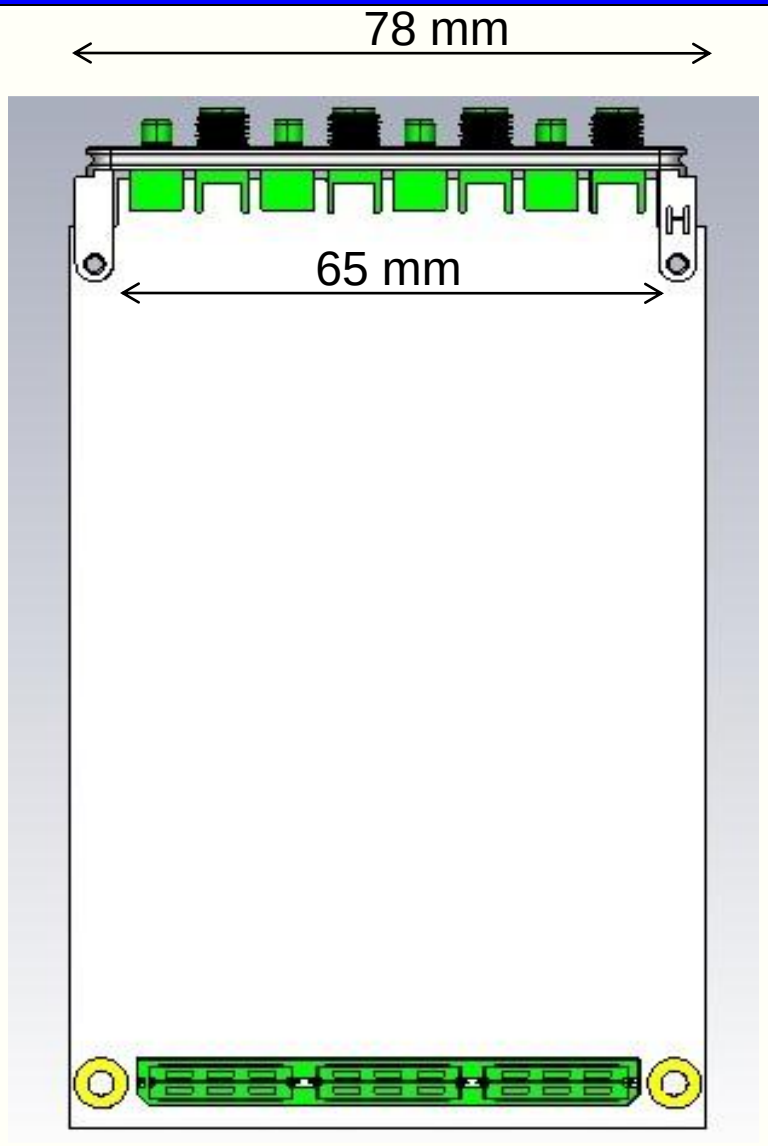




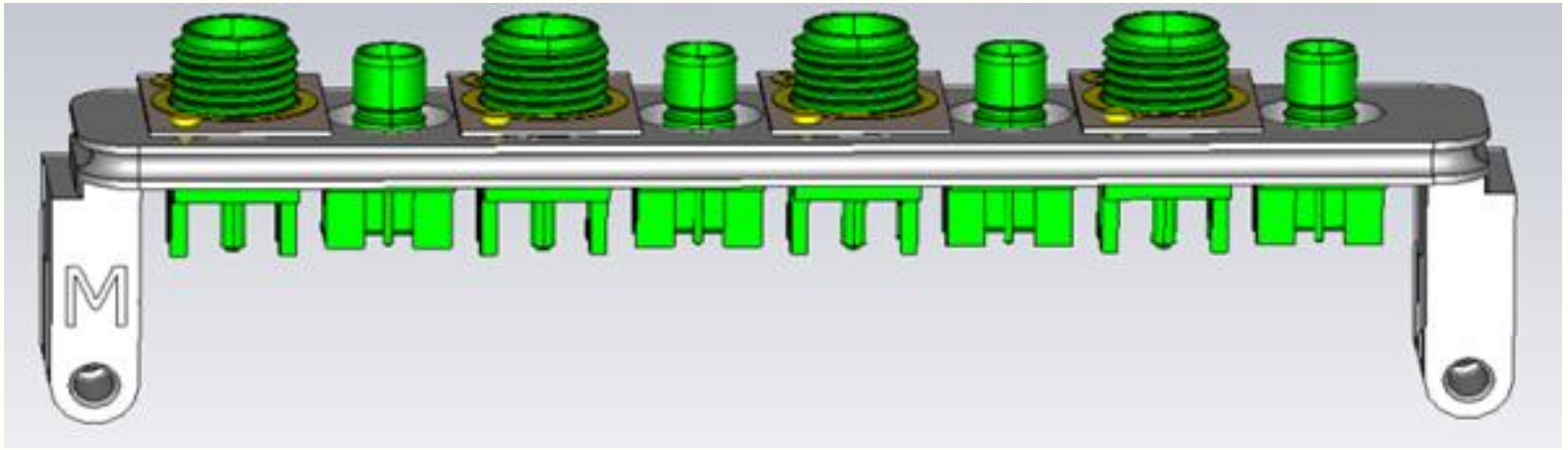
Mezzanine card

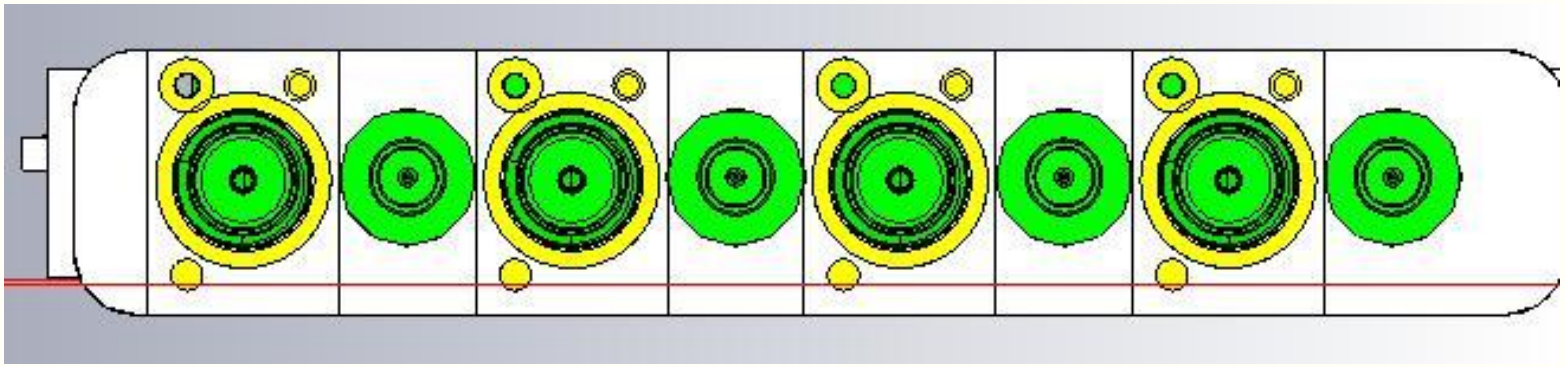
Standard PMC bezel



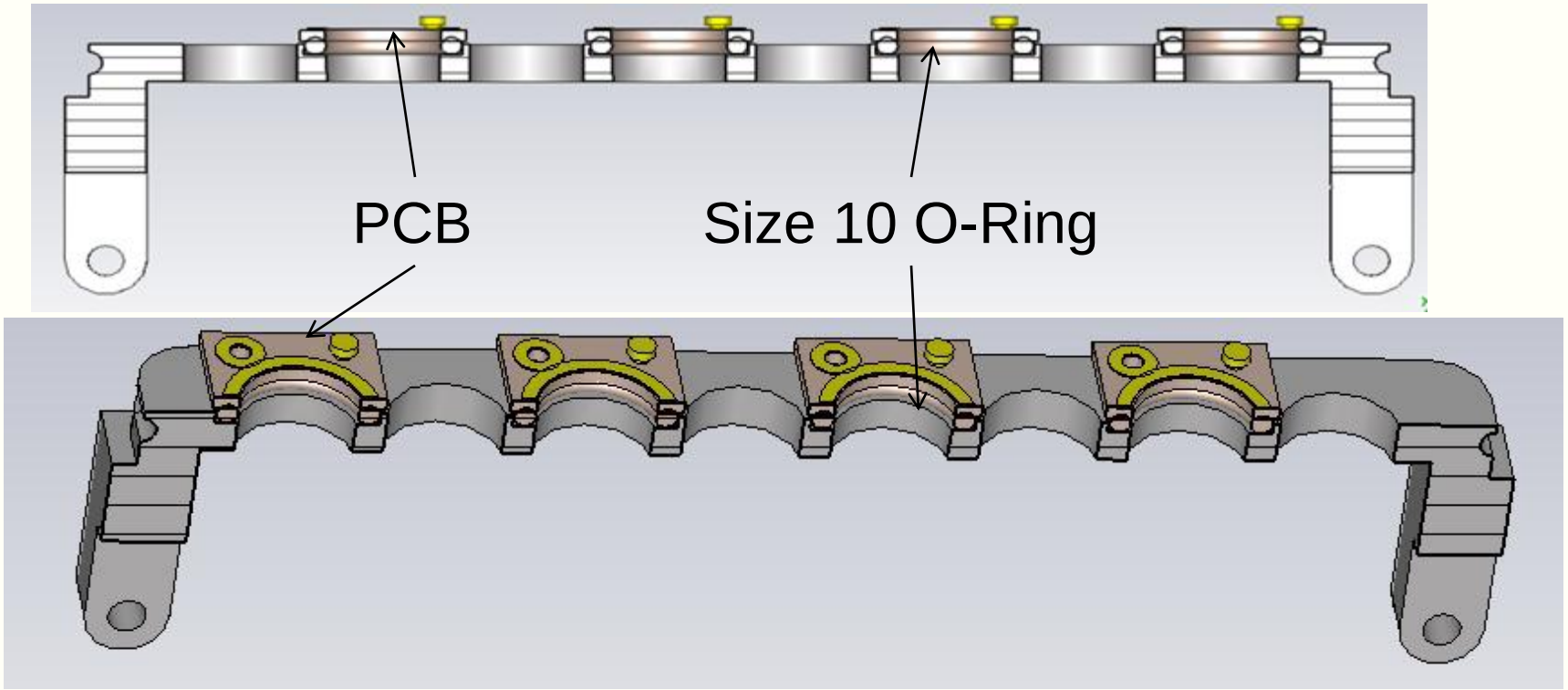


Cable Sense Assembly

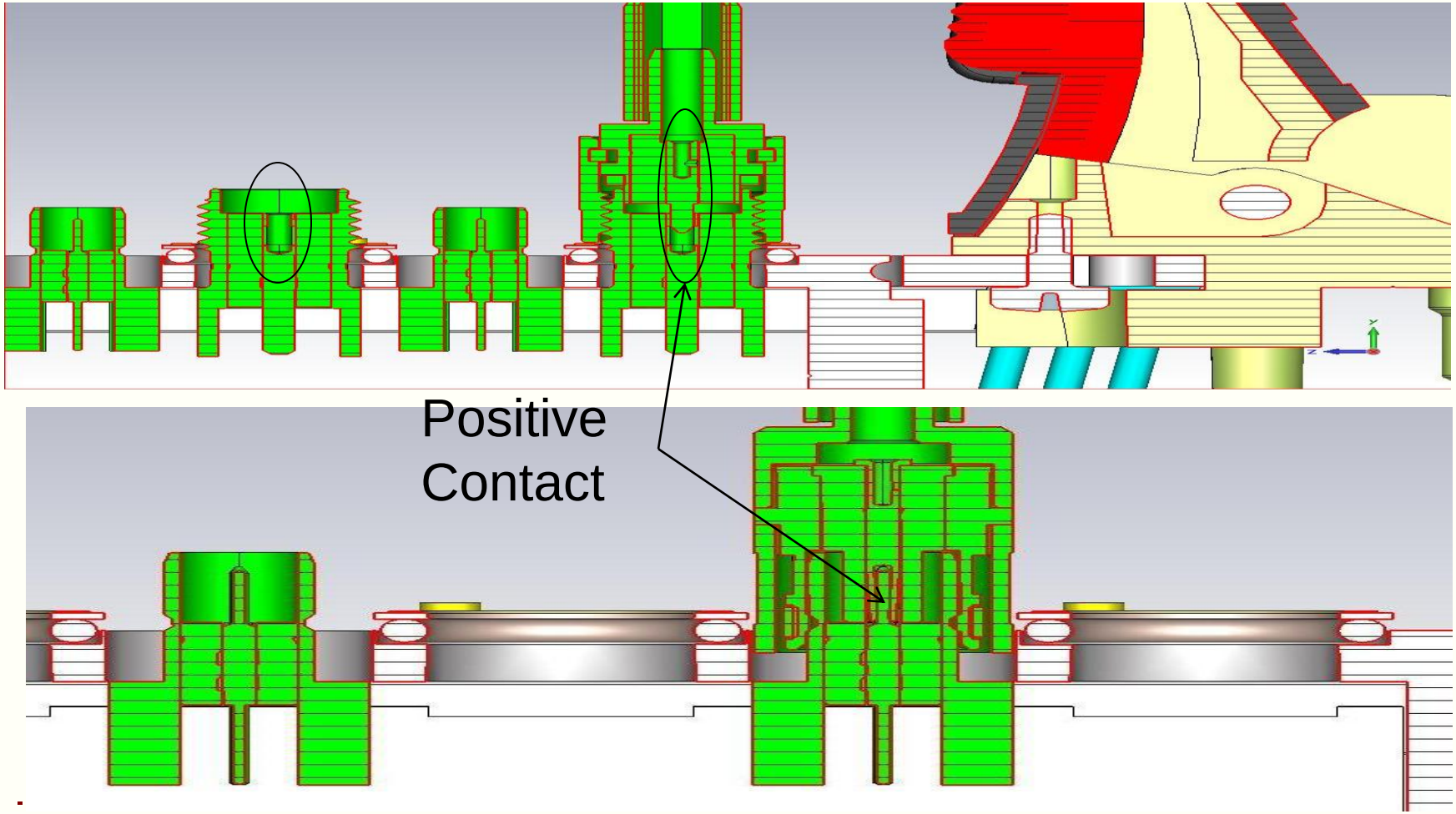




Cross-section view of Bezel



SMA and SMB Connections



LLRF STATUS

- Fermilab has provided technical documentation of the existing boards
- Current LLRF digital board is size 6U based on VXI bus
- Some of the major specifications such as number of ADC/DAC channels, FPGA and DSP to be used have been tentatively formulated
- Fermilab has suggested to upgrade to a new bus interface
- During Paresh's visit various bus standards such as VME64, VXS, VXI4.0, PXI, CPCI, ATCA, MTCA (xTCA), MTCA.4 (also called as MTCA for Physics) have been discussed.
- It is expected that the Fermilab will soon finalize the bus standard to be adopted for the next generation of LLRF
- Based on the discussions with Fermilab design of the digital board has been initiated
- BARC suggests the use of CPCI bus for LLRF system. Fermilab may kindly comment.

Fermilab

पऊवि DAE

THANK YOU

Specififations of Samtec Connector

- QSH-90-01-LDA connector for VME64X board socket
- QTH-90-01-LDA for Mezzanine card
- The connector pins are rated for 125VAC, having 1A current capacity
- The contact resistance is 30mOhms
- The connector is rated for 8GHz 3dB bandwidth
- The connector is optimised for 100 Ohms signal
- The connector has a total of 180 pins out of which 157 pins are signal pins
- The Connector has 3 ground strips in the centre for improved shielding
- The Mezzanine card provides all the VME power supplies

Electrical Details of Mezzanine card

- 32 LVDS pairs
- 2 LVDS Clock pairs
- 20 LVTTL lines
- 5 LVTTL Clock lines
- 24 LVTTL I/O lines
- 4 Single Ended Analog lines
- 8 Differential Analog lines
- 3 SPI channels with 8 slaves each
- 1 I2C/SMB channel
- 1 JTAG channel
- 1 PSNTn for card insertion detection
- The LVDS and TTL lines have 100 Ohms /50Ohms Controlled Impedance