ECON-T and ECON-D ASICs

J. Babbar, G.Bergamin, D.Ceresa, A. Campbell, D.Coko, G.Cummings, C.Gingu, N.Kharwadkar, P.Klabbers, S.Kulis, J.Hirschauer, J.Hoff, M.Lupi, D.Noonan, P.Rubinov, S.Scarfi', A.Shenai, C.Mantilla Suarez, C.Syal, X.Wang, J.Wilson

HGCAL Rentree

5 Sep 2023

Outline

- Reminder of high-level plan
- ECON-D-P1 “Extra Metal” issue
  - Plan for providing 40 MHz ECON-D-P1 in Fall 2023.
- ECON-D-P1 testing/characterization status and known issues
- ECON-T2 design status
- ECON engineering run endgame

Reminder: ECON project high-level plan

ECON-T-P1 :

- Full functionality prototype submitted in June 2021
- Comprehensive chip testing since Dec 2021 reveals no major issues

ECON-T2 :

- Fix few verilog bugs identified in ECON-T-P1 testing
- Adopt final architecture from ECON-D

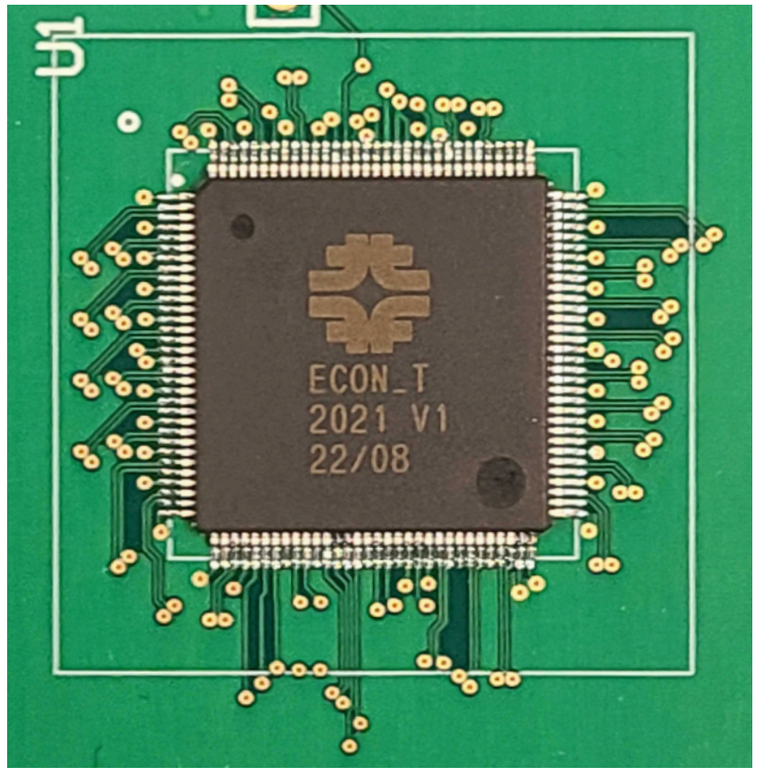
ECON-D-P1 :

- Full functionality prototype submitted on 01-Mar-2023
- Received 26-June-2023
- Functionality, radiation, and system testing ongoing

ECON-T + ECON-D joint engineering run (~80% of production):

- Current plan to submit for fabrication on 01-Nov-2023
- Major decision point: whether to update ECON-D design to fix known low-impact issues?

ECON-T-P1



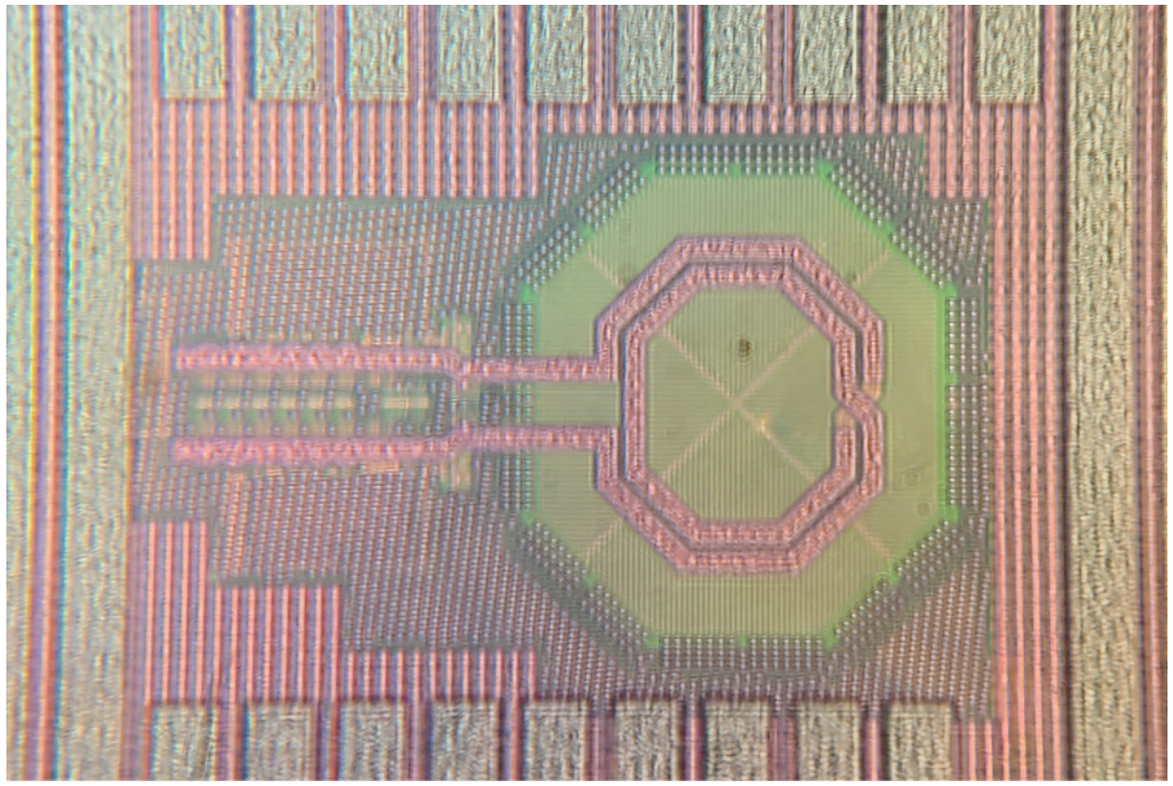
ECON-D-P1

ECON-D-P1

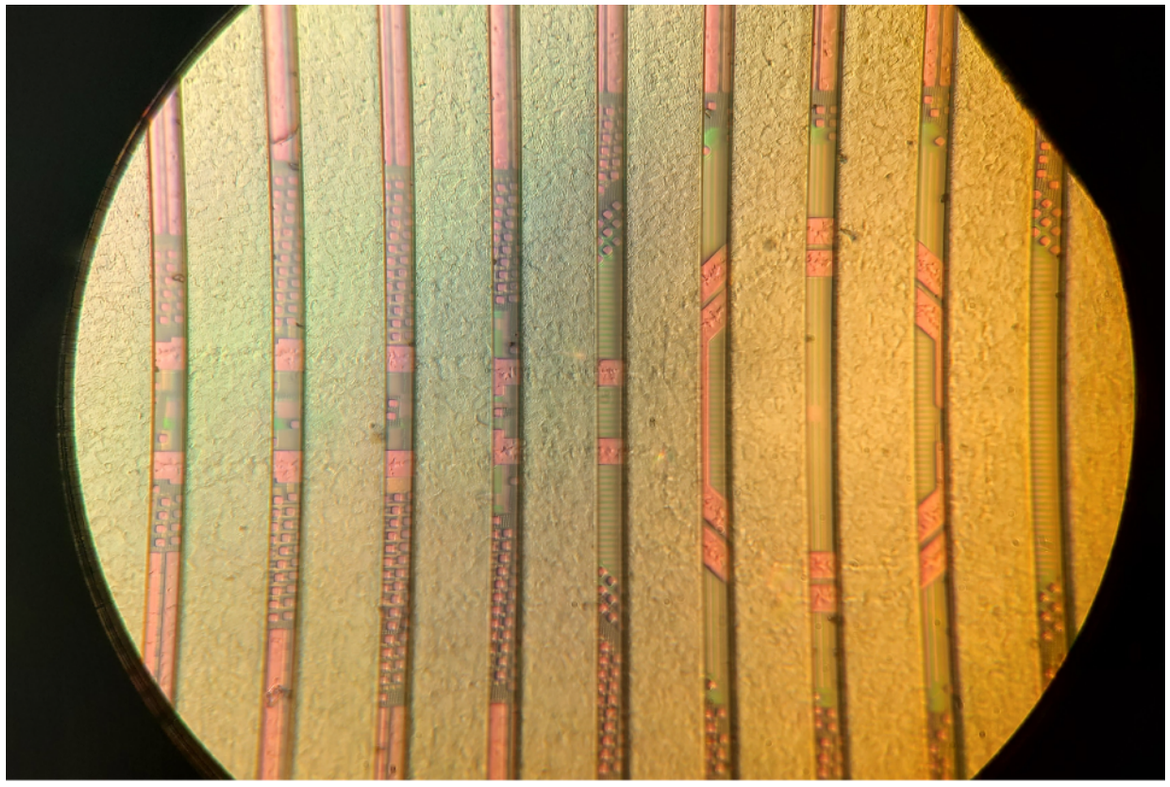
ECON-D-P1 issue : metal stripes over PLL

- ECONs use lpGBT PLL based on LC-tank Voltage Controlled Oscillator (VCO).
- PLL worked well in ECON-T-P1
- ECON-D-P1 design unintentionally included top metal stripes for power distribution above the inductor of the PLL.
    - Top metal layout not included in verification and does not trigger design rule violation
- Power stripes reduce magnetic flux through inductor -> reduces inductance -> increases frequency of VCO
- ECON-D-P1 operates at 41.5 - 49 MHz — NOT 40 MHz

Correct layout in ECON-T-P1 :

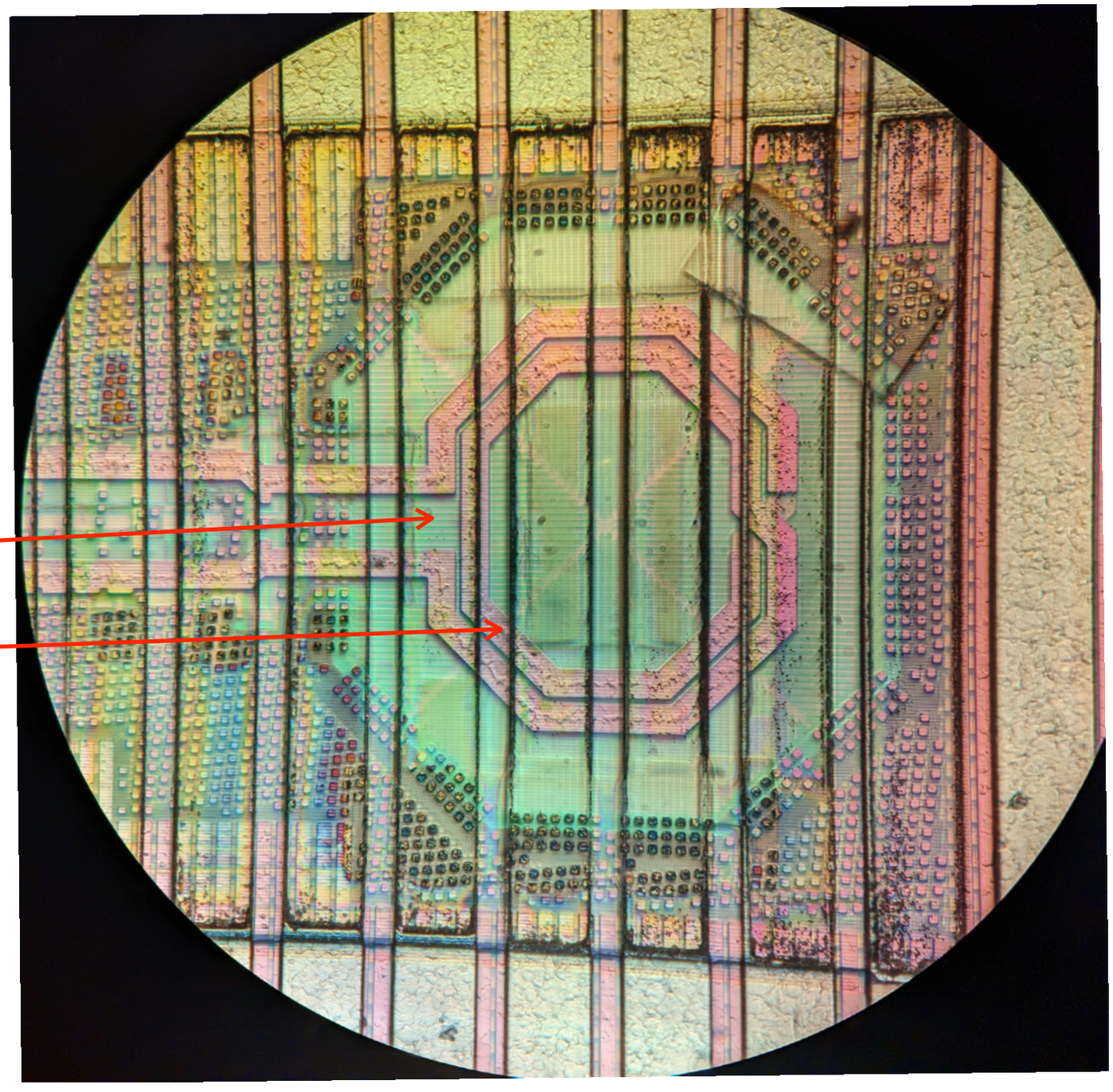


Incorrect layout from ECON-D-P1;
AP-layer metal stripes ARE over the PLL circuit:



Removing “extra metal” with FIB

- We removed the extra metal with a Focused Ion Beam (FIB) from 5 chips in July
- PLL locking range with metal stripes removed matches expectation of 36–44 MHz ✅.
- Simulation results match observed ~5 MHz frequency shift, confirming that extra metal is the only issue ✅.



- Top metal stripes removed
- Apparent “pedestals” left in dielectric between top and M9

Plan to provide 40 MHz ECON-D-P1 in Fall 2023

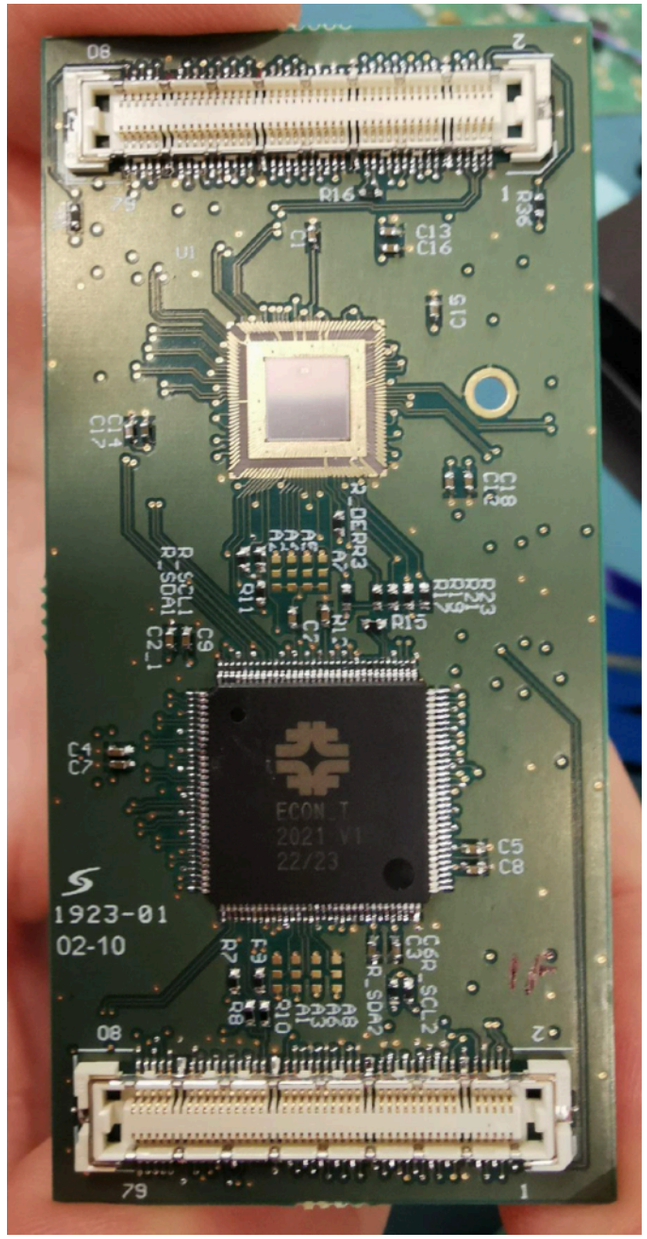
- **ECON-D-P1 that operate at 40 MHz required** for
  - **Sep 2023** : Test beam (2 ECON-D-P1)
    - 1 at CERN, 1 more to ship to CERN today, 1 stays at FNAL
  - **Oct 2023** : System test of 2 full LD wagons (12 ECON-D-P1) for ESR
  - **Nov 2023 – early 2024** : Cassette prototype test (~100 ECON-D-P1)
  - Production chips not available until April 2024

- Perform **FIB modification** on 15 additional ECON-D-P1.
  - PO to be released this week.
  - Vendor to deliver 5 chips/week on Sep 22, Sep 29, Oct 6 (approx) ✅
  - Chip-on-board Concentrator Mezzanines (CM) available to ship from Fermilab on Sep 29, Oct 6, Oct 13

- Perform **mask respin** of ECON-D-P1 prototype run to produce 400 ECON-D-P1 with corrected top metal (minimum)
  - Predicted foundry ship date : Oct 24 ✅
  - Arranging packaging now
  - Ship foundry → IMEC → CERN → IMEC → Packaging vendor by Nov 14
    - Direct shipping foundry → packaging vendor would save ~3 weeks, if possible

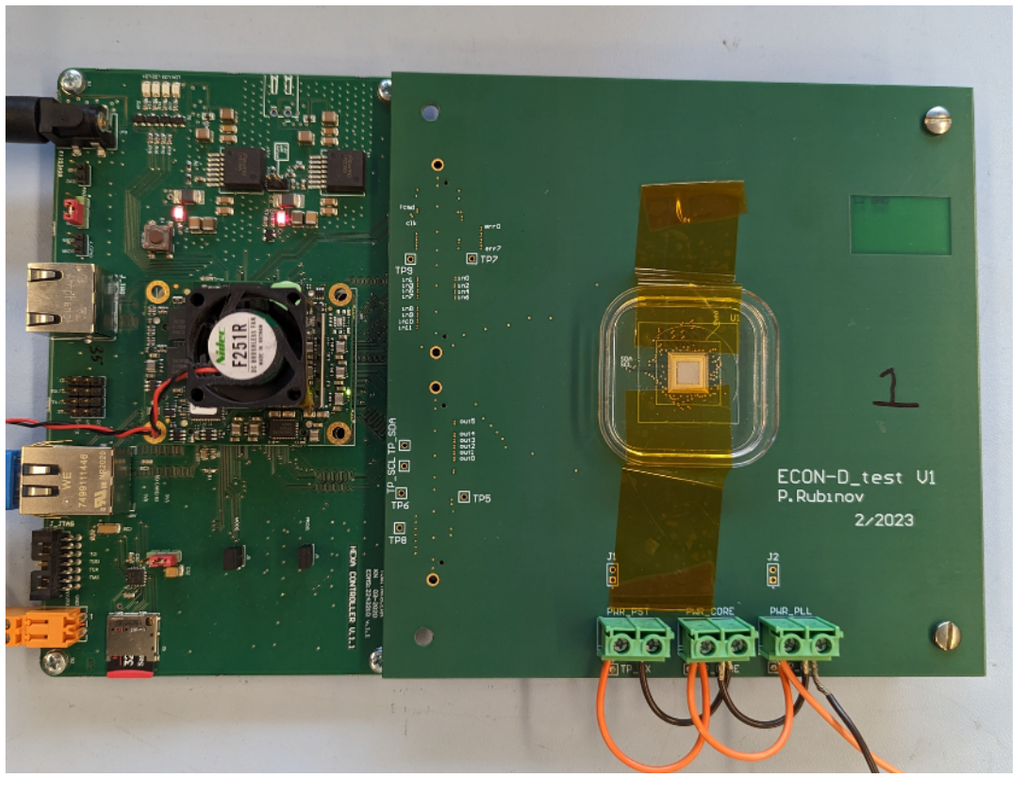
- CM test system:
  - PCB for standard CM : produced, but unassembled
  - FW and SW are both based on ECON test infrastructure with focus on verifying good CM assembly (rather than ECON functionality)

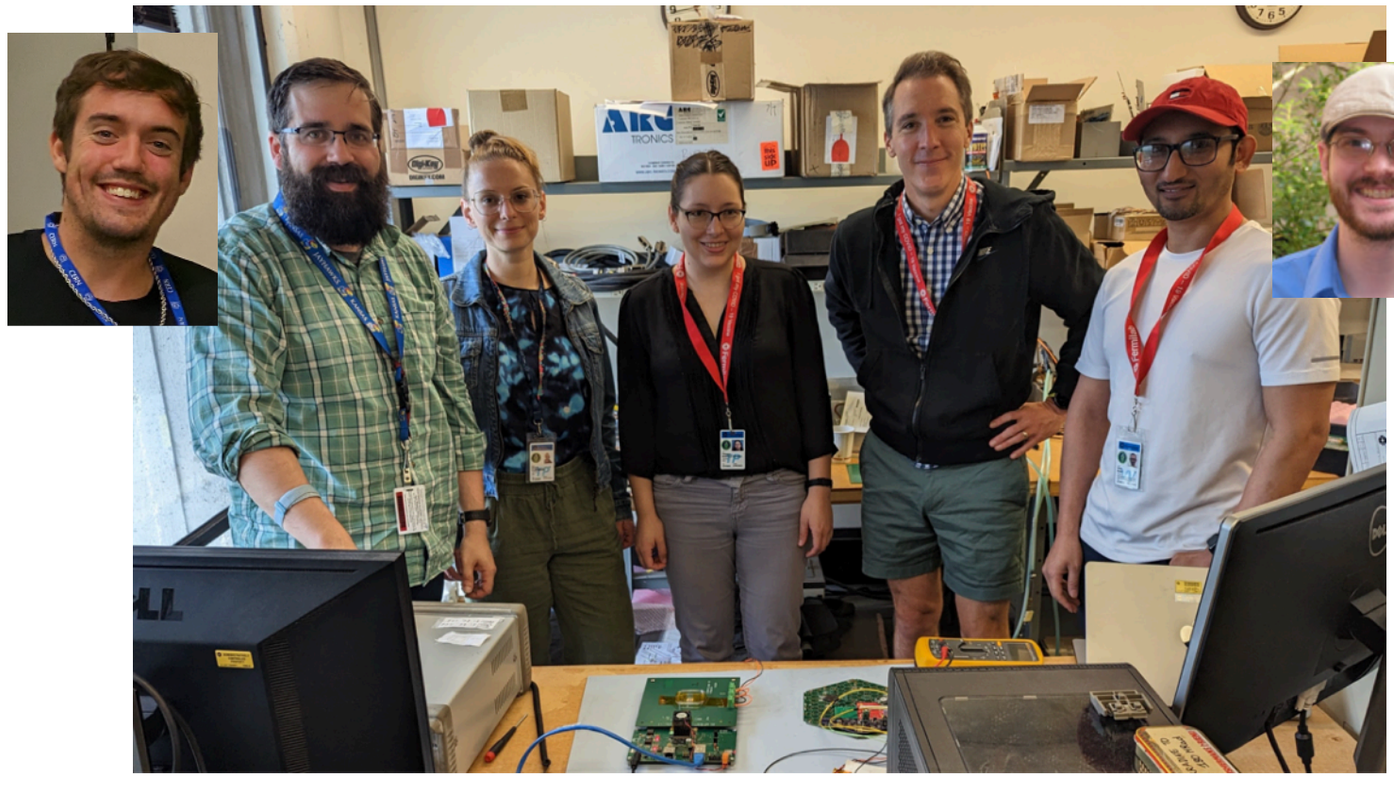
CM with FIB-modified
ECON-D-P1 and ECON-T-P1



ECON-D-P1 testing

- **June 26** : First ECON-D-P1 available ✅
- **July** :
  - Initial Functionality testing ✅
  - PLL “extra metal” diagnosis ✅
  - Characterization of FIBed chips ✅
  - Preparation for radiation testing ✅
- **August 5** : Single Event Effect (SEE) testing at Northwestern Medicine Proton Center cyclotron ✅
- **August 18 - 30** :
  - System noise diagnosis and fix ✅
  - Total Ionizing Dose (TID) testing at CERN ObeliX X-ray machine ✅

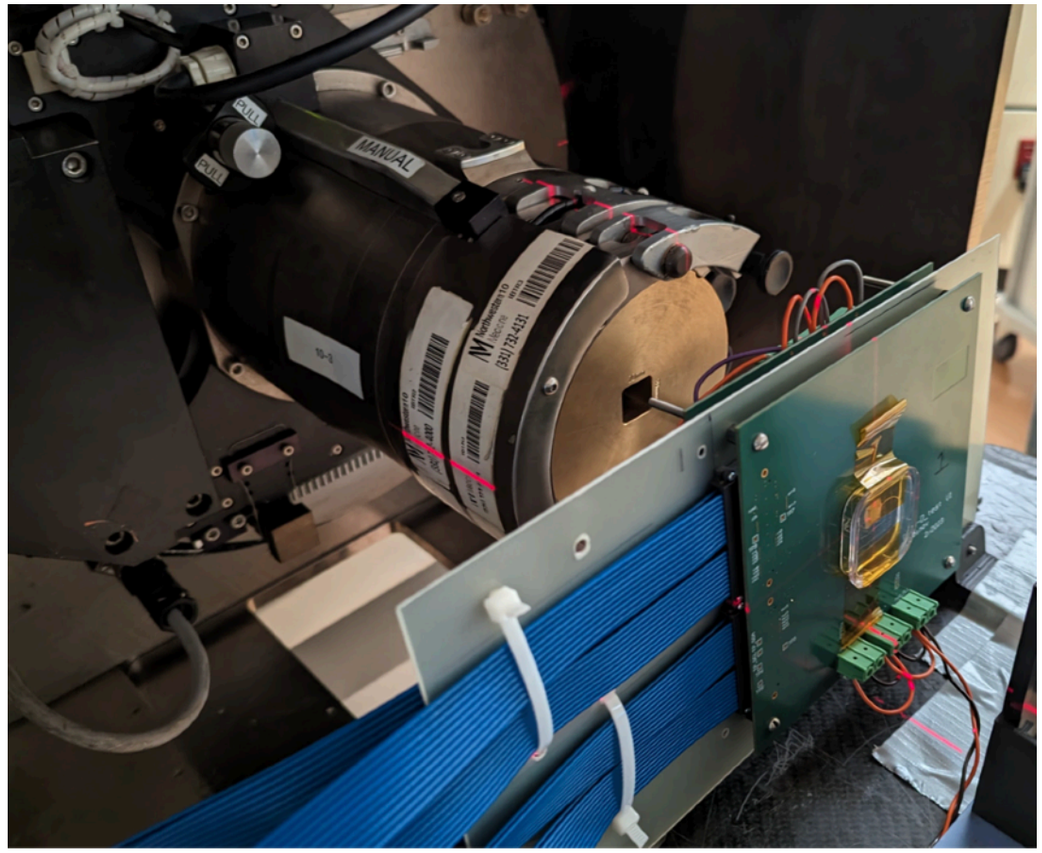




ECON-D-P1
SEE testing

- Northwestern Medicine Proton Center Cyclotron
  - 200 MeV protons
  - Flux = 3e10 /cm^2/s
  - Fluence = 5e13/cm^2 per chip

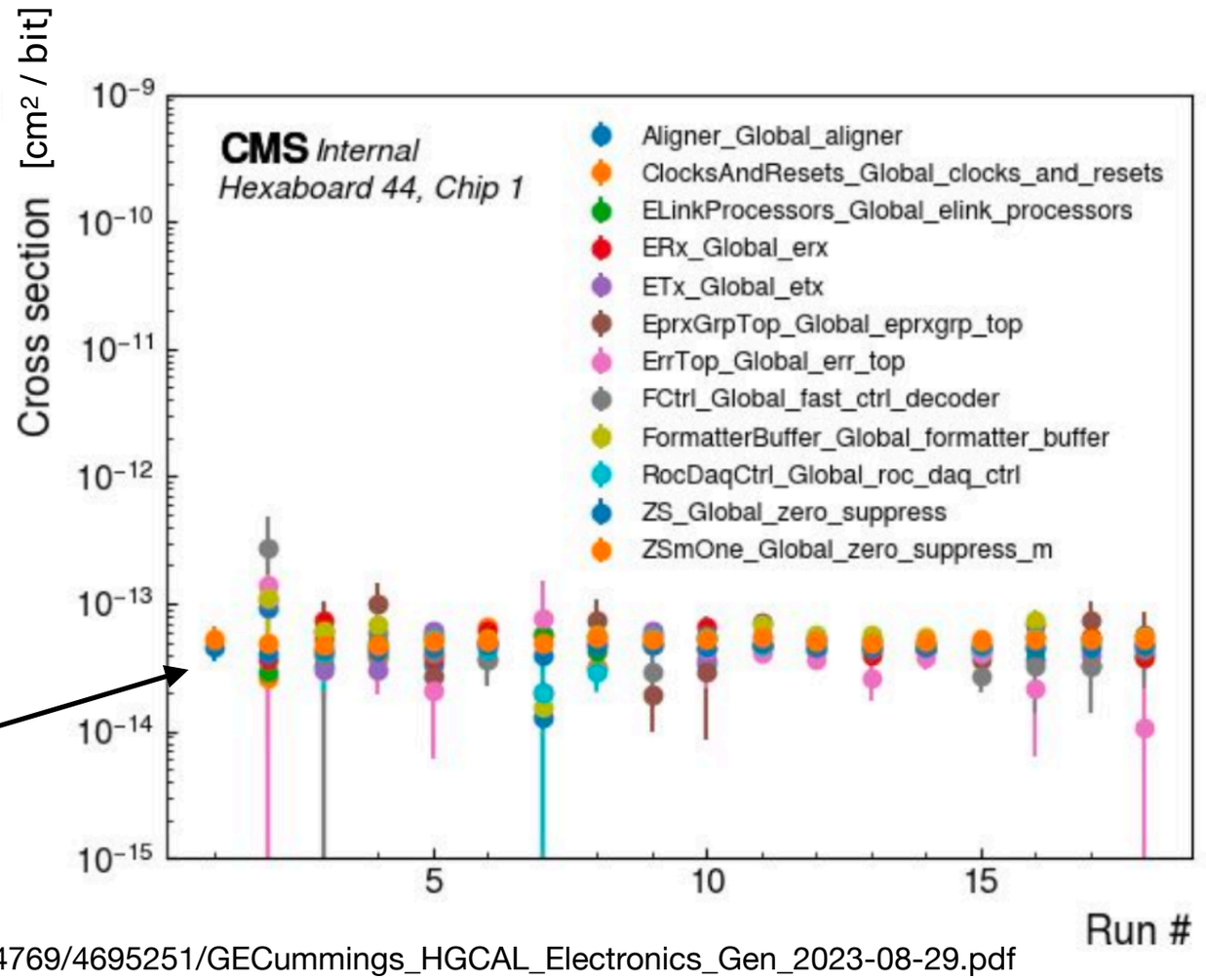
- Tested 2 chips for total fluence = 1e14/cm^2
- HL-LHC high-energy hadron fluence averaged over all HGCAL ECONs = 1e14/cm^2
- **20x higher fluence** than for ECON-T-P1 ✅



Results:

- Observed zero errors requiring chip reset →
  - Rate for all HGCAL < 1.3e-3 errors/sec (95% CL)
  - **Period for all HGCAL > 13 minutes/error (95% CL)** ✅
- Observed zero configuration errors ✅
- Measured SEU cross section / bit using internal monitoring of TMR corrected errors — good agreement with ECON-T-P1 and RD53_SEU chips ✅
- Detailed analysis progress

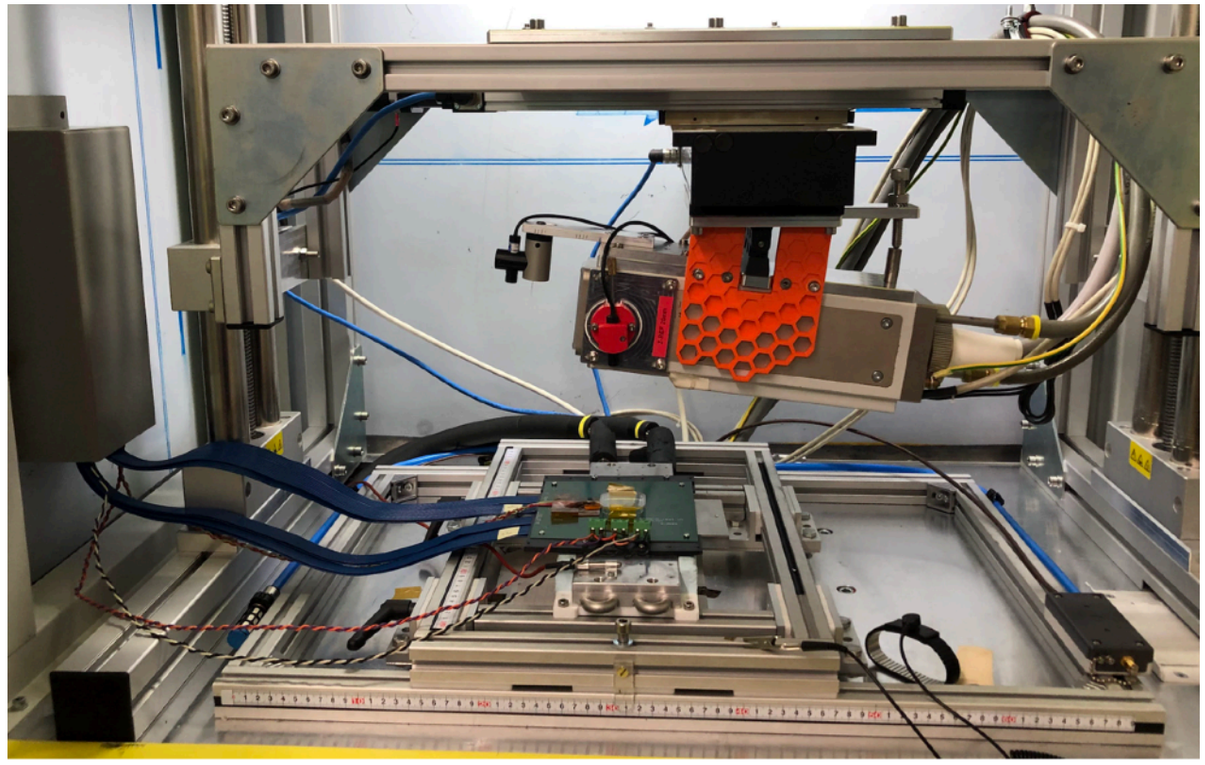
SEU cross section per pre-voted bit measured in 12 configuration register blocks in 15 “runs” with fluence 1e10-1e13/cm2 each.



https://indico.cern.ch/event/1317001/contributions/5555049/attachments/2704769/4695251/GECummings_HGCAL_Electronics_Gen_2023-08-29.pdf

ECON-D-P1 TID testing

- CERN ObeliX X-ray facility
- HGCAL requirement = 220 Mrad
- Irradiated 3 chips ✅
  - 1 chip with FIB modification
  - 2 chips without FIB modification



Test parameters:

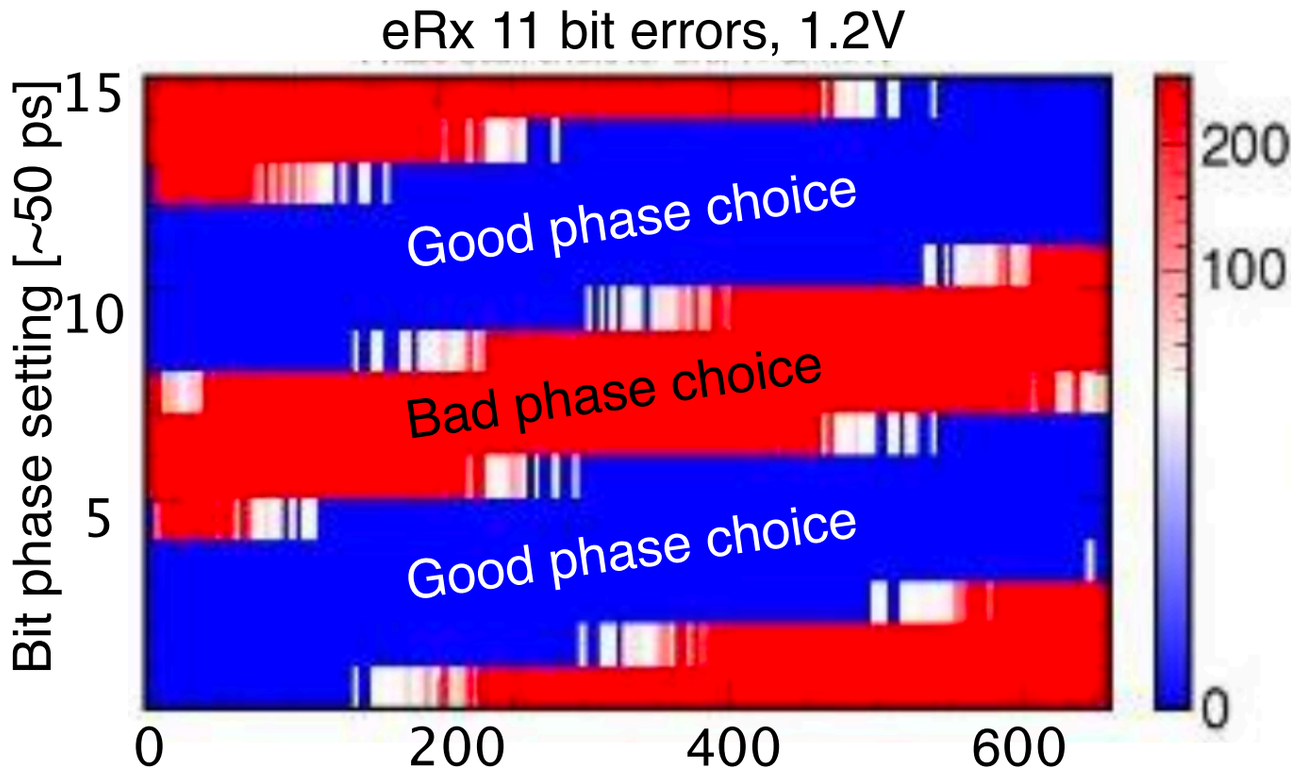
- TID = 660 Mrad/chip ✅
- Dose rate = 9.2 Mrad/hour
- Temperature ~ -20°C
- VDD : 1.08 - 1.32V
- CLK freq : nominal ± 1 MHz

Continuous test loop at all VDD + Freq

- Power draw, temperature
- Automatic PLL capacitance selection
- Bit alignment phase scans on 1.28 Gbps inputs/outputs
- 4 Built-In Self Tests (BIST) for each of 24 SRAM/chip
- Bit errors on 1.28 Gbps outputs eTx

Results:

- Failure of 1/4 BIST for 1/24 SRAMs at 100 Mrad, 1.08V 🟥
  - Diagnosis in progress
- Good behavior to 660 Mrad, 1.2V ✅
  - Evidence of small bit error rate at 450 Mrad, 1.08V



https://indico.cern.ch/event/1317001/contributions/5555050/attachments/2704780/4695462/Campbell-TID-Testing-Summary-Corrected.pdf

ECON-D-P1 Functionality Testing

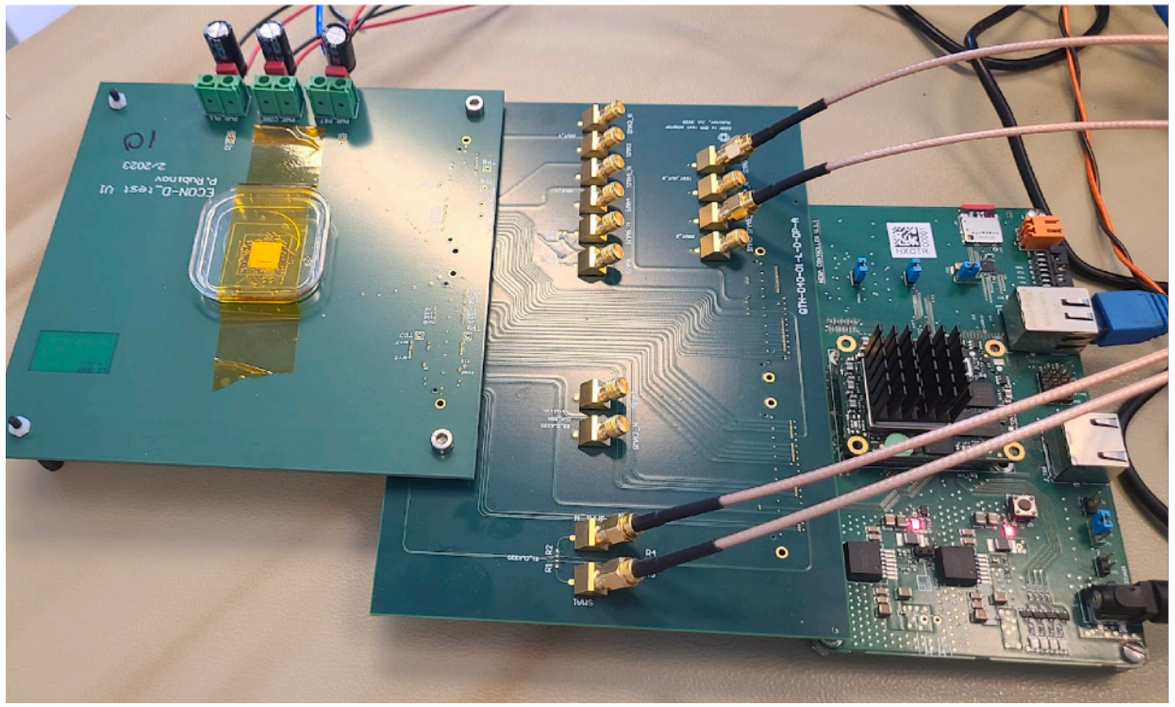
- We have extensive experience with ECON-D-P1 : multiple chips operated continuously by multiple users since June 26

Systematic functionality testing in decent shape, but delayed by:

- study of PLL “extra metal” issues
- preparation for radiation testing
- test system power-related jitter issues

System jitter diagnosed and fixed with additional decoupling ✅

- Studies being applied to CM design
- Thanks for S.Kulis and S.Beiereigel (CERN) for help diagnosing!



✔️ Done
🚧 Work In Progress.
✔️/🔄 Functionality checked, additional characterization tests still planned
👍 Good

Block	Test	Status	Result
FC	Receive FC clock	✔️	👍
	Receive and respond to FC	✔️	👍
	Introduce FC errors	✔️	👍
PLL	Lock with ref. clock	✔️	👍
	Lock with input test clock	✔️	👍
	Measure locking time	✔️	👍
	Measure VCO frequency / lock	✔️	👍
	Lock with range of frequencies	✔️	👍
	Set VCO CapSelect manually	✔️	👍
I²C	R/W to every register	✔️	👍
	R/W to every I²C address	✔️	👍
	Read data stream during I²C	✔️	👍
Aligner	Automatic/Manual word align	✔️	👍
	Trigger manual snapshot	✔️	👍
	Alternative masks/IDLE	✔️	👍
ePortRX	Phase-align with fixed-phase mode	✔️	👍
	Phase-align with automatic mode	✔️	👍
	Manual phase-align after resets	✔️	👍
	PRBS after phase/word alignment	✔️	👍

Block	Test	Status	Result
Resets	Verify reset functionality	✔️/🔄	👍
	Read data after/during reset	✔️/🔄	👍
	Time to recover from reset	🚧	
Datapath	Pass-through mode	✔️	👍
	Test simple mode	✔️/🔄	👍
	Test predictive mode (low priority)	🚧	
	Varying zero suppression thresholds	✔️/🔄	👍
	E/B/O reconstruction and matching	🚧	
Formatter / Buffer	Fill/Empty buffer	🚧	
	Vary neTx and truncation	🚧	
	Packet Vetos	✔️/🔄	👍
eTx/eRx	Eye diagram	✔️	👍
	Inversion and individually enable	🚧	
Reset Requests	Check watchdogs	🚧	
	Clearing requests	🚧	
Power	Maximum/minimum consumption	🚧	
	Nominal configurations and vary datasets, voltage, neTx	🚧	
Env.	Operate at -30 C	✔️/🔄	
	Operate at 1.2V ±10%	✔️	

https://indico.cern.ch/event/1317001/contributions/5555047/attachments/2704779/4695269/ECOND_Testing_Summary_August_29_2023.pdf

ECON-D-P1 in b27 readout system

- CM with ECON-D-P1-40MHz and ECON-T-P1 brought to CERN on Aug 17.
- Many thanks to Milos Vojinovič, Andre David, and Ragu Shukla for rapid deployment and evaluation in the b27 ROC → ECON → Serenity test system
- Results from Aug 29 look good:

- I2C ok for both ECONs and PUSM state is READY.
  - …but I2C address conflict with ROC. ←RESOLVED
- (Bare unencapsulated and wire-bonded) ECON-D-P1
  - ROC→ECON-D alignment: OK
  - ROC event data in ECON-D snapshot: OK
  - ECON-D→Serenity alignment: OK
  - ECON-D packets to Serenity*: yesterday
  - ROC/ECON-D EBO alignment: "as we speak"
- (Packaged) ECON-T-P1
  - *Was the packaged chip tested before assembly? Yes, according to Danny*
  - ROC→ECON-T alignment: Not OK ← In progress?
    - One issue resolved - eRX sampling phase (cont. phase track)

https://indico.cern.ch/event/1317001/contributions/5556307/attachments/2704882/4695444/20230829 ECON mezzanine at b27.pdf

ECON-D-P1 Known Issues

- No issues **require** fix, but fixes are available and chip could be respun in ~1 month (reimplement blocks, top-level, and redo verification)

Name	Impact	RTL solution	Description
15-word packet	Low	Yes	Packet data + following mandatory IDLE corrupted for rare case (15-word packet) + (active eRx11) + (eRx11 ch35 & ch36 passing ZS) → loss of sync with BE
CRC calc	Very Low	Yes	CRC corrupted for very rare case of packet with repetitive data → lost event, no loss of sync with BE
Error-In	Low	Yes	Inversion of logic handling Error-In pins prevents use for forwarding ROC PLL Lock bit ; ECON will detect loss of lock through sync monitoring
S-bit	Very Low	Yes	Inversion of logic handling internal errors corrupts status bit summary in event packet header ; currently not used by BE
SET I2C	Low	Yes	SET vulnerability in i2c logic could result in corruption of configuration; addressed with read back

- **ROC+ECON RTL co-simulation**: details of system behavior in response to Chip_Sync and Event Buffer Reset Fast Commands warranting discussion before ECON submission
    - Will finalize plan at Sep 12 HGCAL Electronics meeting
- More on final slide

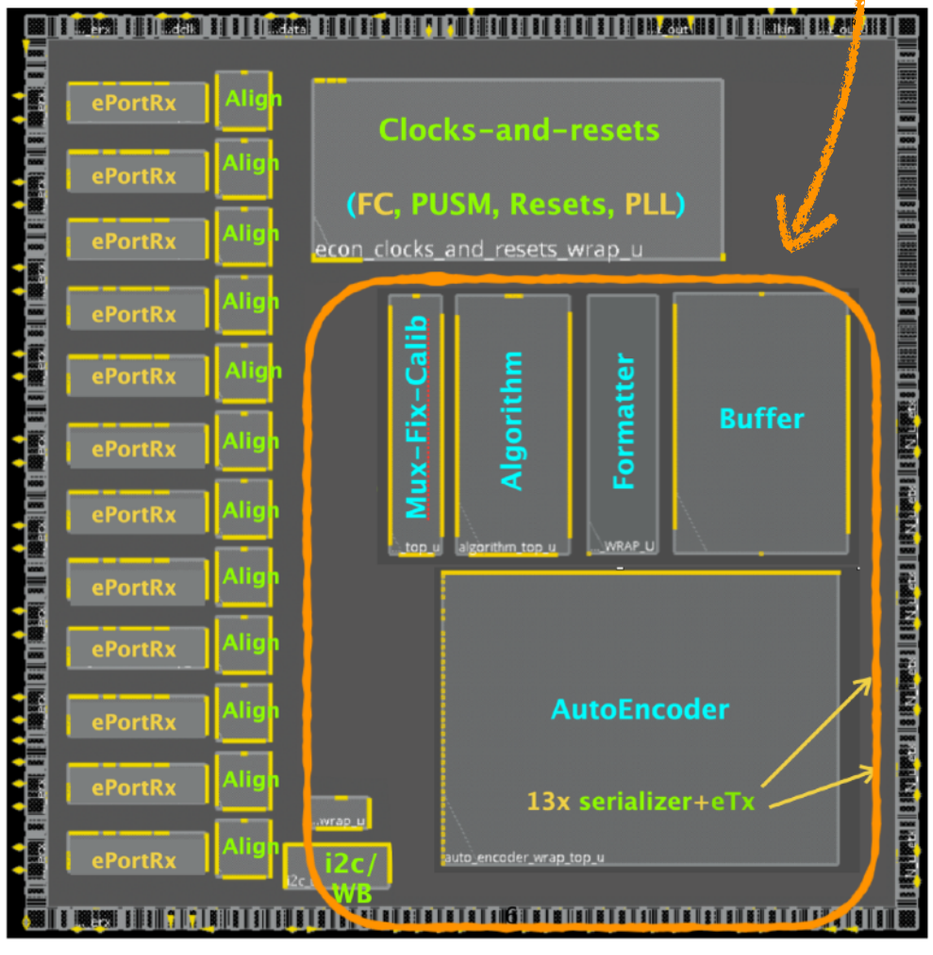
https://indico.cern.ch/event/1317001/contributions/5555096/attachments/2704145/4696048/econ_pre_review_EDITED.pdf

ECON-T2 strategy

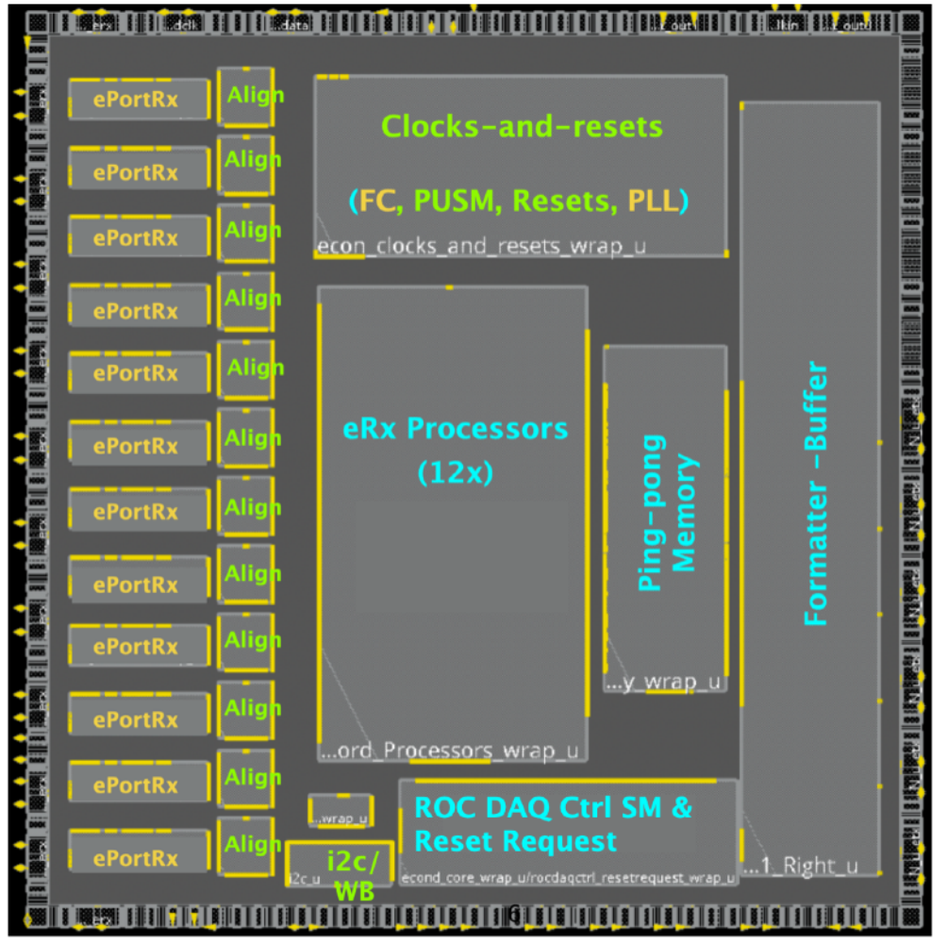
ECON-T-P1 data-handling blocks (orange box) will be dropped into ECON-D architecture allowing ECON-T2 to benefit from improvements in ECON-D triplication, clock distribution, and I/O periphery.

	RTL status	
	April 1, 2023	May 3, 2023
Modify RTL & UVM : i2c / slow control	Complete	Complete
Modify RTL & UVM : MUX-Fix-Calib	Merge in progress	Complete
Modify RTL & UVM : Algorithms	Merge in progress	Complete
Modify RTL & UVM : Formatter	Merge in progress	Complete
Modify RTL & UVM : Buffer	In progress	Complete
Modify RTL & UVM : Top-level	In progress	Complete
Update handling of misaligned eRx	In progress	Complete
Update Super Trigger Cell encoding	Not started	Merge in progress

ECON-T2



ECON-D



ECON-T2 design status

- Several RTL + UVM code releases since April :

Release	Impact	Description
2.0.0	Apr 26	First release
2.1.0	May 17	Include “Bad eRx” module
2.2.0/1/2	Jun 2-9	Major UVM deployment, minor RTL bugs
2.3.0	Jun 30	UVM read-from-file; RTL bug fixes
2.4.0	Jul 20	UVM+RTL Bug fixes
2.5.0	Sep 4	Final RTL

UVM status

- AutoEncoder UVM model recently included
- Model for Bad eRx module in progress — complete this week or next
- Packet length coverage still could be improved

PNR status

- Have worked through entire design flow except (i) DRC density and (ii) LVS checks
    - Continue working on these in v2.4.0
- Block-level PNR for v2.5.0 in progress — takes ~1 week
- Top-level PNR takes ~1 day + ~1 day to provide output data for UVM
    - Will include clock glitch filters for first time in v2.5.0 — could introduce small delay

ECON Engineering Run planning

ECON Engineering run submission endgame

- Planning to submit combined ECON-T + ECON-D engineering run in early Nov-2023 — exact date is flexible
  - Produce 46k ECON-T + 56k ECON-D
  - Produce maximum 20 engineering run wafers + 25 production wafers (minimum lot)

Month	Sep				Oct				Nov			
Week	36	37	38	39	40	41	42	43	44	45	46	47
ECON-T2 block PNR	Davide + Gianmario											
ECON-T2 top PNR		Chinar + Alpana										
ECON-T2 RTL UVM	Already running											
ECON-T2 post-layout UVM					Requires final PNR							
ECON-D2 RTL release												
ECON-D2 block PNR				Davide + Gianmario								
ECON-D2 top PNR					Chinar + Alpana							
ECON-D2 RTL UVM	Already running											
ECON-D2 post-layout UVM							Requires final PNR					

- ECON-T2:
  - Design completion by end September
  - UVM completion in October

- Potential ECON-D2:
  - RTL release + block PNR + top PNR + UVM could be interleaved with ECON-T2 work
  - UVM has been running in parallel all summer - ECON-T2 developments also verified for potential inclusion in ECON-D2
  - Realistic schedule impact would not be zero, but would be “few weeks” rather than “month or two”
  - ECON-D2 respin would draw some attention from ECON-T2 final verification.
  - Decision on ECON-D2 respin planned for Sep 12 meeting

Important ECON meetings in Sep-Oct

Date	Goal
Tues, Aug 29	Introduce ECON-D-P1 testing results and known issues meeting
Tues, Sep 12	Require decision on whether to respin ECON-D to implement fixes for ECON-D-P1 known issues
Tues, Oct 10 (TBC)	ECON-T2 (and ECON-D2?) submission review

Additional Material

ECON-T-P1 issues

- All issues are understood and verilog fixes implemented or obviated.
- Issues in red will be fixed implicitly by adoption of ECON-D architecture.

Block	Issue	Fix	Impact on ECON-T-P1 and system testing
PLL	Naming mismatch in verilog prevents automatic VCO capacitor selection.	Verilog fix	Manually select VCO capacitor via I^2C.
PUSM	PUSM requires all ePortRx DLL to lock regardless of whether ePortRx is active.	Verilog fix	Run with all ePortRx enabled.
Aligner	Error counters used gated I^2c clock, i.e. only count errors every 256 clocks.	Verilog fix	Error counters miss sporadic or rare errors.
Serializer	Endianness is inverted (intended MSB first).	Verilog fix	Revert endianness in back-end electronics.
Serializer	SEUs in "data enable" circular shift registers.	Verilog fix	None
System	Functionality to route different PLL output clocks to CLK MON pins was not implemented.	Verilog fix	CLK MON pins observe fixed PLL output clock.
System	Phase of enable for serializer synchronized to incorrect 40MHz clock.	Verilog fix	Manually adjust phase
BE alignment	Empty buffer required for well behaved Link-Reset-ECON-T alignment sequence	Verilog fix	Perform backend alignment with empty buffer or STC/BC algorithms
I^2C	Power draw during I^2C transaction leads to jitter in 1.28 GHz clock	I^2C clock gating updated	Proper phase alignment of eRx.
Autoencoder	SEU rate larger in last 100 bytes out of 1608 bytes of I^2C weights	Verilog fix	None
Error Mon.	Mask bits on alignment errors in a single channel cannot be set via i2c	Verilog fix	Cannot mask individual errors, only error status of full channel (no impact on testing)

Suppress data from bad eRx + mask error bits with FC

New block

ECON-D-P1 packaging

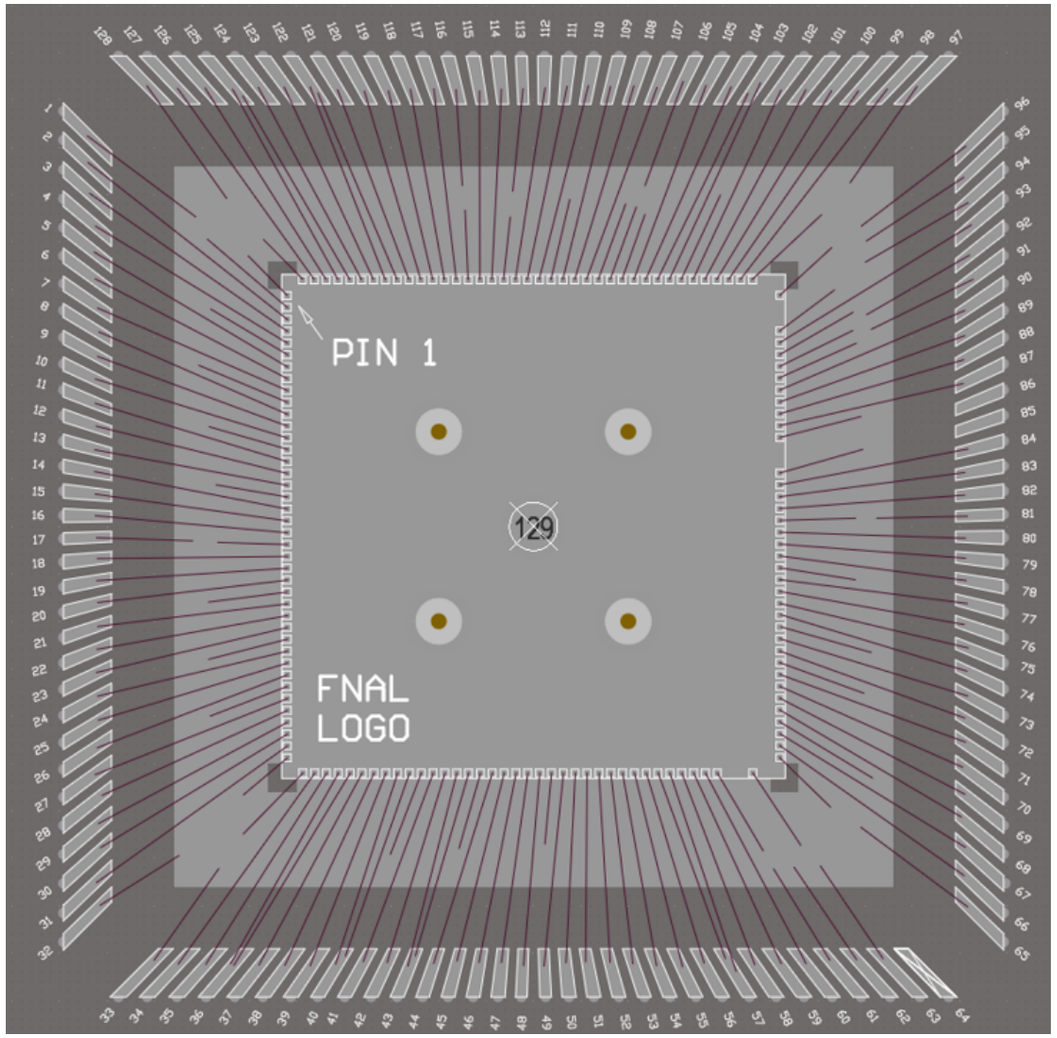
- Chip can be fully tested with wire bonded chip-on-board test system

- **Same IMEC+Greatek vendor and process as ECON-T-P1 (2022)**
  - Interactions managed by IMEC
  - Same process for DUNE ASICs
  - Package in two batches (100 parts + 350 parts)

- Greatek **maintained quoted 4 week leads time** for packaging of 100+100 parts for ECON-T-P1

- **Technical preparation for assembly** is proceeding — Greatek has everything they need (bonding diagram, netlist, expected dates, etc)

- **Purchase order finalization** in progress
  - Final quote from IMEC received in April
  - Purchase req is working way through CERN system – and being followed closely.



System tests : ECON-T-P1 & ECON-D emulator

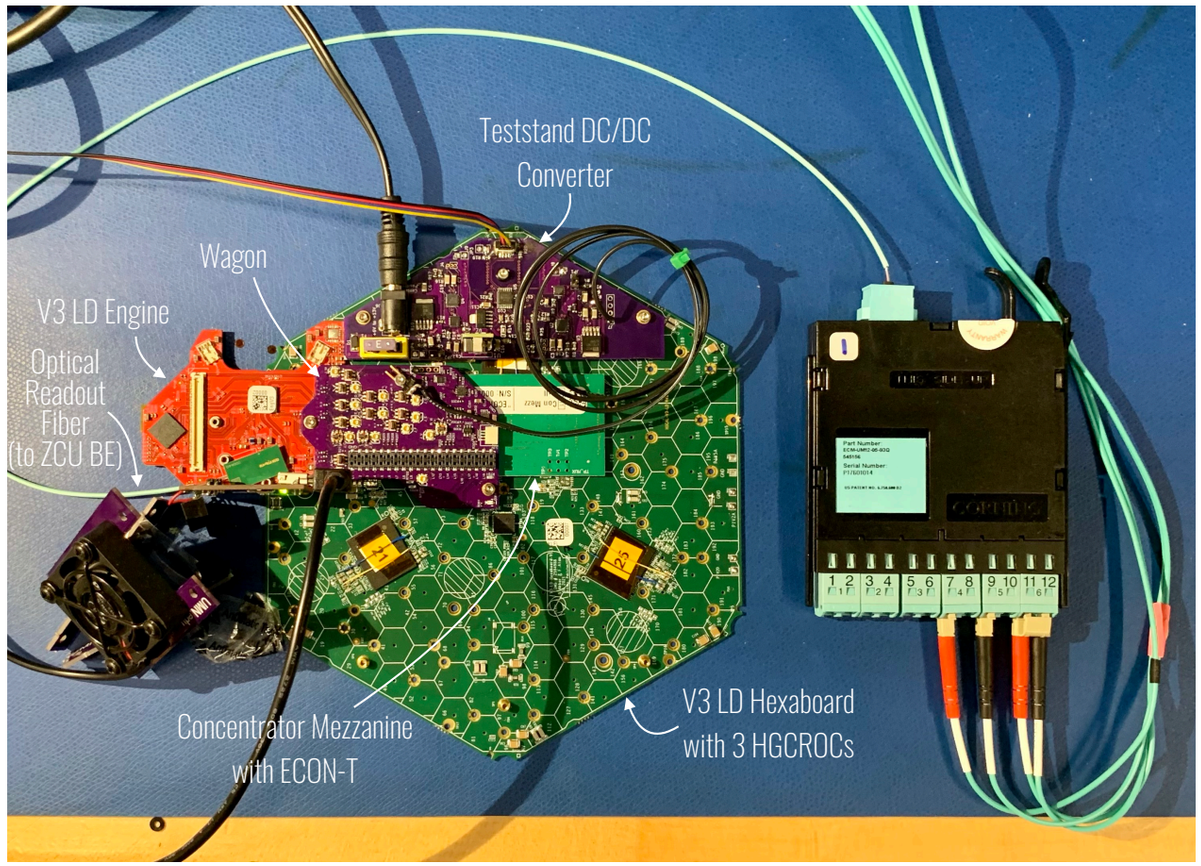
System tests with ECON-T-P1 and ECON-D emulator verifies interfaces:

- Reset functionality, Realistic fast command response latency
- Confirm automatic & manual alignment for both ROC-ECON and ECON-BE

Three system test stands exist:

- **Minnesota** and **Fermilab**:
  - ROC → ECON-T-P1 → ZCU link capture
  - ROC → ECON-D emulator in ZCU
- **CERN** :
  - ROC → ECON-T-P1 → Serenity back end (BE)
  - ROC → ECON-D emulator in Serenity BE

Minnesota front-end test stand (very similar setup at FNAL)



Minnesota has verified

- Stable alignment of ROC → ECON-T-P1
- Stable alignment of ROC → ECON-D emulator
- Reset behavior and stable alignment following reset
- ROC + ECON-D emulator response to L1A

Recent progress at Fermilab:

- V3 test stand setup in March
- Tested reset sequences, link stability, ECON-D emulator functionality

At CERN, successfully exercised:

- ROC → ECON-T-P1 → back end (BE) path
- ROC → ECON-D emulator → BE path
  - Slow+fast control of FE performed with DAQ BE
  - Capture/unpack ECON-T (D) data with TPG Stage 1 (DAQ BE) firmware

ECON testing resources

- Team has good coverage for needs in robot, hardware, firmware, software, and test execution.

Person	Primary Role	Inst.	Pos
Klabbers	Robot	FNAL	Sci
Mantilla-Suarez	Software	FNAL	Post doc
Cummings	System testing	FNAL	Post doc
Noonan	Software	FNAL	Sci
Rubinov	Hardware	FNAL	Sci
Wilson	Firmware	Baylor	Post doc
Bam	ECON-T testing	U Alabama	Student
Campbell	ECON-D testing	U Alabama	Student
Babbar	Robot	Panjab	Student

ECON design resources

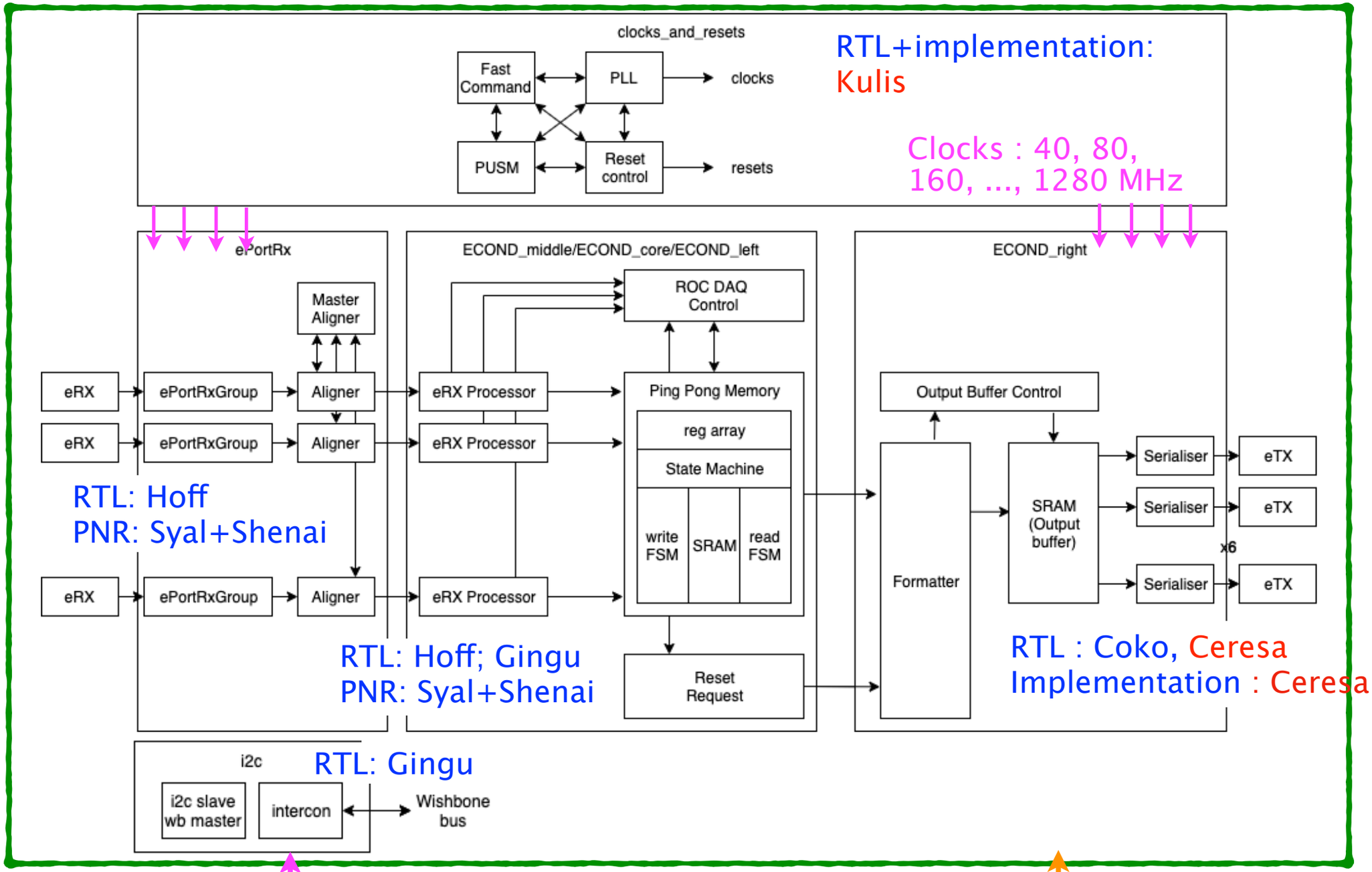
* RTL = Verilog
  UVM = Verification
  PNR = Place-and-route

- Since the Nov-2022 P2UG report, **addition of 3 new designers** (**) provides excellent team depth and invaluable flexibility for replanning work to minimize delays.
  - 1 new FNAL engineer for UVM
  - 2 new CERN ESE (CHIPS) engineer for RTL/UVM and PNR

		Expertise				
Person	**Primary Role for ECON-T2**	**RTL***	**UVM***	**Analog**	**Digital**	**Inst.**
Hoff	Lead Eng, RTL, UVM	X	X			FNAL
Gingu	UVM, RTL	X	X			FNAL
Kharwadkar **	UVM		X			FNAL
Shenai	Fully Granular block-level PNR				X	FNAL
Syal	Top-level PNR				X	FNAL
Lupi	UVM	X	X			CERN
Ceresa	Formatter/Buffer	X		X	X	CERN
Kulis	MUX-Fix-Calib+TMRG	X		X	X	CERN
Scarfi' **	SEU/SET sim + UVM	X	X			CERN
Bergamin **	Algos + Power Ana + CDC UVM	X		X	X	CERN
Other recent contributors to design and verification						
Wang	PLL	X		X		FNAL
Noonan	UVM support		X			FNAL
Coko	Formatter RTL	X			X	Split

ECON-D division of labor

Full chip assembly : Syal, Shenai



Verification

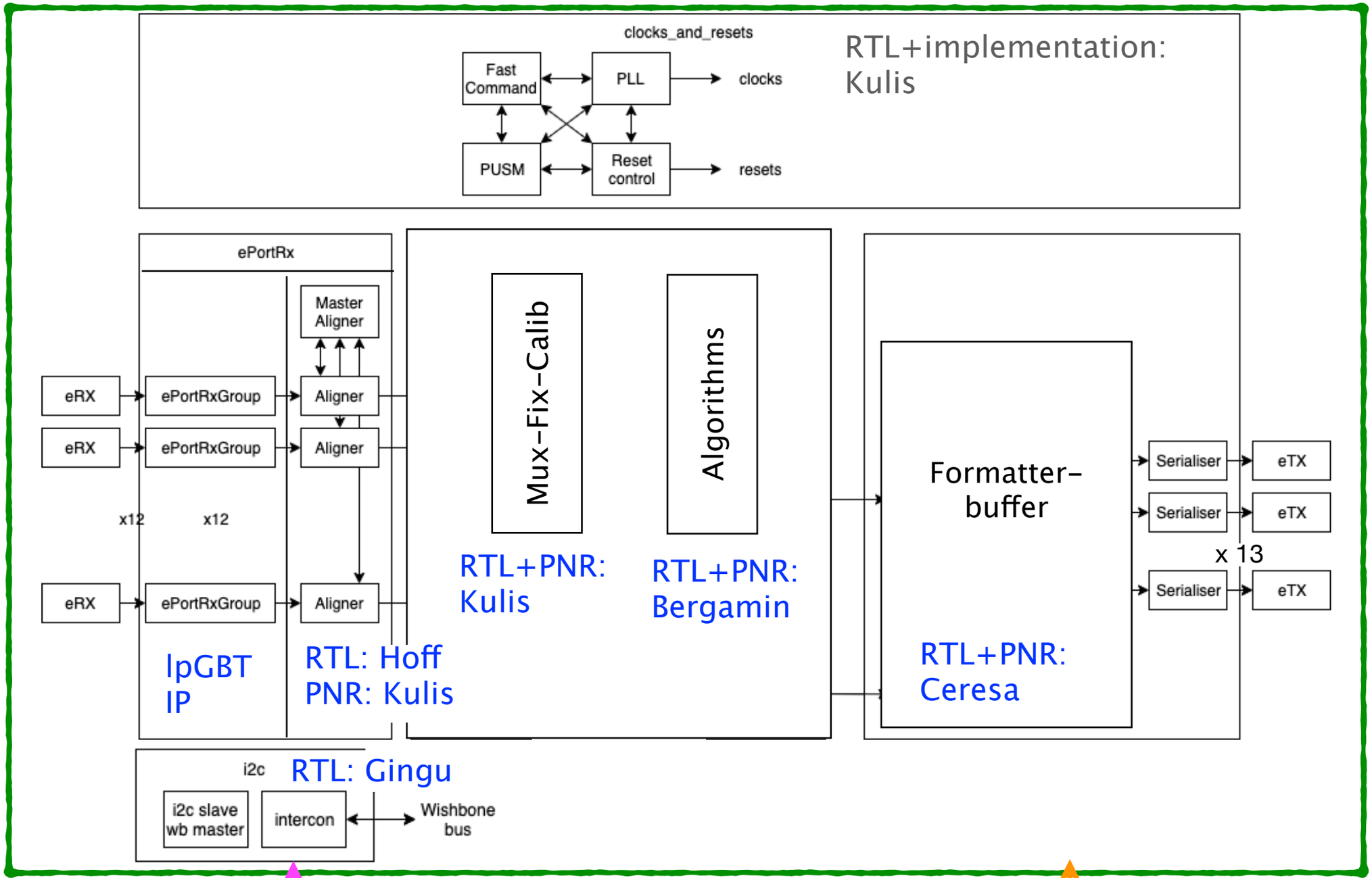
Lupi, Hoff

SEU Verification

Lupi, Hoff

ECON-T2 division of labor

Full chip assembly : Syal; Full-granularity block PNR : Shenai



Verification

Lupi, Hoff, Gingu, Scarfi', Kharwadkar (ECON-D focused)

SEU Verification

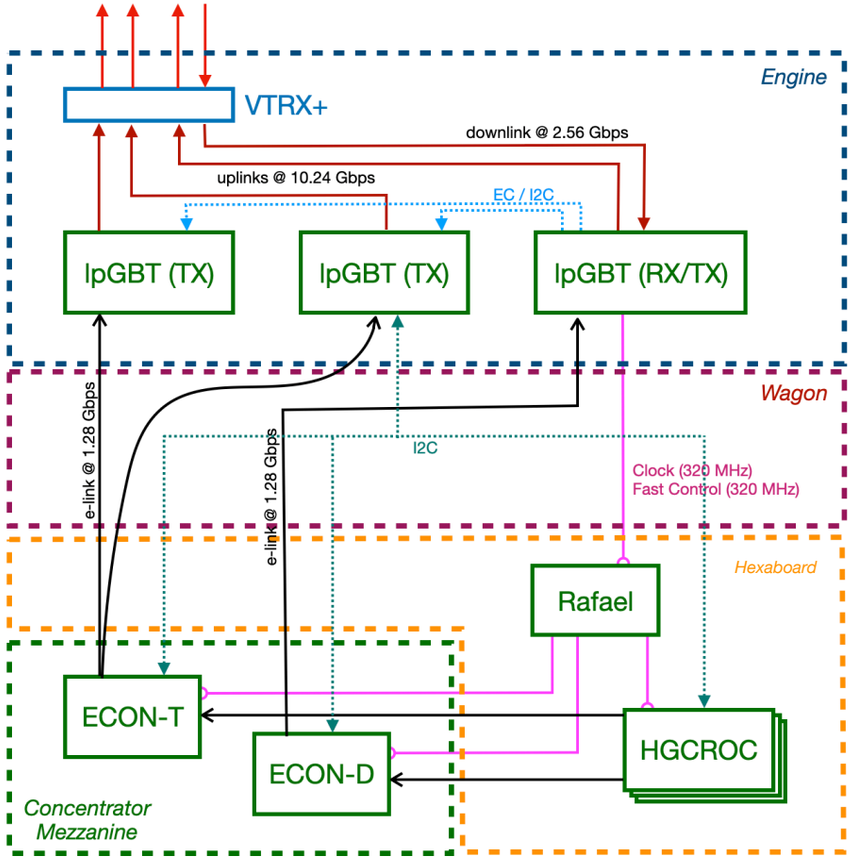
Lupi, Scarfi'

Overview

Two Endcap Concentrator (ECON) ASICs on independent data paths:

- **ECON-T** : select or compress HGCROC trigger data for transmission off detector at 40 MHz
  - includes five user-programmable algorithms for data selection/compression
  - Each main logic block performs same function at 40 MHz
- **ECON-D** : perform most digital processing of sensor data for events passing L1 trigger at 750 kHz
  - **zero suppression** with programmable corrections for common mode noise and BX-1 pileup
  - **concentrate data** to reduce number of links to back-end
  - **time-analysis of error conditions** to generate and send reset requests to back-end
  - process **extended 41-BX HGCROC event packet** for each L1A ➔ more complex state machines
  - **design and verification more complex than ECON-T**, more susceptible to loss of sync (e.g. via SEE) than ECON-T

- ECON-T latency : 20 BX
- TID tolerance : 200 Mrad
  - Use 65 nm TSMC process, recommended libraries with radiation characterization
- SEE tolerance : 3e6/cm^2/s hadrons with E>20MeV
  - triple modular redundancy for flip-flops, clocks/resets, logic for all configuration and critical state machines
- Low power : ≤5 mW/channel (total ECON-T+D)
  - 65 nm LP TSMC process
  - power optimized design (clock gating)
- Numbers of 1.28 Gbps inputs/outputs
  - 12 inputs, 6-13 outputs
  - (most modules use 1-2 outputs)
- Package
  - 128-pin LQFP



FE architecture for LD silicon