ETROC2 Minor Modifications (at metal layer 2)

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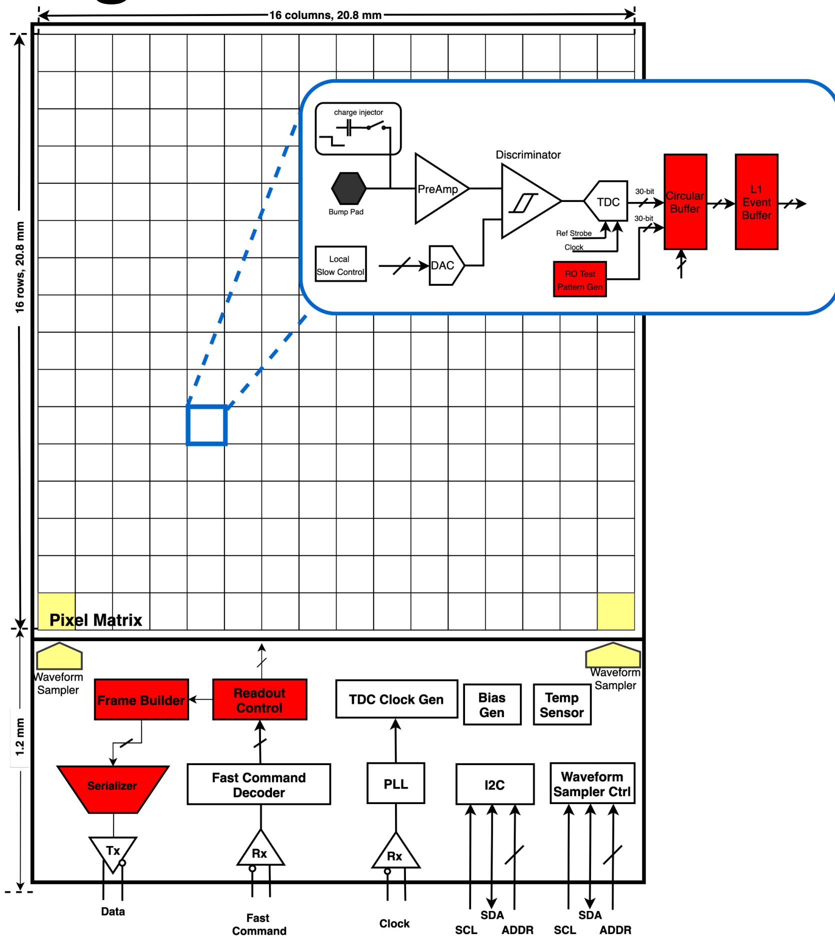
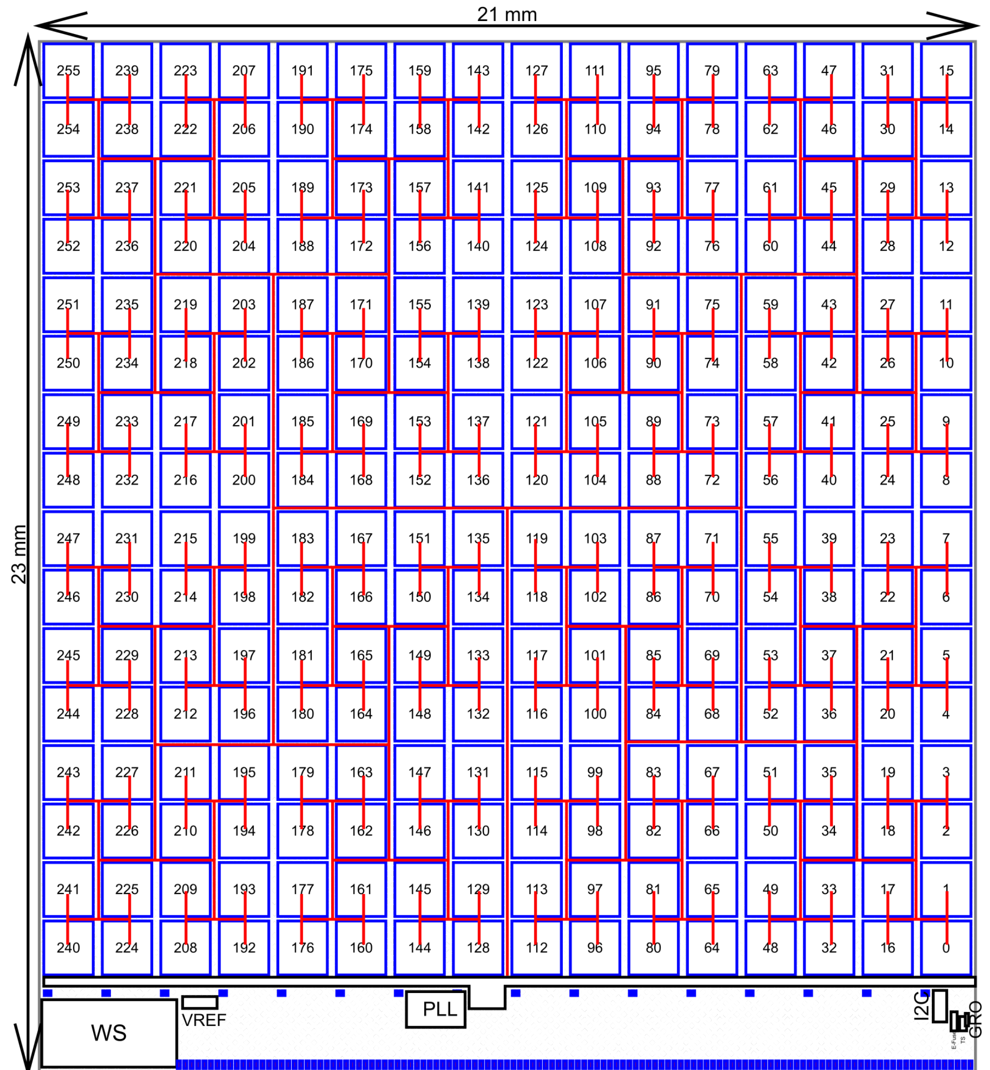
Sep. 11, 2023

Outline

1) Overview of ETROC2.
2) 1st round of minor modifications and its results.
3) 2nd round of minor modifications for the rest of the four wafers on hold at TSMC

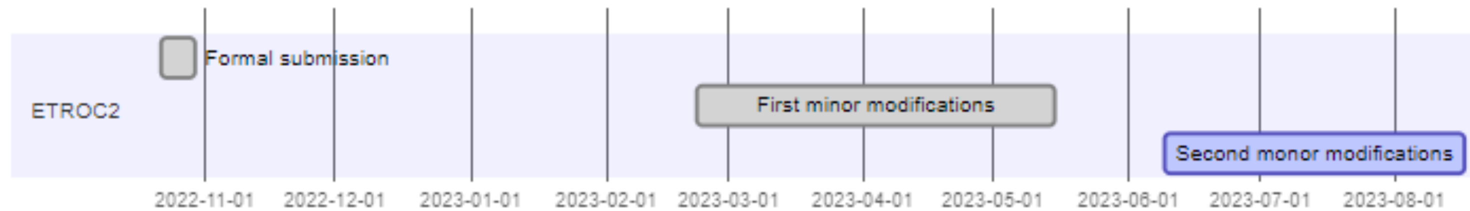
Diagram of ETROC2





ETROC2 is a 16x16 pixels readout chip.

ETROC2 Submission Timeline



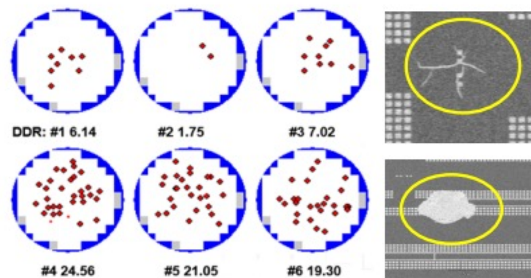
- Oct. 2022, ETROC2 formal submission.
- Feb. 2023 – May 2023, first round (R1) of minor modifications to mitigate the defects caused by the large 'floating' metal layer 3 before the upper layers are built.
- Jun. 2023 – present, second round (R2) of minor modifications for metal layer 2 are ready for submission.

IMEC N65 TMSI07 Skew lot N60R91 Defects Issue

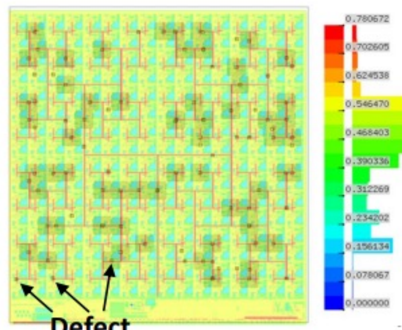
[Slide from TSMC]

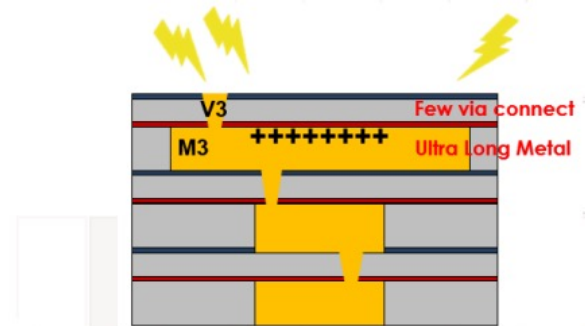
- **Description :** TMSI07 N60R91 found arcing like defect in M4_CMP stage with defect ratio 1.7~24.5%.
- **Investigation :**
  - Inline check : No abnormal process record & confirmed all neighbor products & lots w/o similar defect issue
  - The defects are layout dependency : All defects are located in V3 region with ultra long M3 line
  - ➔ The root cause is suspected Via etch process charging is difficult to release on ultra long metal lines induced arcing defects
  - Leading lot N60R80 w/o defect scan but might suffered similar issue due to it's layout dependency
- **Action :**
  - Since layout dependency can't be covered by process tuning ➔ we will still release wafers for shipping and provide defect map for IMEC ink out
  - Need IMEC help to check layout if long M3 have connection to OD and the OD area for charge release during process for further RTO evaluation

Defect map & images (in M4)



M3 pattern density





→ All Defects are located in ultra-long & high pattern density's M3 metal line

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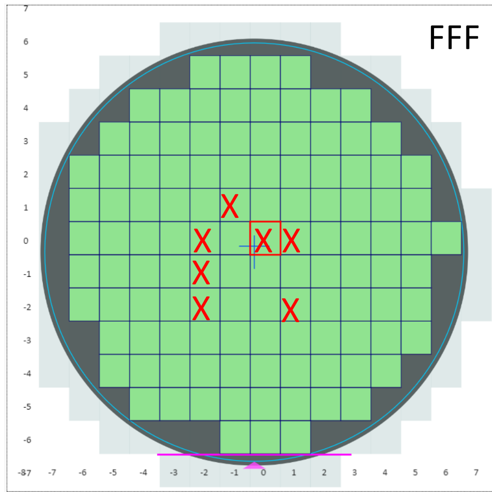

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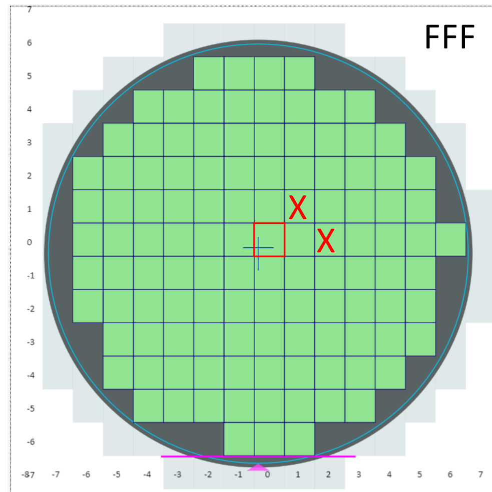

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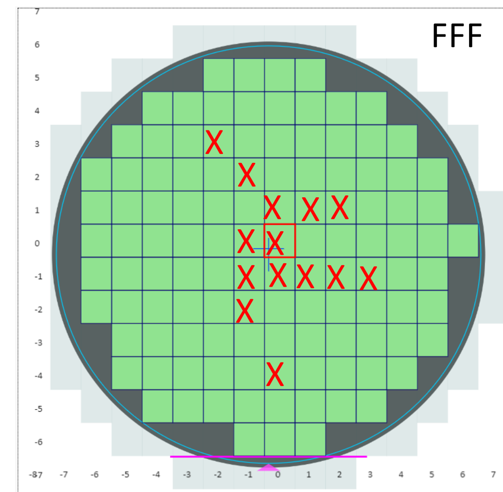
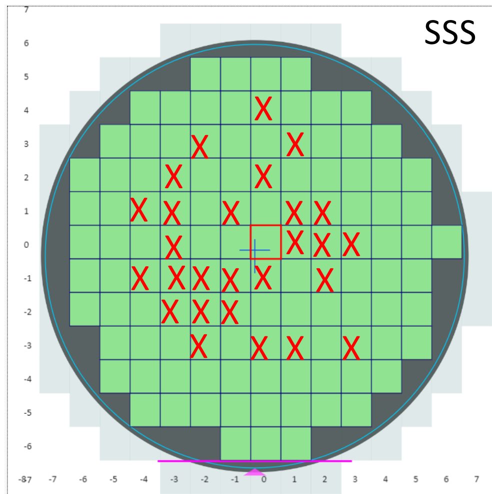


#3

[Slide from TSMC]

Defect map measured by TSMC from the ETROC2 corner lot:
6 wafers,
with
#1/2/3 in FFF corner
and
#4/5/6 in SSS corner



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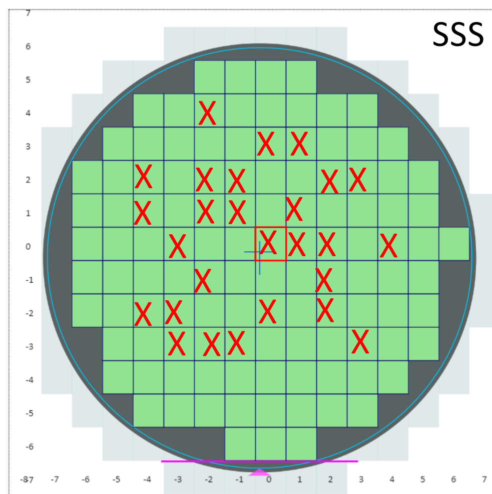

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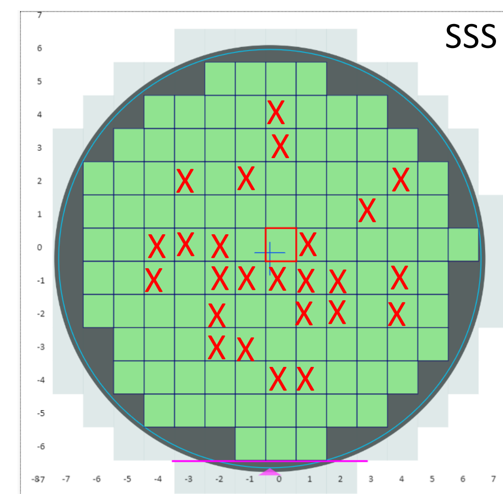
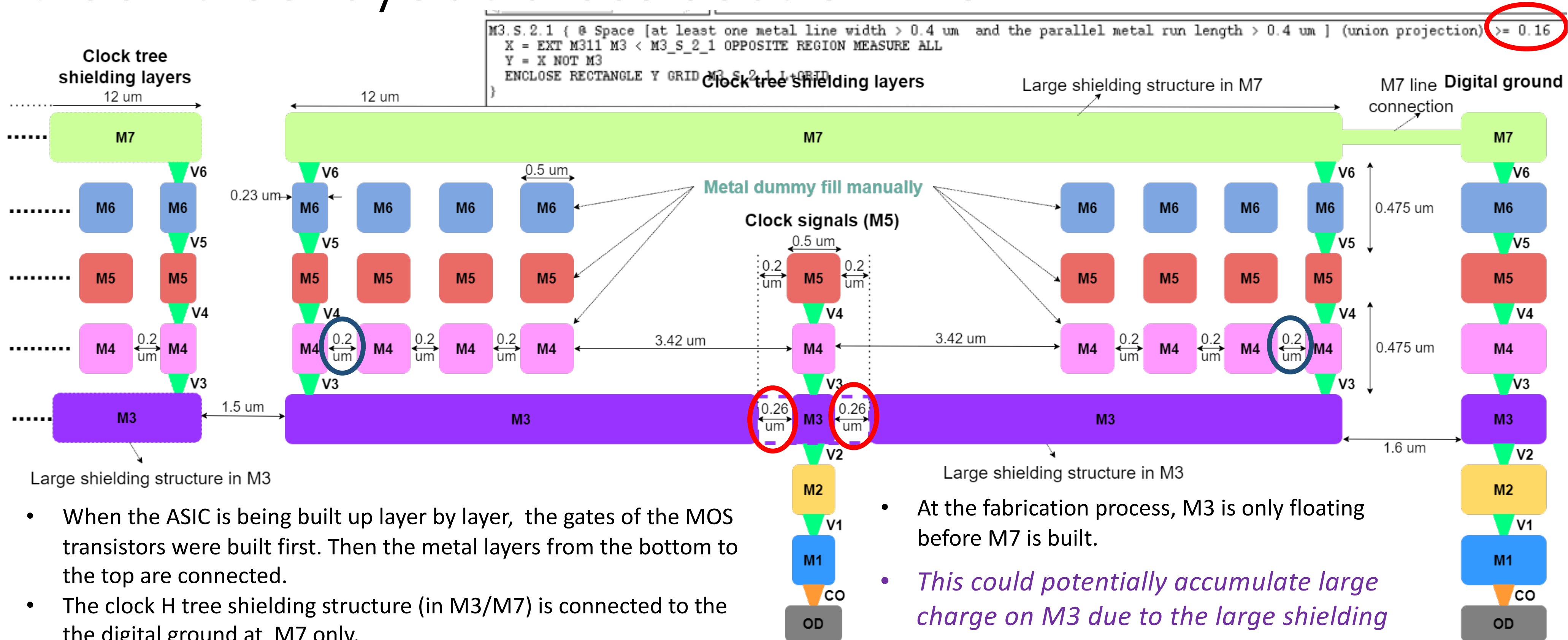


#6

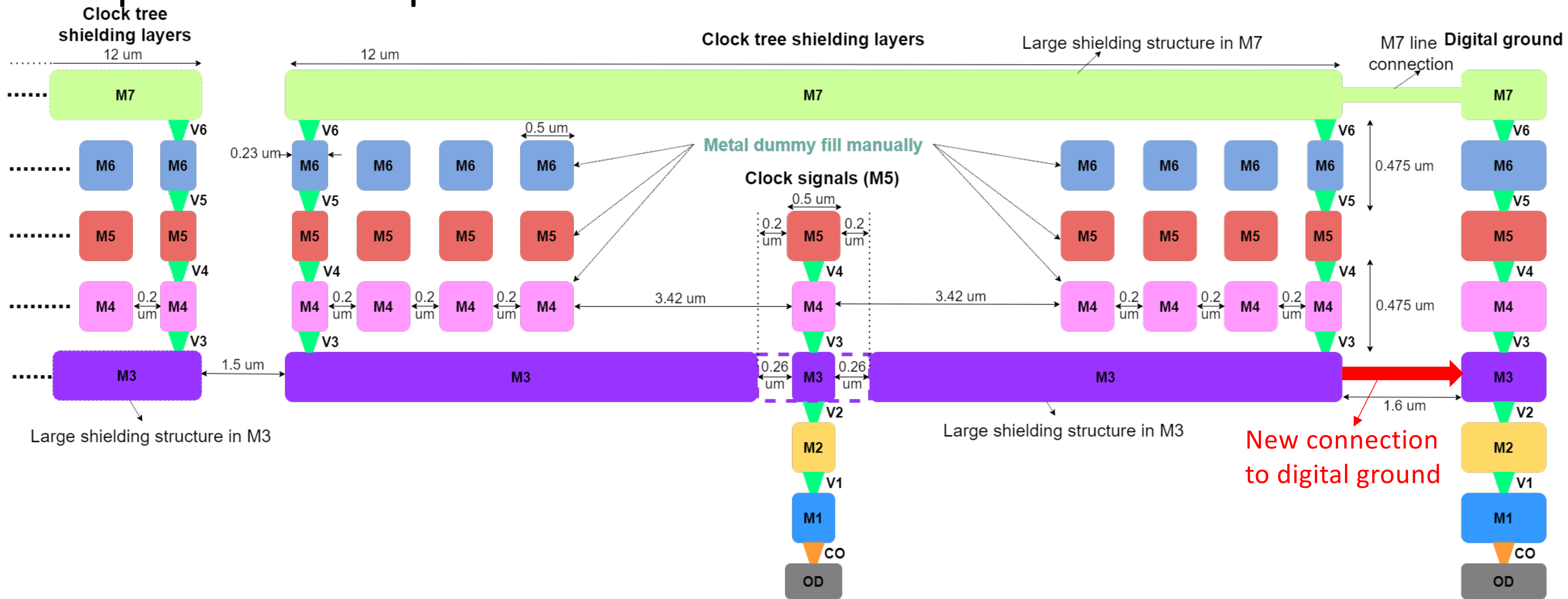
Clock tree layout cross section view



- When the ASIC is being built up layer by layer, the gates of the MOS transistors were built first. Then the metal layers from the bottom to the top are connected.
- The clock H tree shielding structure (in M3/M7) is connected to the the digital ground at M7 only.
- The relatively large shielding in M3 layer would be floating before M7 is built in the fabrication process.
- The minimum space requirement of the wide metal is 0.16 um. To play safe, we use 0.26 um space between M3 of clock signals and M3 shielding.

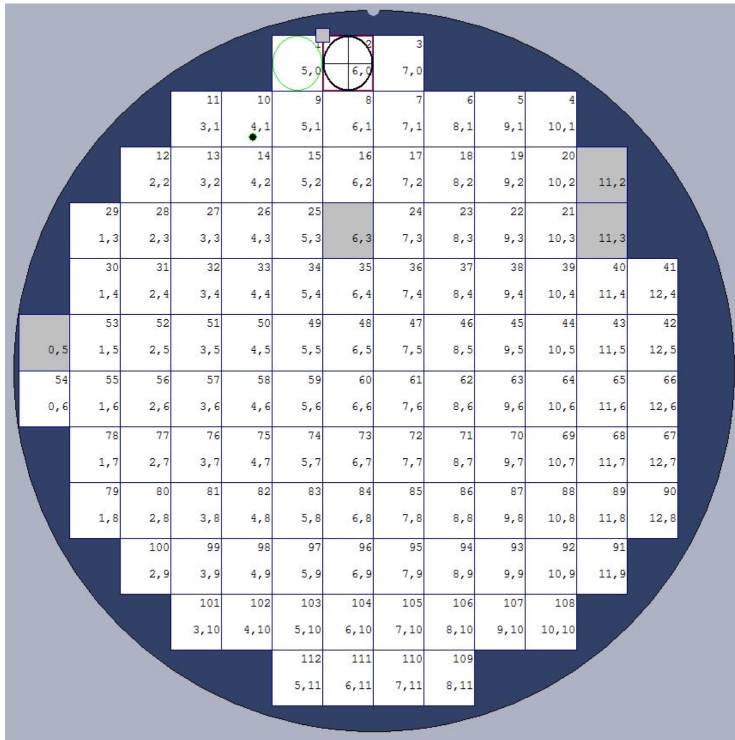
- At the fabrication process, M3 is only floating before M7 is built.
- *This could potentially accumulate large charge on M3 due to the large shielding structure, large enough to possibly cause damage during the fabrication process.*
- *There is no warning on this potential issue by the design tools/rules.*

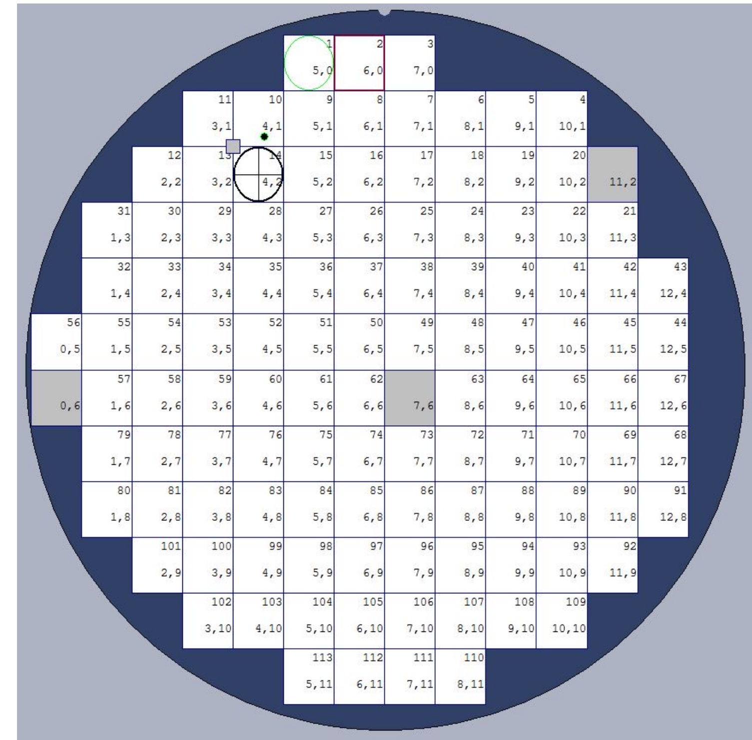
Proposed simple solution



- *The proposed solution is connecting the shielding structures to the digital ground by only updating M3 without modifying other sections, even no via added and no chip dummy fill modified.*
- *All M3 parts should have a connection to OD ground without going through high metals, such during production, the M3 always has a discharge path*

Wafer probing results after R1 minor modifications





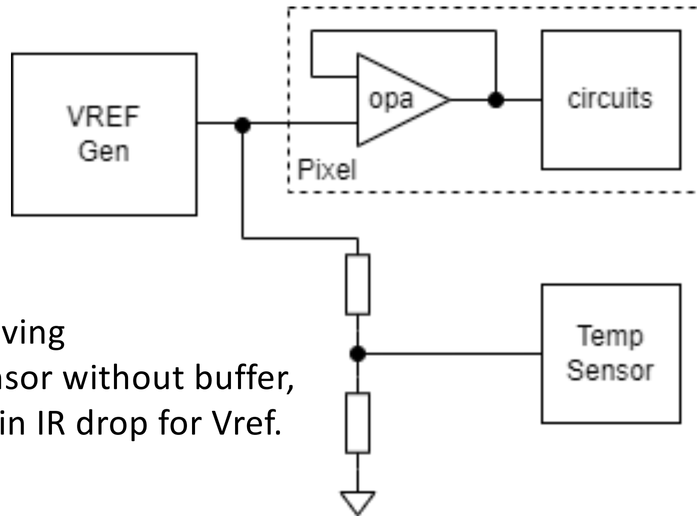
- The yield of the two released wafer at typical corner is 97% after initial test.
- The 1st round of minor modifications addressed the defect and improved the yield significantly.

Outline of R2 minor modifications at metal layer 2

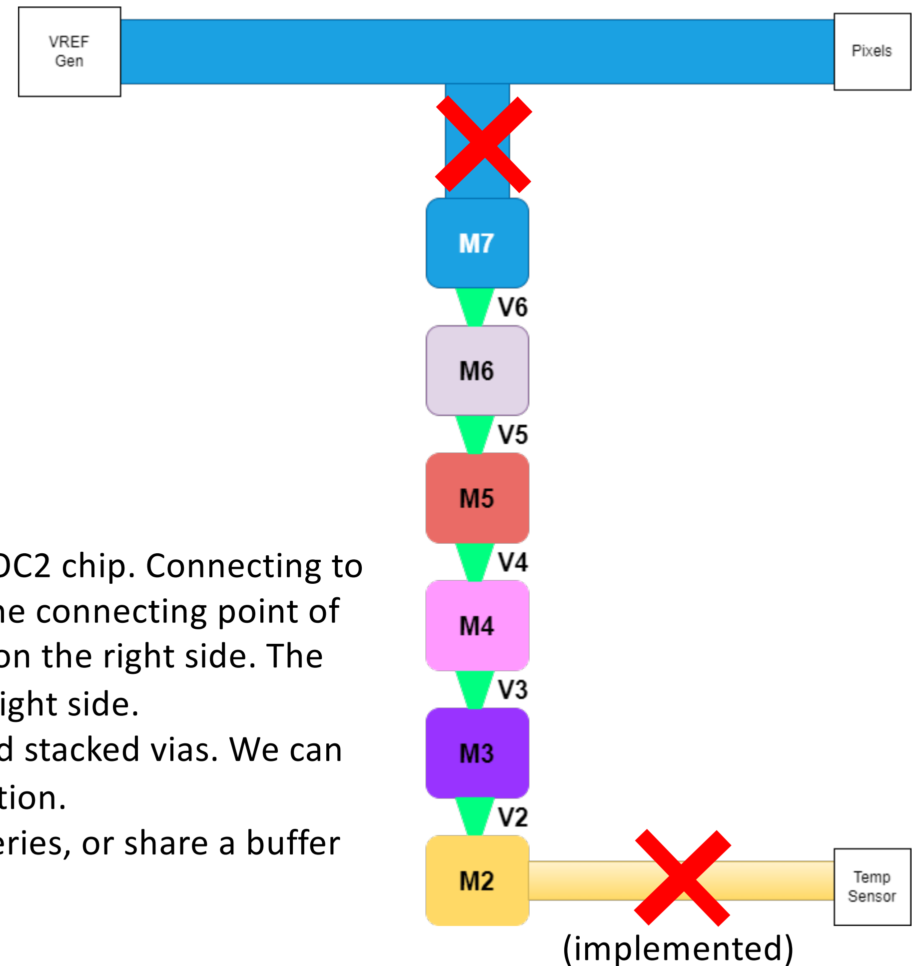
1) Disconnecting the VREF of TS (Temp Sensor).
2) Connecting floating ground net in WS.
3) Change the clock selection for Efuse.

The above three are the known minor issues identified during ETROC2 testing so far

Diagram of Vref distribution and layout connection

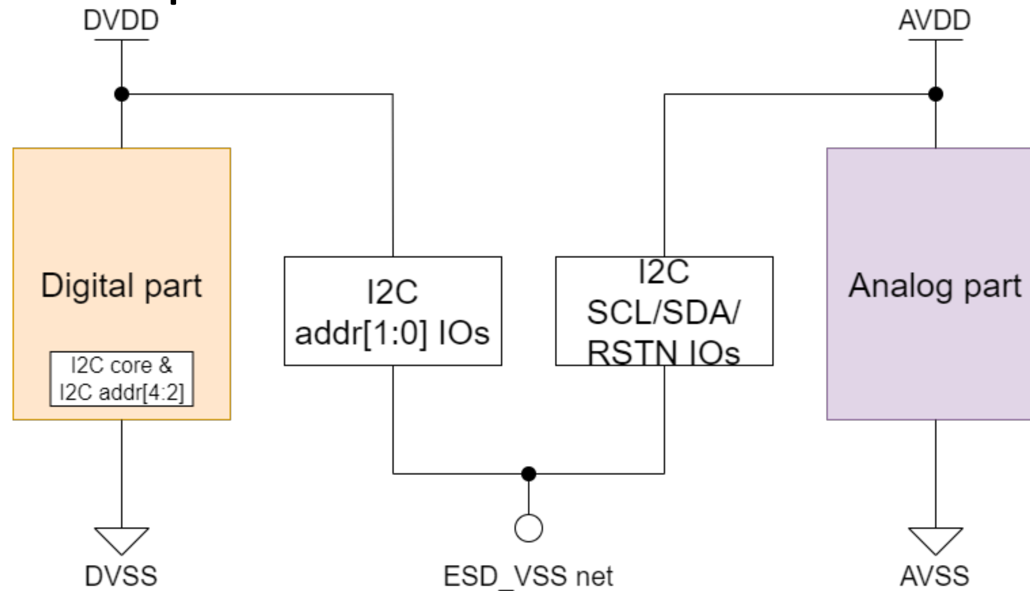


Vref is driving
Temp Sensor without buffer,
resulting in IR drop for Vref.



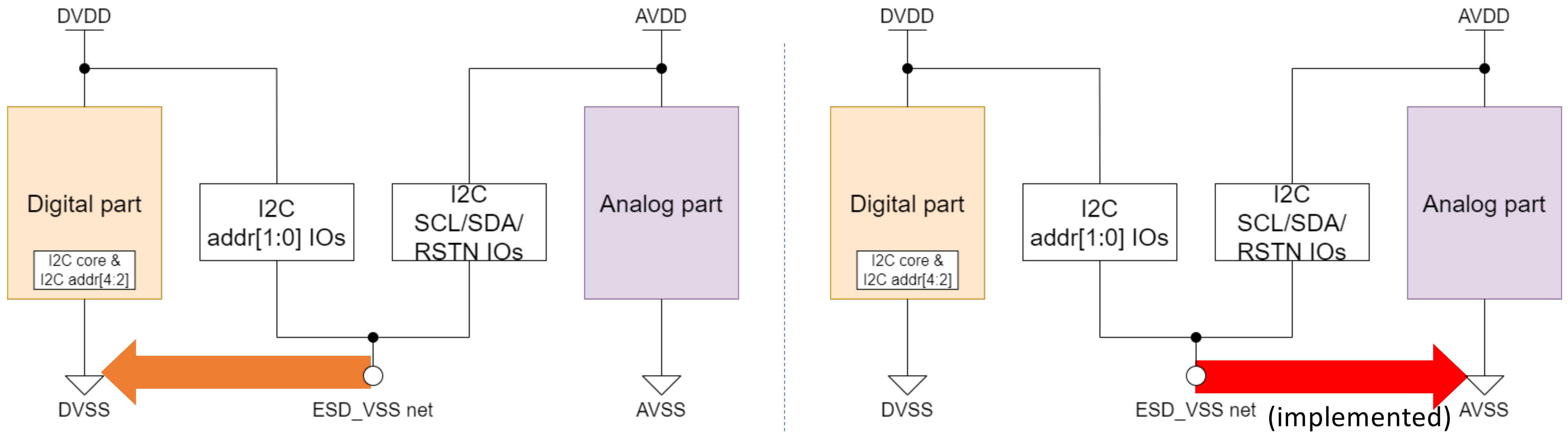
- The VREF generator is in the lower left part of the ETROC2 chip. Connecting to the wide and horizontal metal layer to each column. The connecting point of the wide metal 7 and the Vref input of Temp sensor is on the right side. The cross section of the connecting point is shown on the right side.
- Since the connection using metal layer M7 and M2, and stacked vias. We can cut either metal 7 or metal 2 to disconnect the connection.
- In ETORC3, we can insert a buffer before the resistor series, or share a buffer from one pixel (0, 0) to address this issue.

Diagram of WS power distribution



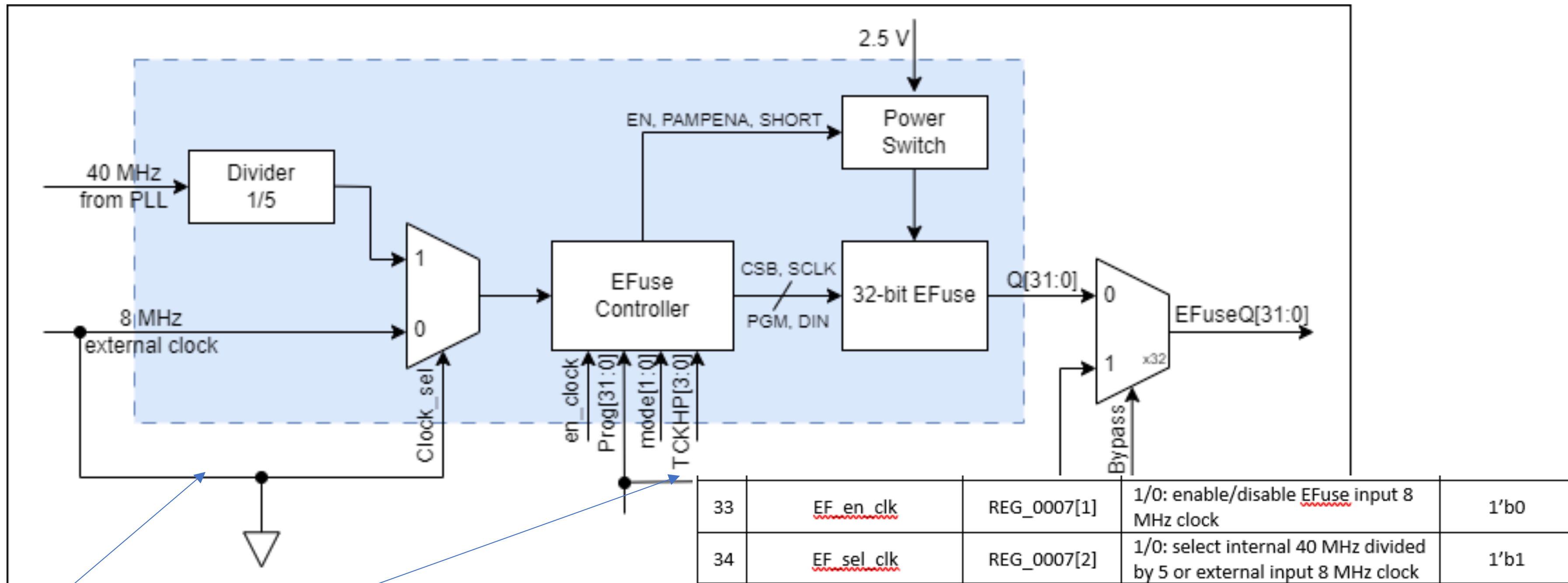
- There are two power domains in WS schematic, digital power domain (DVDD, DVSS) and analog power domain (AVDD, AVSS). The digital and analog powers will be mapped as VDDWSD and VDDWSA on the test board, respectively.
- Digital part includes the digital circuits and digital power pads. The I2C core and the IOs of device address [4:2] are in the digital part. Analog part includes the analog circuits and analog power pads.
- The powers of lower 2-bit I2C address were connected to DVDD. The powers of SCL/SDA/RSTN were connected to AVDD. All the grounds of these 5 pads are connected to the net of ESD_VSS but did not connect to either ground of DVSS or AVSS. This scenario is confirmed in the schematic and layout of WS.

Possible solutions for WS floating ground



- Left diagram shows to connect the ESD_VSS net to the digital ground (DVSS). This solution can be done from metal layer 3 to 6.
- Right diagram shows to connect the ESD_VSS net to the analog ground (AVSS). This solution can be implemented from metal layer 2 to 6.

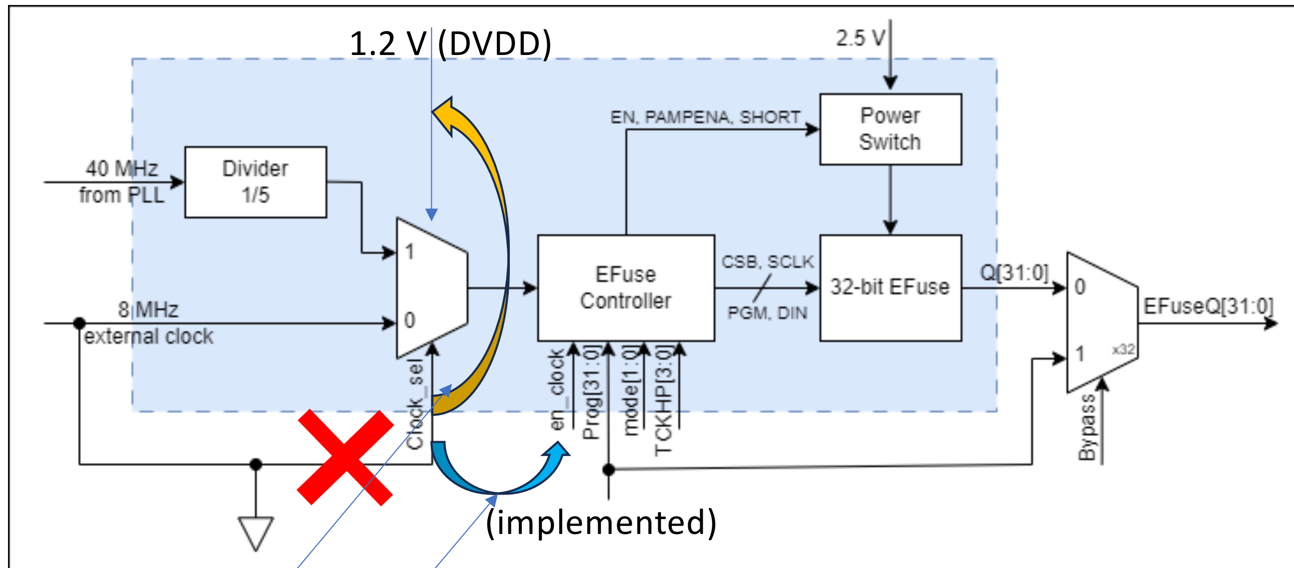
Diagram of Efuse in ETROC2



33	EF_en_clk	REG_0007[1]	1/0: enable/disable EFuse input 8 MHz clock	1'b0
34	EF_sel_clk	REG_0007[2]	1/0: select internal 40 MHz divided by 5 or external input 8 MHz clock	1'b1

- The Efuse in ETROC2 chip is packaged based on the Efuse in ET2-test chip, the original Efuse is the block shown in the blue block above.
  1. pre-set the clock source as the 40 MHz clock from PLL divided by 5.
  2. Adding the bypass operation, if the bypass is enabled the output will be the pre-defined value of Prog[31:0], not the actual value of Efuse.
- In the clock setting, the Clock_sel is tied low with the external clock interface. This causes the external clock is selected as the input clock source which means no clock input to the Efuse controller.

Possible solutions for Efuse clock selection



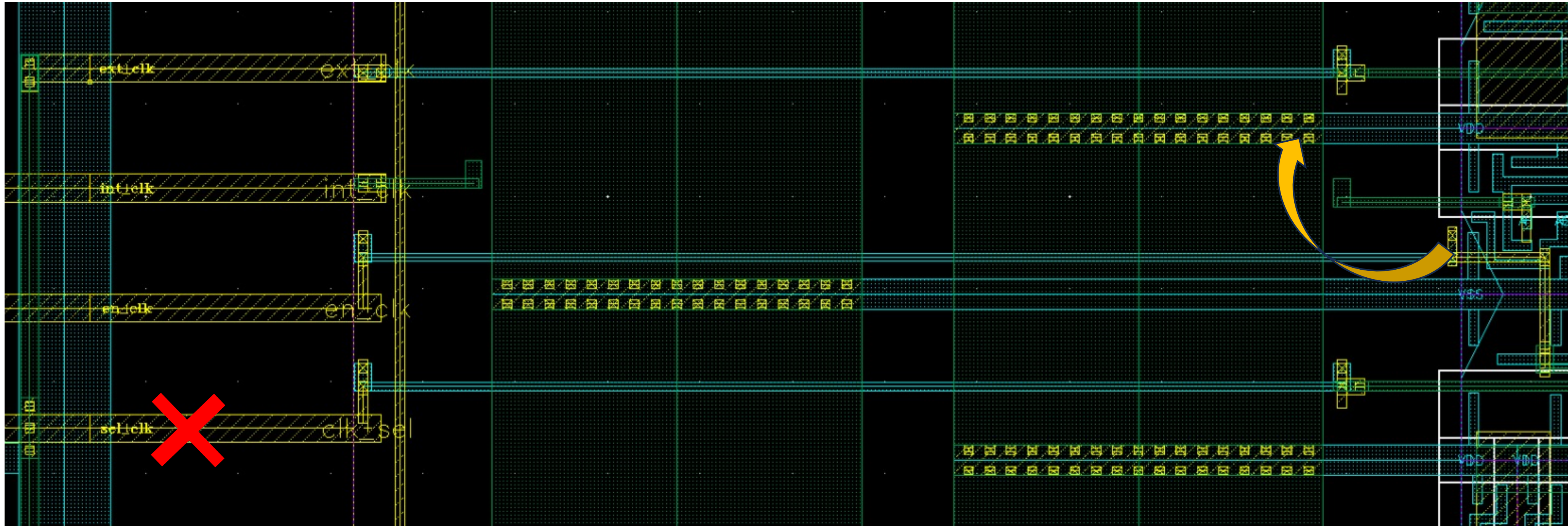
- Disconnect the connection of Clock_sel to the ground (Low), and connect Clock_sel to digital power (DVDD). The Clock_sel will be fixed as logic high to select the internal clock.
- Disconnect the connection of Clock_sel to the ground (Low), and connect Clock_sel to en_clock. En_clock is controlled by I2C, which means if en_clock is enabled (active high), the input clock is using the internal clock. If en_clock is disabled, the clock mux will select external input (ground) which will save power consumption.
- The modifications can be done on metal layer 2.

Summary

- R1 minor modifications on metal layer 3 only addressed the defect during the fabrication process.
- R2 minor modifications on metal layer 2 only are proposed and implemented. The GDS file is ready for submission.
  - These minor modifications will be applied to the 4 wafers still on hold at TSMC

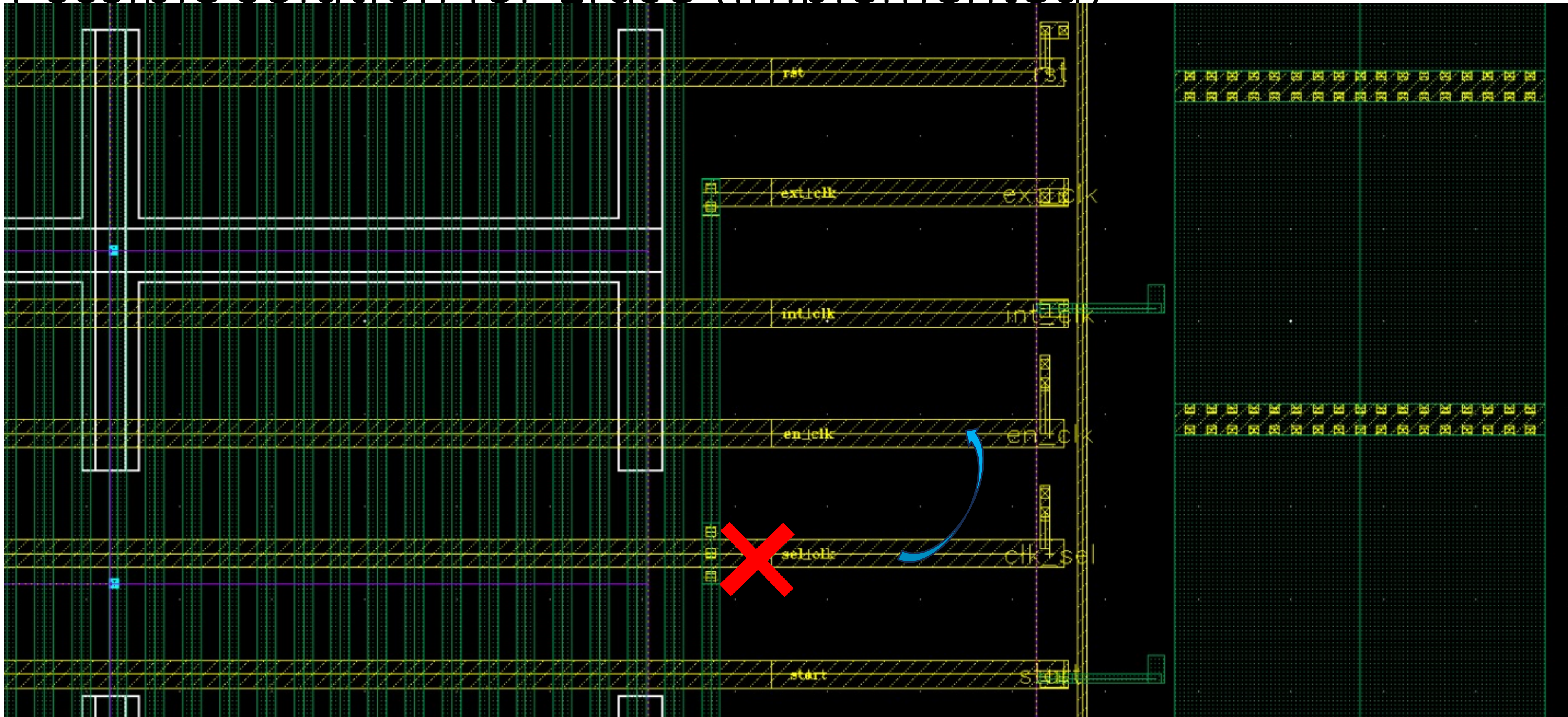
Backup

Possible solution for EFuse



- Disconnect the connection of Clock_sel to the ground (Low), and connect Clock_sel to digital power (DVDD). The Clock_sel will be fixed as logic high to select the internal clock.

Possible solution for Efuse (implemented)



- Disconnect the connection of Clock_sel to the ground (Low), and connect Clock_sel to en_clock. En_clock is controlled by I2C, which means if en_clock is enabled (active high), the input clock is using the internal clock. If en_clock is disabled, the clock mux will select external input (ground) which will save power consumption.

ETROC2_WS_DMY

LVS w/ seal ring

Calibre - RVE v2017.3_38.30 : svdb ETROC2_WS_DMY

File View Highlight Tools Window Setup

Navigator | Info

Results
- Extraction Results
- Comparison Results

ERC
- ERC Results
- ERC Summary

Reports
- Extraction Report
- LVS Report
- Parallel Compare Log

Rules
- Rules File

View
- Info
- Finder
- Schematics

Setup
- Options

Comparison Results

Layout Cell / Type
- peripheryTMR
- PixelCol
- PixelCol1
- ETROC2_WS_DMY
  - Discrepancies
    - Incorrect Ne
      - Discrepa
      - Discrepa
    - Incorrect Ins
      - Discrepa

Cell ETROC2_WS_DMY

LAYOUT NAME

Discrepancy #3 in I

X793/C25739(20990.875

Calibre - RVE v2017.3_38.30 : svdb ETROC2_WS_DMY_sealRingRemoved_forlvsOnly

File View Highlight Tools Window Setup

Search

LVS w/o seal ring

Navigator | Info

Results
- Extraction Results
- Comparison Results

ERC
- ERC Results
- ERC Summary

Reports
- Extraction Report
- LVS Report
- Parallel Compare Log

Rules
- Rules File

View
- Info
- Finder
- Schematics

Setup
- Options

Comparison Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
peripheryTMR	peripheryTMR	0L, 0S	0L, 0S	0L, 0S
PixelCol	PixelCol	0L, 0S	0L, 0S	0L, 0S
PixelCol1	PixelCol1	0L, 0S	0L, 0S	0L, 0S
ETROC2_WS_DMY_sealRingRemoved_forlvsOnly	ETROC2_WS	423880L, 423880S	692271L, 692271S	309L, 309S

Cell peripheryTMR Summary (LVS Box)

peripheryTMR was treated as an LVS Box

ETROC2_WS_DMY chip DRC

Calibre - RVE v2017.3_38.30 : ETROC2_WS_DMY.drc.results

File View Highlight Tools Window Setup Help

Search

Show All ETROC2_WS_DMY, 3048 Results (in 9 of 13 Checks)

Check / Cell	Results	Flat
Check MOM.R.1	27	544
Check DRM.R.1	1	1
Check PO.R.1	1000	353126
Check PO.R.4	1000	55771
Check M8.DN.4	2	2
Check M9.DN.2	11	11
Check RM.WARN.2	1000	6980
Check LUP.1g	6	144
Check ESD.WARN.1	1	1
Check DENSITY_PRINT_FILES	0	0

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27

```
MOM.R.1 { @ Poly shielding and underneath NW or PW must bias at same potential for reliability consideration. If poly shielding terminal could not be tied to the underneath NW or PW, customer should keep bias between poly terminal and underneath well within thin gate oxide (Without OD2) or thick gate oxide (With OD2) maximum applied voltage for reliability consideration.
@ DRC only check following conditions:
@ (1) {(MOM_PO INTERACT (MOM_OD NOT INSIDE OD2)) INTERACT ((MOMDMY(155;100) OR MOMDMY(155;0)) NOT (MOMDMY(155;27))} [Poly shielding MOM with dummy OD underneath] and underneath NW or PW must bias at same potential through metal connection.
MOM_OD = COPY ODi
PO_MOMi = (ILP1i INTERACT (MOM_OD NOT INSIDE OD2)) INTERACT ((MOMDMY OR MOMDMY_100) NOT MOMDMY_2T)
NW_NOT_POi = NWi NOT PO_MOMi
PW_NOT_POi = PWELi NOT PO_MOMi
EXT PO_MOMi NW_NOT_POi < 0.001 ABUT == 0 NOT CONNECTED REGION
EXT PO_MOMi PW_NOT_POi < 0.001 ABUT == 0 NOT CONNECTED REGION
}
```

Check MOM.R.1

ETROC2_WS_DMY chip DRC mim_ant

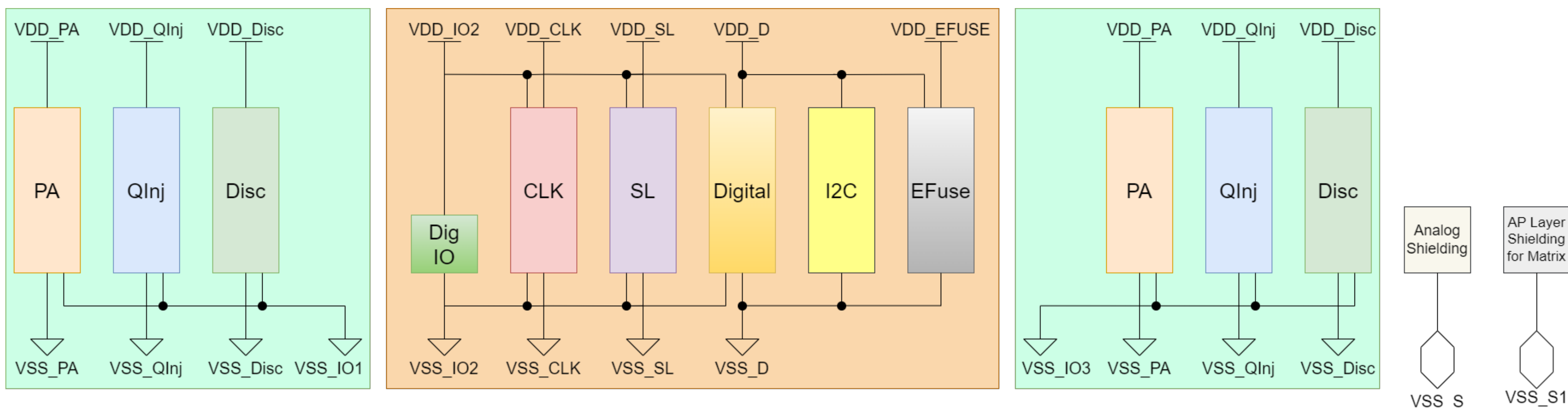
File View Highlight Tools Window Setup Help

Search

Show All
No Results Found

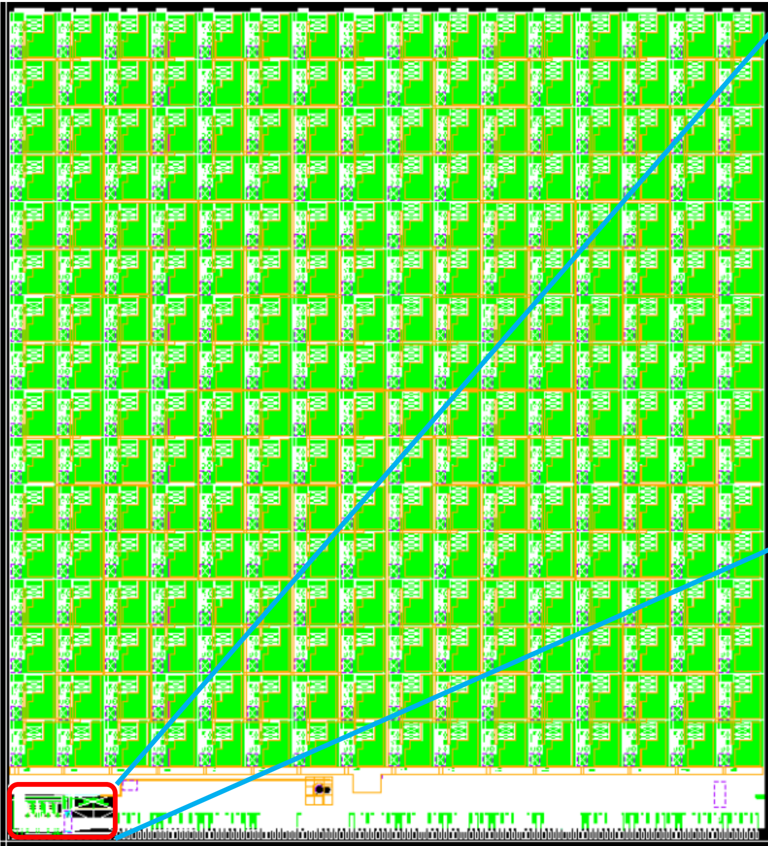
Check / Cell | Results

Diagram of ETROC2 power distribution

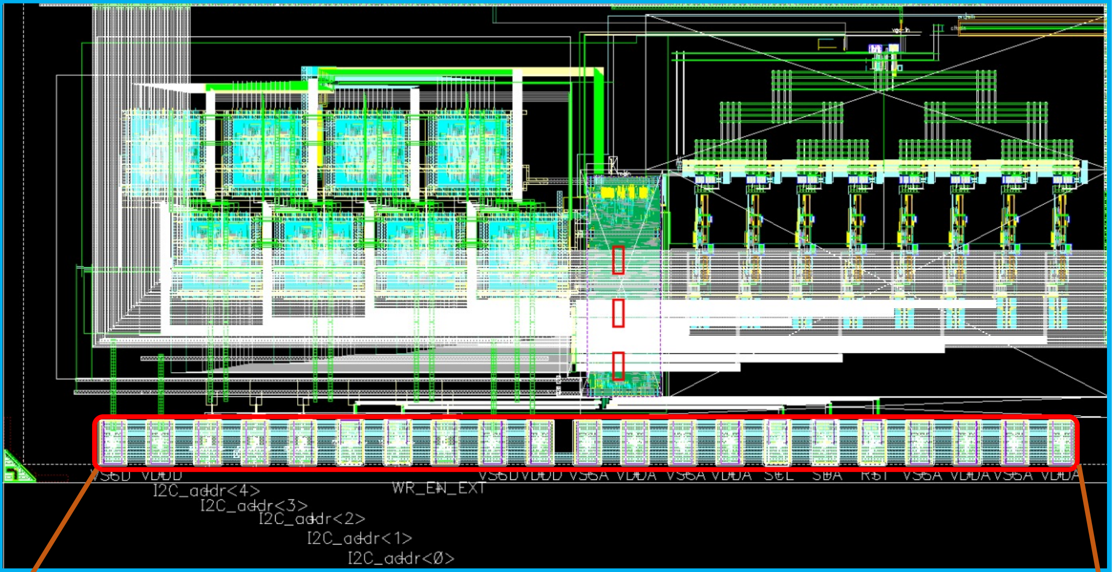


- Considering the locations of the PLL and the globalDigital are in the middle part, the IOs are divided into 3 sections, the left analog IOs, the digital IOs in the middle, the right analog Ios.
- Independent power supplies of pre-amplifier (PA), charge injection (Qinj), discriminator (Disc), clock generator (CLK), serial link (SL), digital part (Digital). Digital part includes readout, I2C, EFuse, etc. Efuse needs a 2.5 V power supply only for the EFuse programming.
- For the analog IOs, extra analog grounds (VSS_IO1, VSS_IO3) are needed for the IOs in each section. VDD_IO2 and VSS_IO2 are provided for the digital IOs.
- In addition, VSS_S is the IO with 3 pads connected to the shielding structure for the analog part in each pixel. An VSS_S1 is a pad employed to connect the AP shielding layer on the top of pixel matrix.

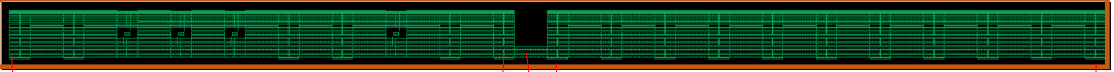
Layout of WS in ETROC2



WS layout



Digital power domain on metal layer 3



Digital power domain

Analog power domain

Ground for the signals of WS I2C pads (float)

- There are two power domains in WS, digital power domain (DVDD, DVSS) and analog power domain (AVDD, AVSS).