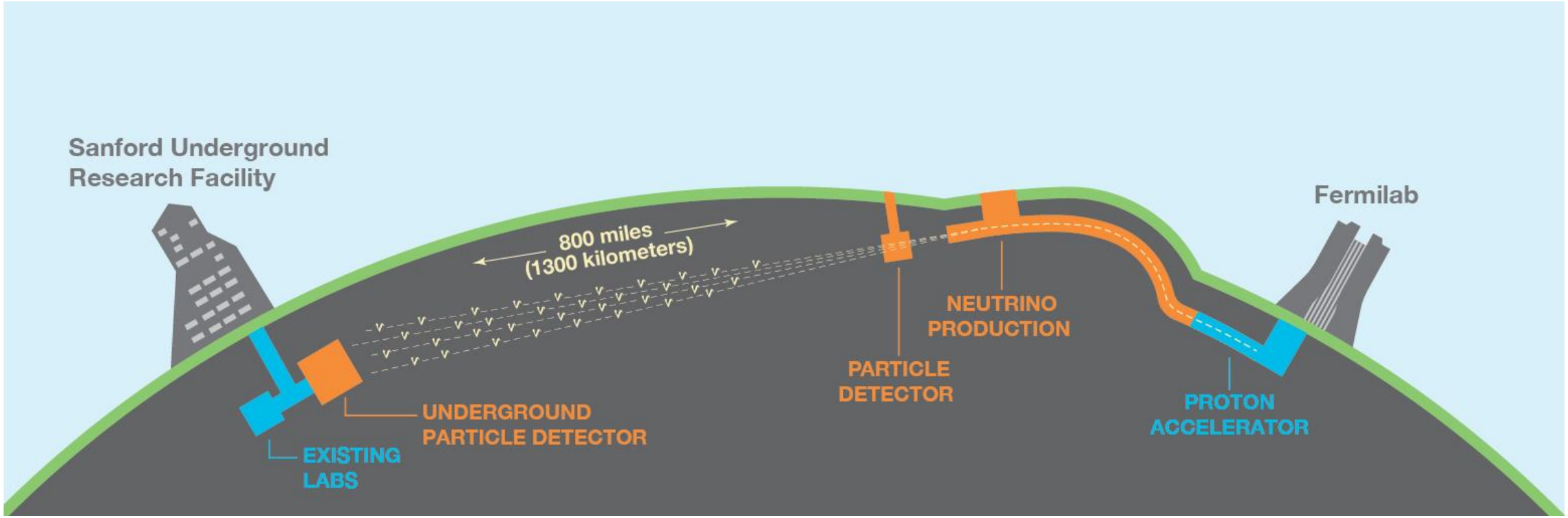
High-performance test bench for the automation of DAPHNE board minimum performance tests

Fabian Castaño (On behalf of the UdeA DUNE members)

NuCo 2023

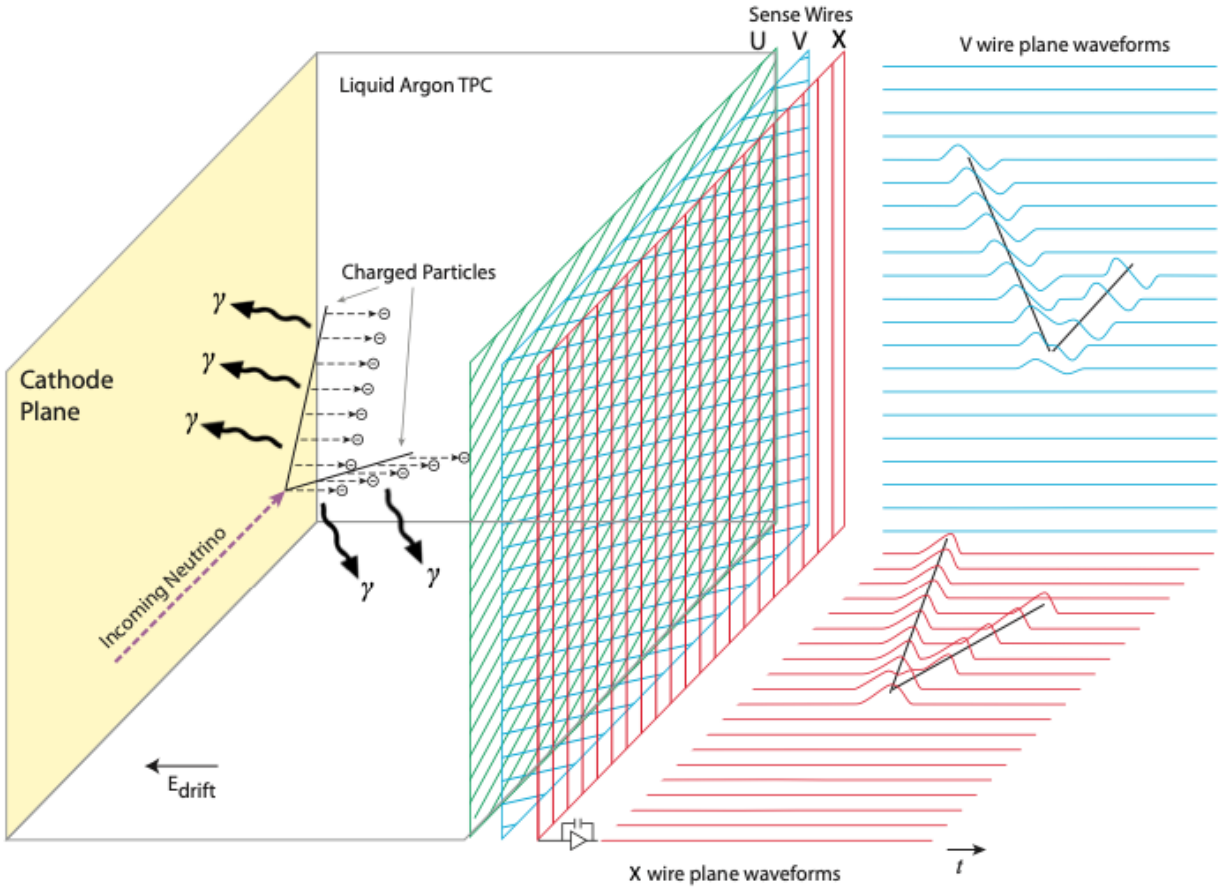
30 September 2023

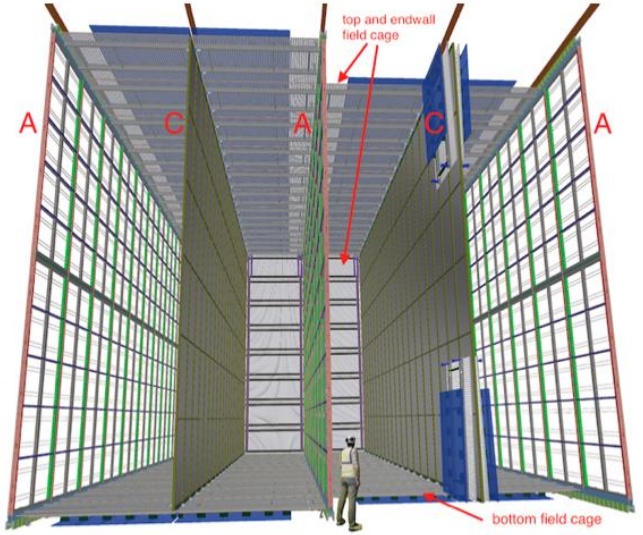
What is DUNE?



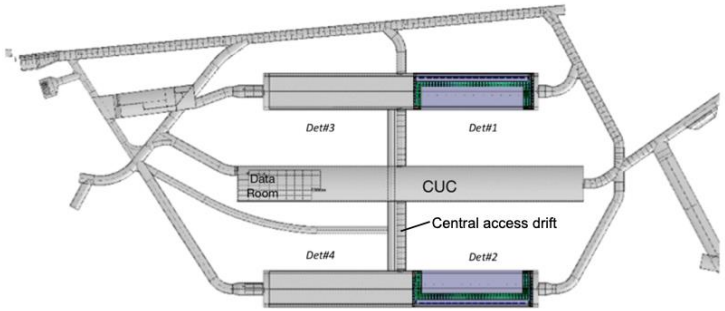
- Investigate Neutrino oscillation to prove charge parity violation (CP)
- Determine the order of the mass of the neutrinos
- Study supernovae, the formation of neutron stars and black holes

Far Detector (FD)





65.8 m (L) by 18.9 m (W) by 17.8 m (H)

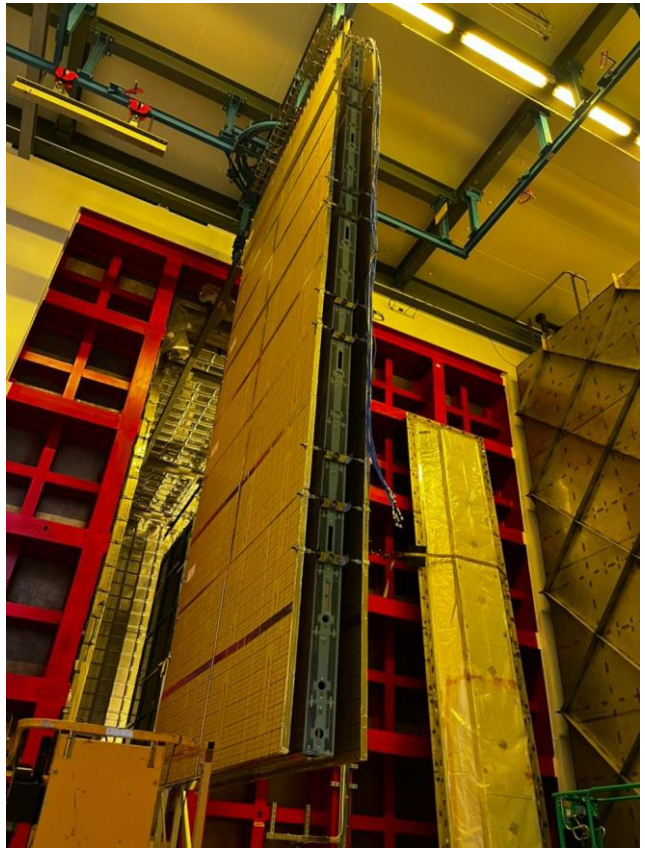


B. Abi, R. Acciarri, M. Acero, G. Adamov, D. Adams, M. Adinolfi et al., Volume IV. the DUNE far detector single-phase technology, Journal of Instrumentation 15 (aug, 2020) T08010–T08010.

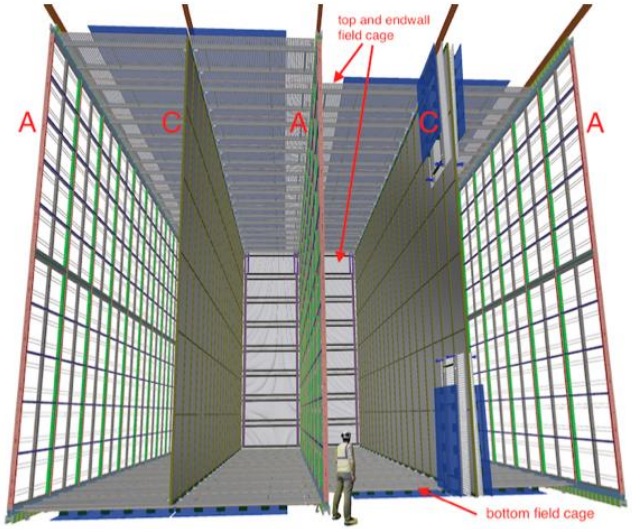
Horizontal and Vertical Drift

- ProtoDUNE-2

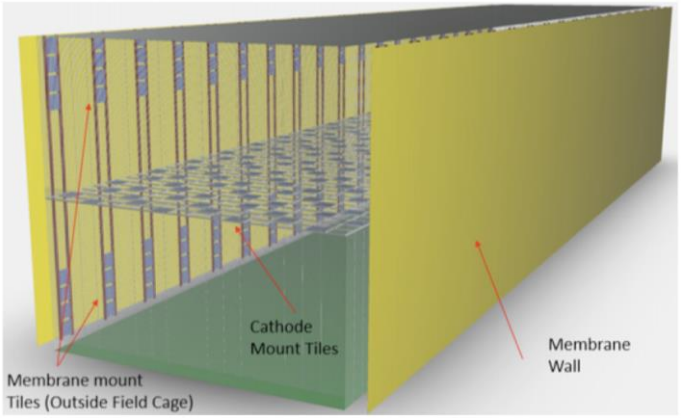
  Prototype Experiment built in CERN (Geneva, Switzerland)



HD

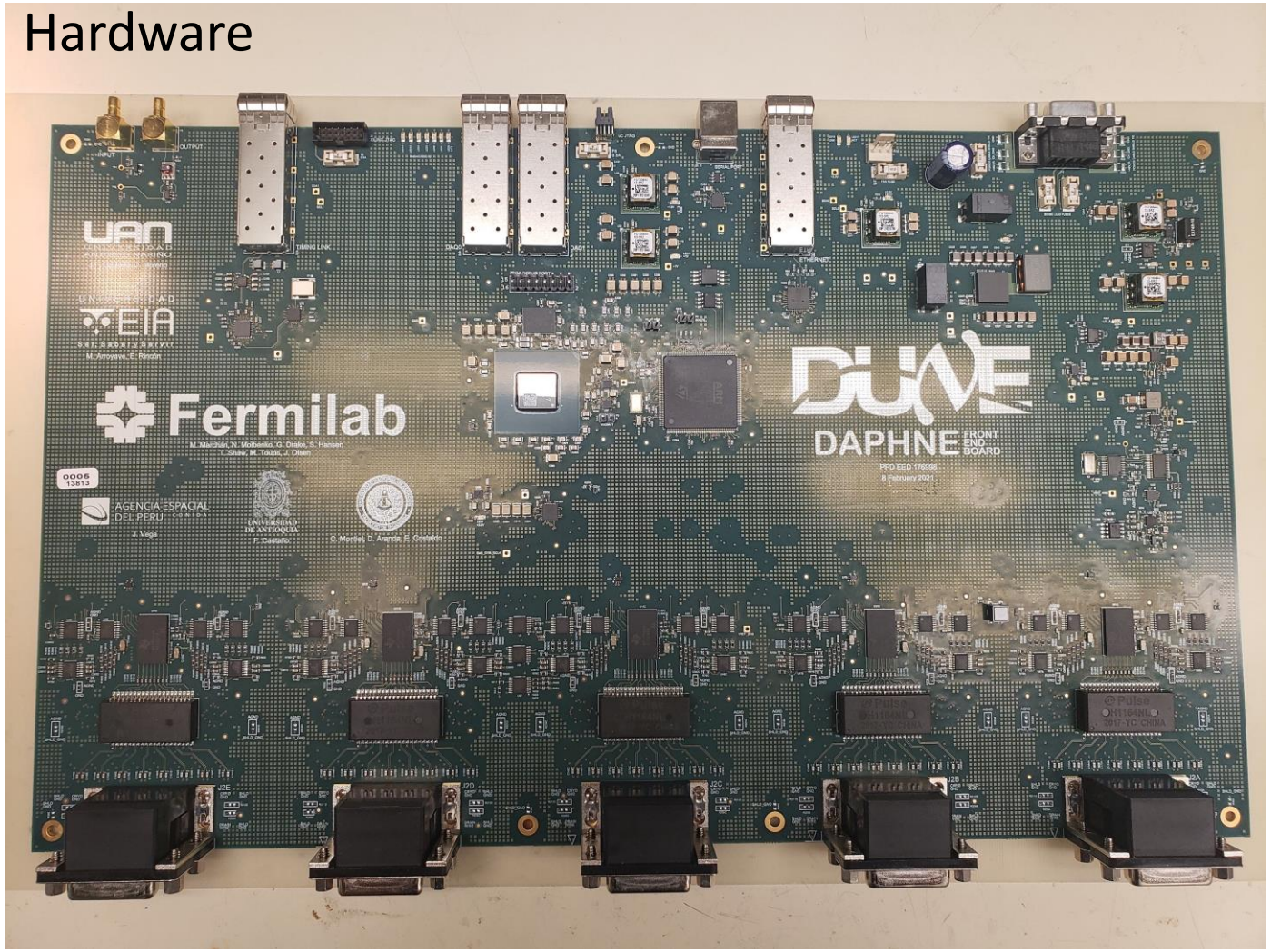


VD

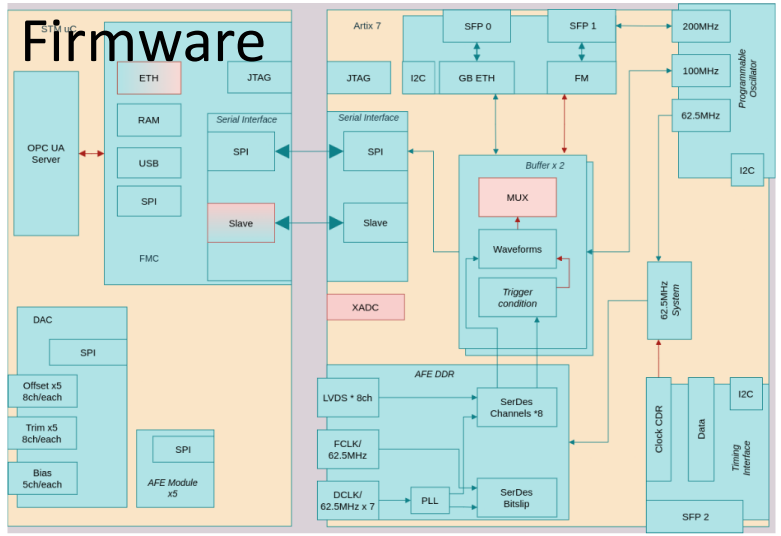


DAPHNE V1 and V2A

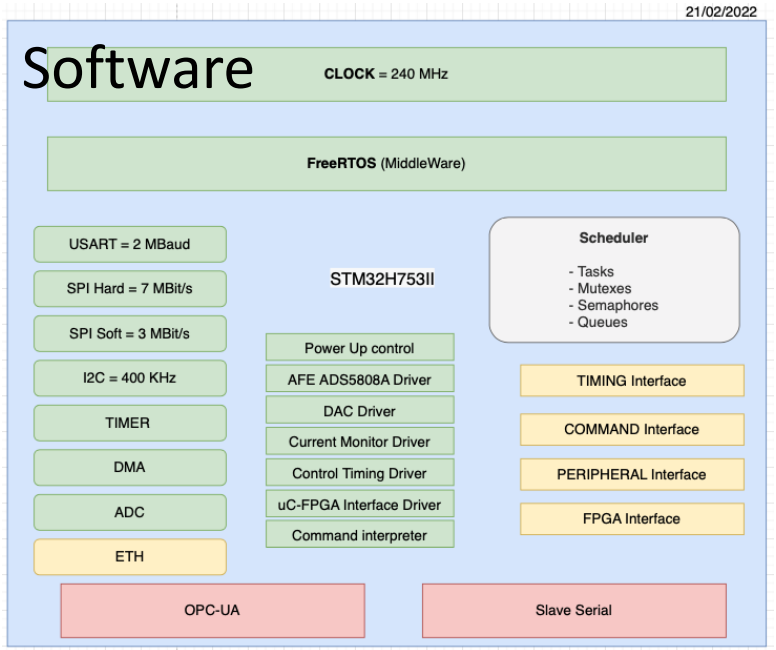
Hardware



Firmware



Software

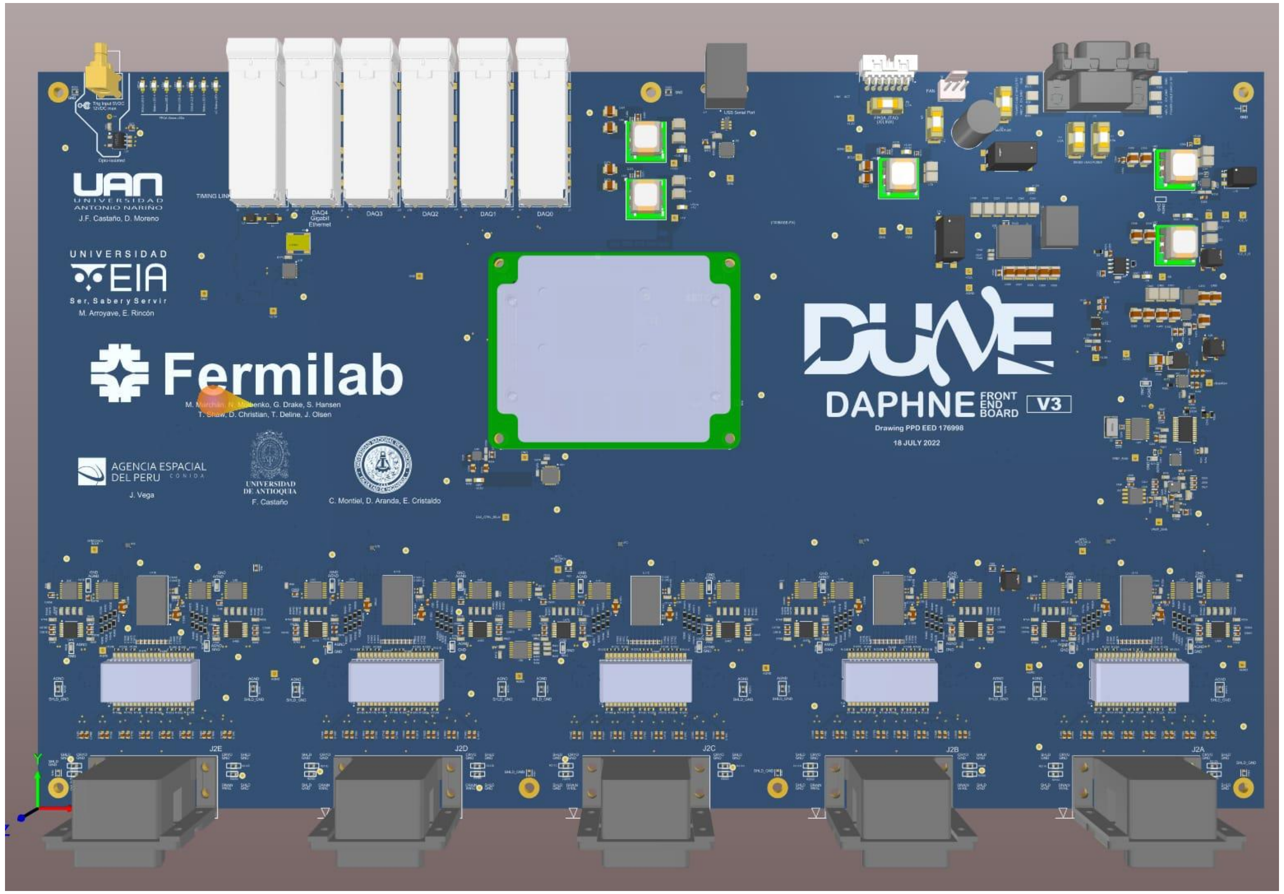


DAPHNE V3

- Kria KR260 – DAPHNE V3

  Design of new architecture for Photon Detection System

  - Acquisition of development boards for the collaboration

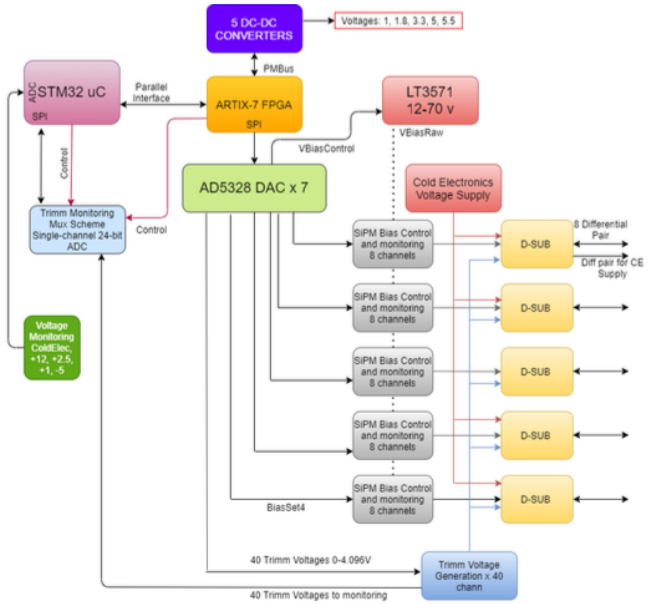


https://github.com/fabioc9675/KRIA_Starter_Guide/blob/documentation/Tutorial/T01_Kria_and_Vivado.md

Challenges (Operation and Diagnosis)

- It is necessary to implement an automatic test.
- Manual test:
  - A lot of time
  - Reprocessing
  - Non-standardization
  - Possible failures
- Automatic test:
  - Better performance
  - Multiple evaluation simultaneously
  - Standardization
  - Traceability.

VOLTAGE GENERATION AND MONITORING

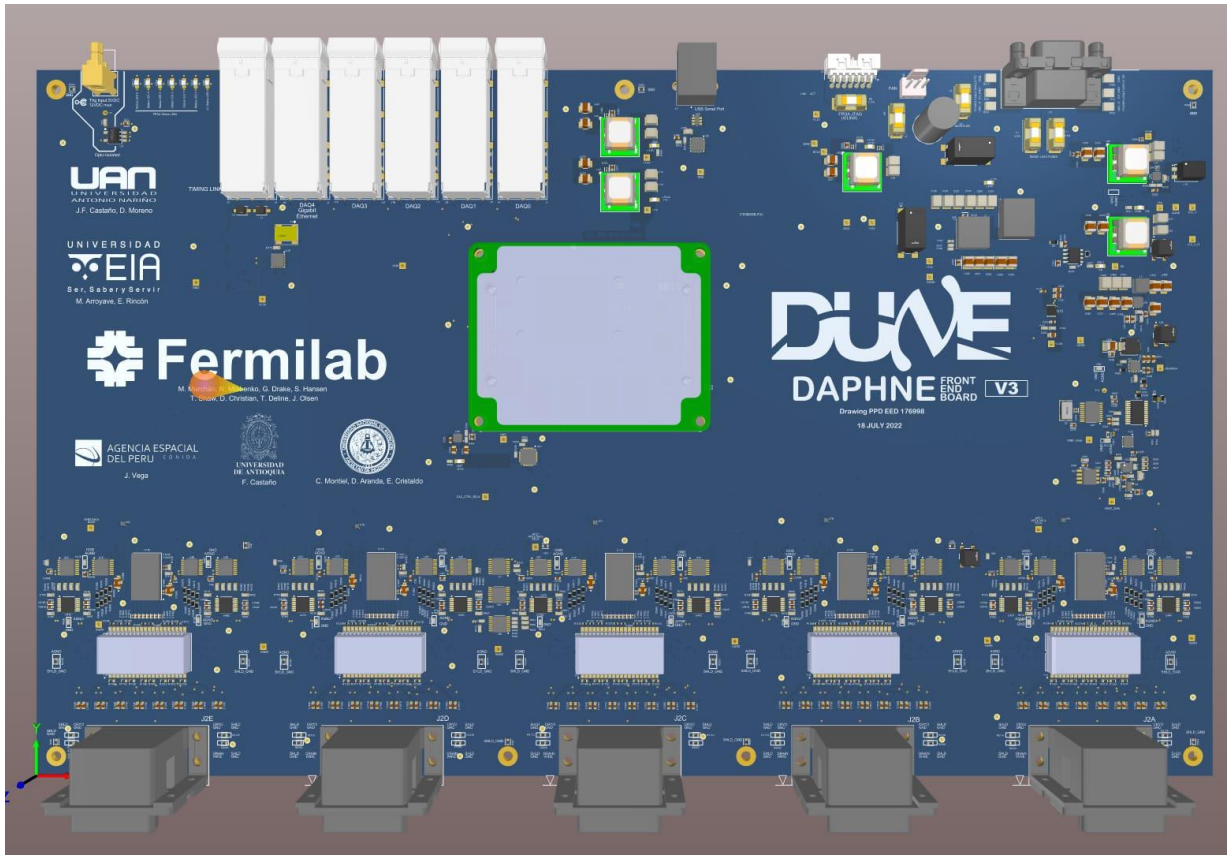


Voltage/Parameter	Bias Raw	SiPM Bias	Trimm
Range (V)	12-70	0 V-BiasRaw	0-4.096
Generated by	DC-DC Boost Converter	Custom Circuit	DAC+custom circuit
Adjusted by	FPGA/12 bits DAC	FPGA/12 bits DAC	FPGA/12 bits DAC
Adjustment Precision	14,16 mV (for BiasRaw=70 V)	14,16 mV	1 mV
Generated for	General	8 channels, 5 groups	Individual channel

Also, can be used to do diagnosis and evaluation of performance in real time

Institutional Goals

- To define of minimum operating requirements and testing protocol.
- To design and manufacturing an electronic test bench board system.
- To evaluate and validating the test bench performance.
- To evaluate the performance of a DAPHNE board using the test bench.

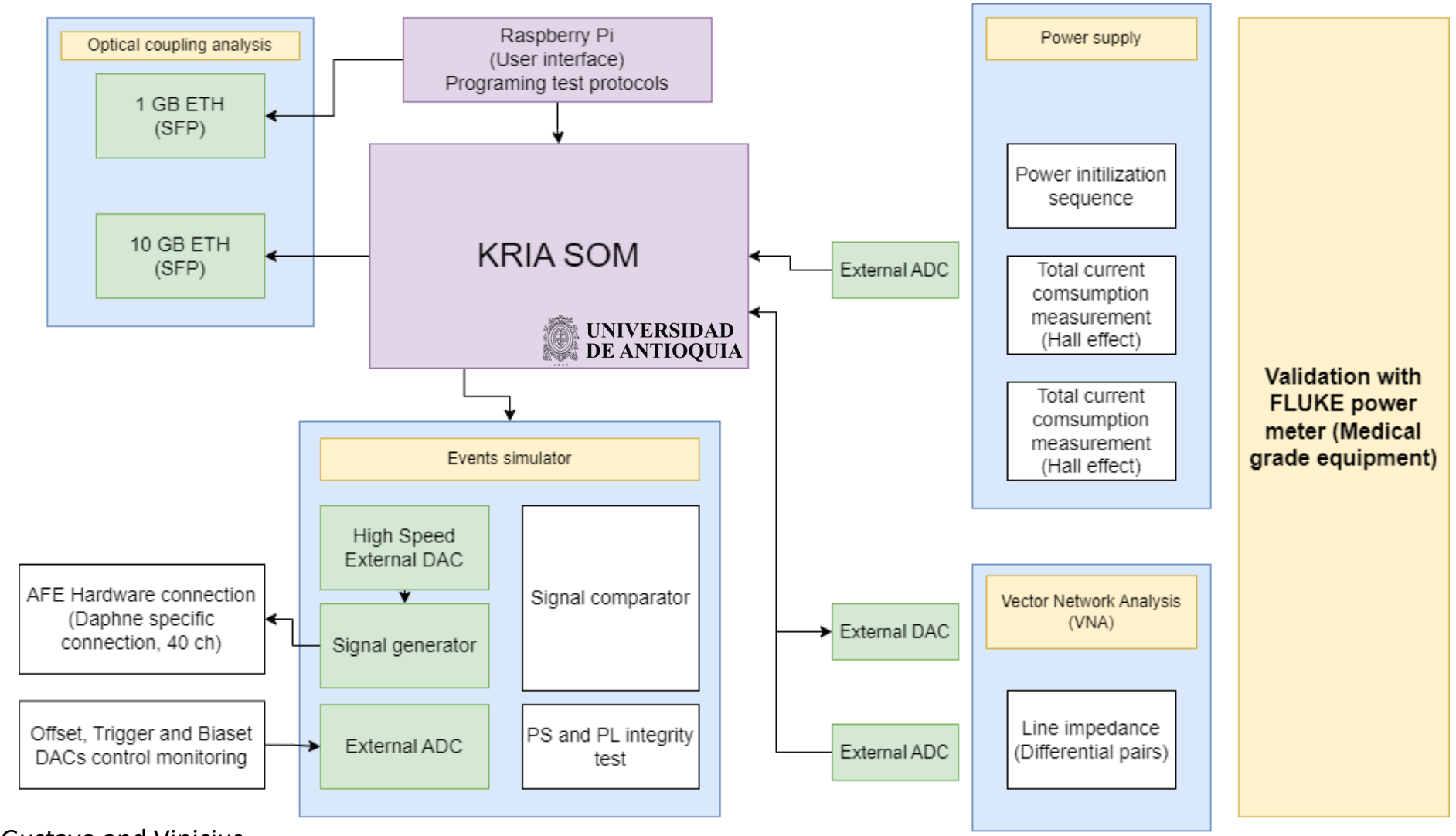


Use the test bench infrastructure to simulate hardware event signals and assess the performance of the DAPHNE board.

Proposed technical tests

- **Operating voltage test:** Verify the board operation under specified voltages.
- **Board impedance test:** Evaluate signal integrity, power distribution and high-frequency performance.
- **Digitizing systems (AFEs) test:** Validate the AFE's performance, linearity, noise levels, dynamic range, and overall fidelity in digitizing signals from various sources.
- **PL operation (Fast DAQ) test:** Timing accuracy, synchronization capabilities, data integrity, and overall system throughput.
- **Signal conditioning test:** Gain, frequency response, linearity, noise levels, distortion, and impedance matching.
- **PS operation (Slow control) test:** Reliability, responsiveness, and accuracy in performing slow control tasks, such as adjusting settings, configuring parameters, or managing system states.

Test bench architecture



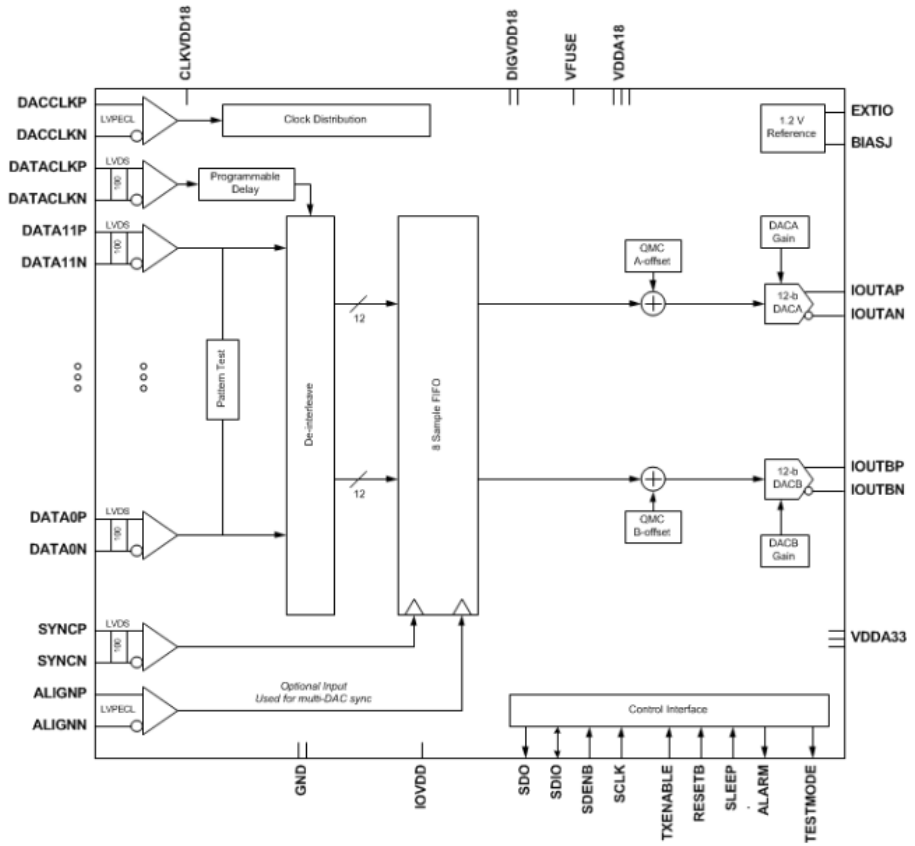
Cooperation with Gustavo and Vinicius

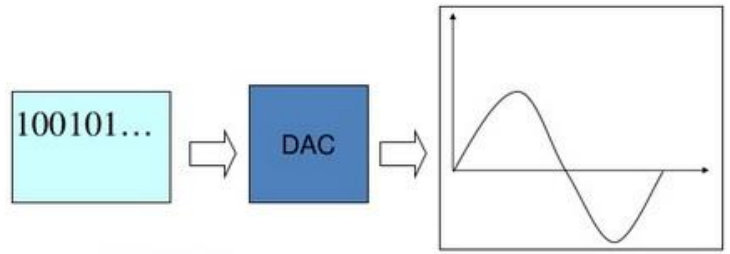
Test bench as event signal simulator

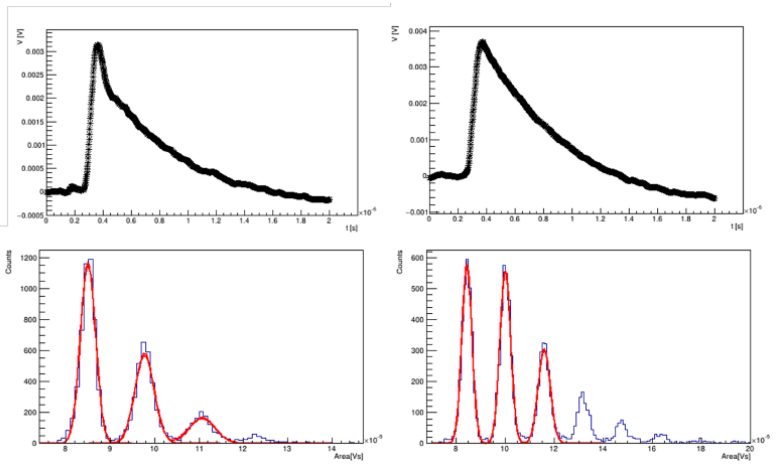
DAC3154 ACTIVE

https://www.ti.com/product/DAC3154

Dual-channel, 10-bit, 500-MSPS digital-to-analog converter (DAC) with input FIFO and current sour



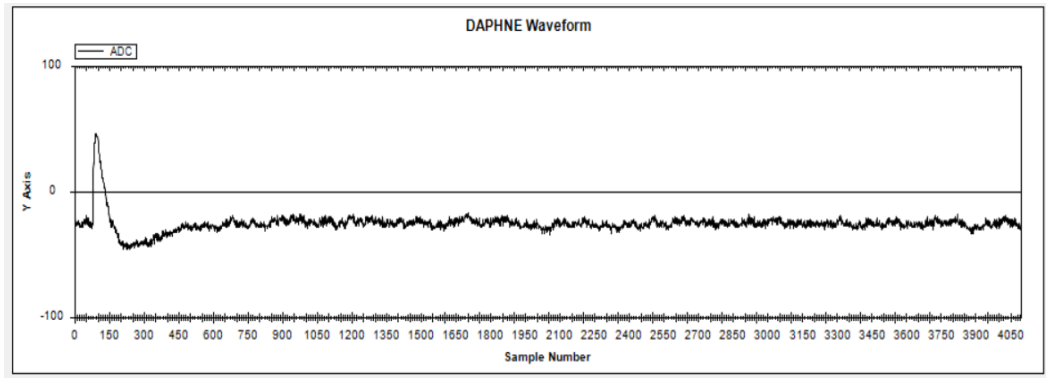


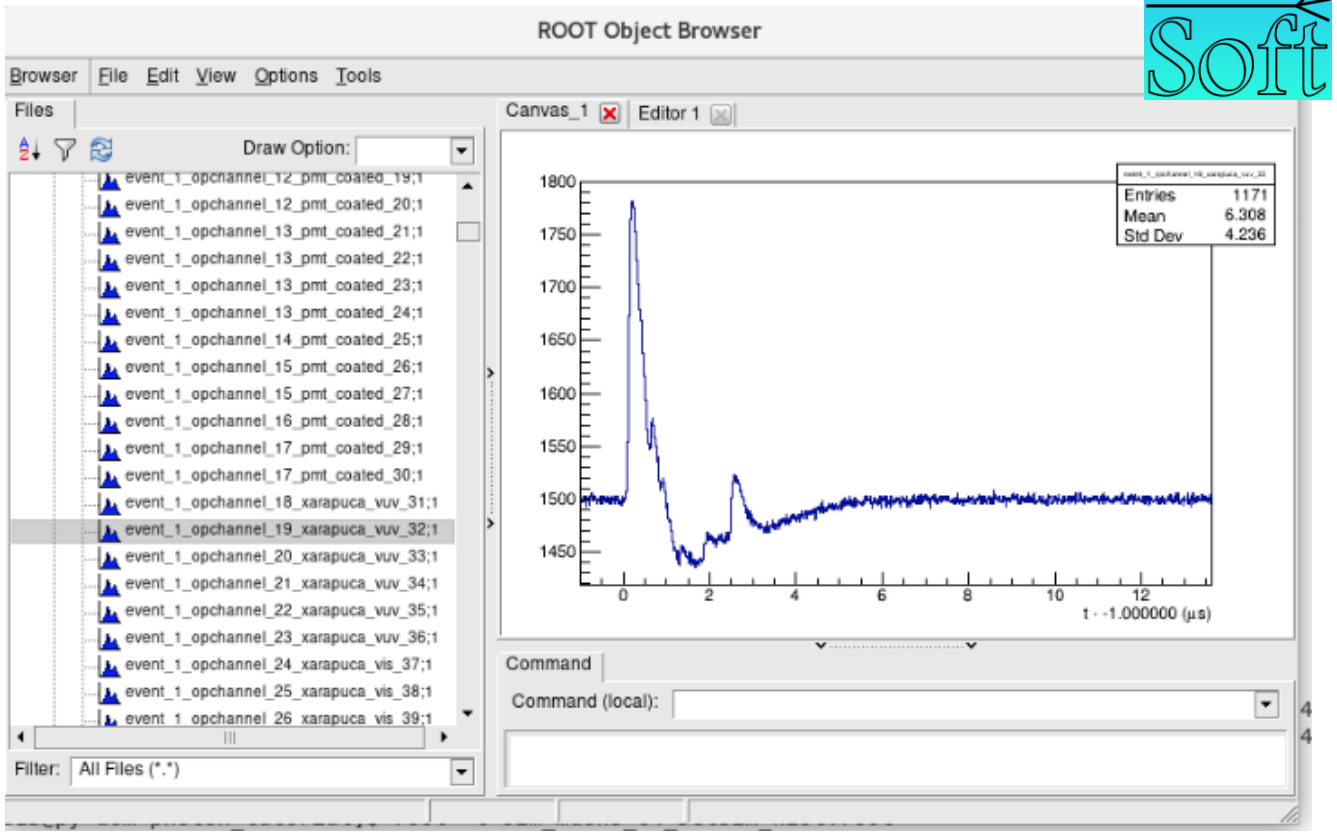


LoopBack with AFE5808A

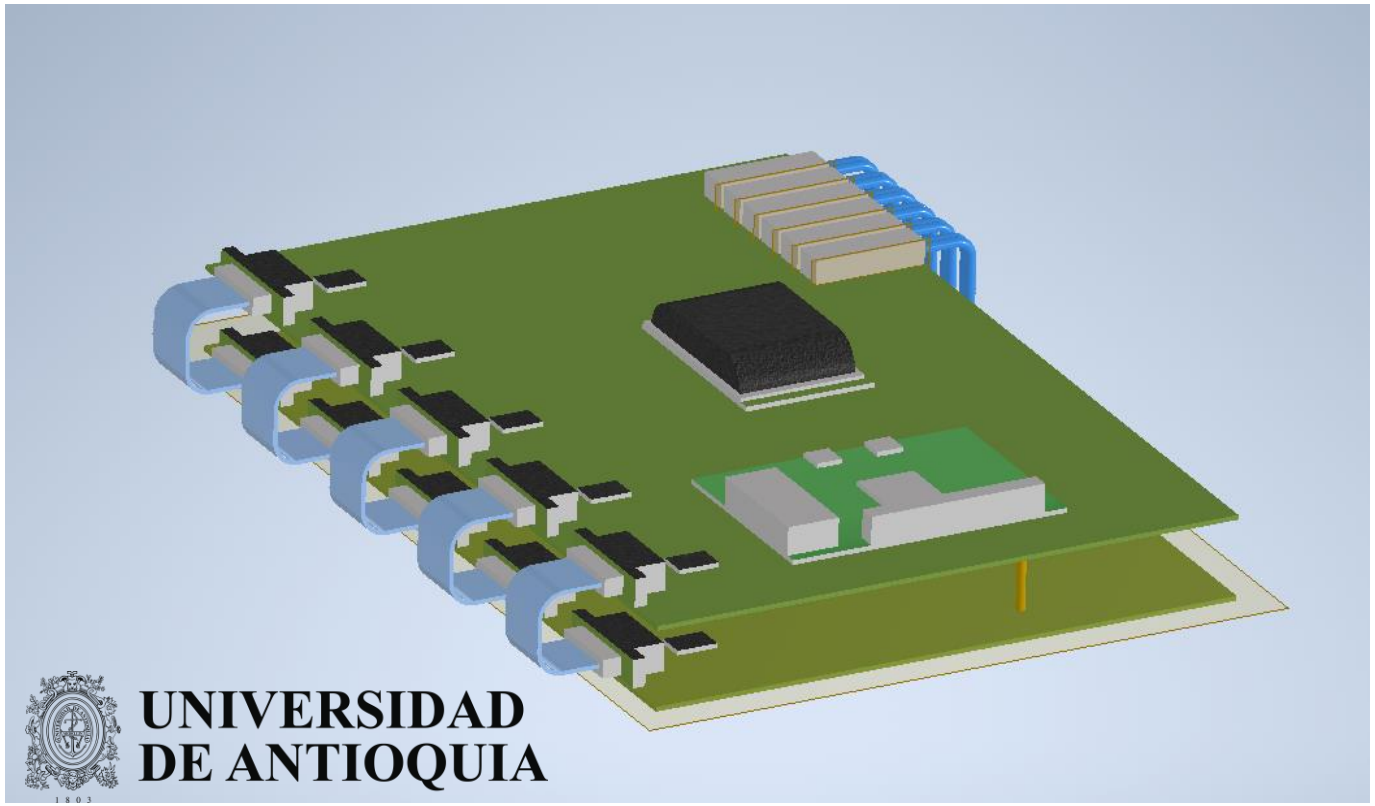
Test bench as event signal simulator

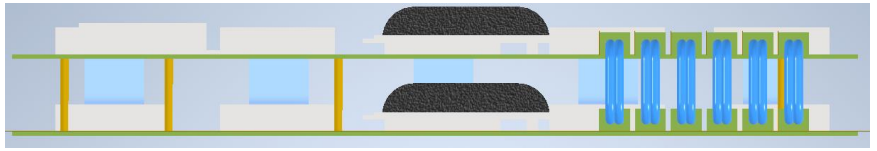
- Generation of simulated events based on physics.
- Measurement of the performance in readout system.
- Diagnosis of electronics' system.

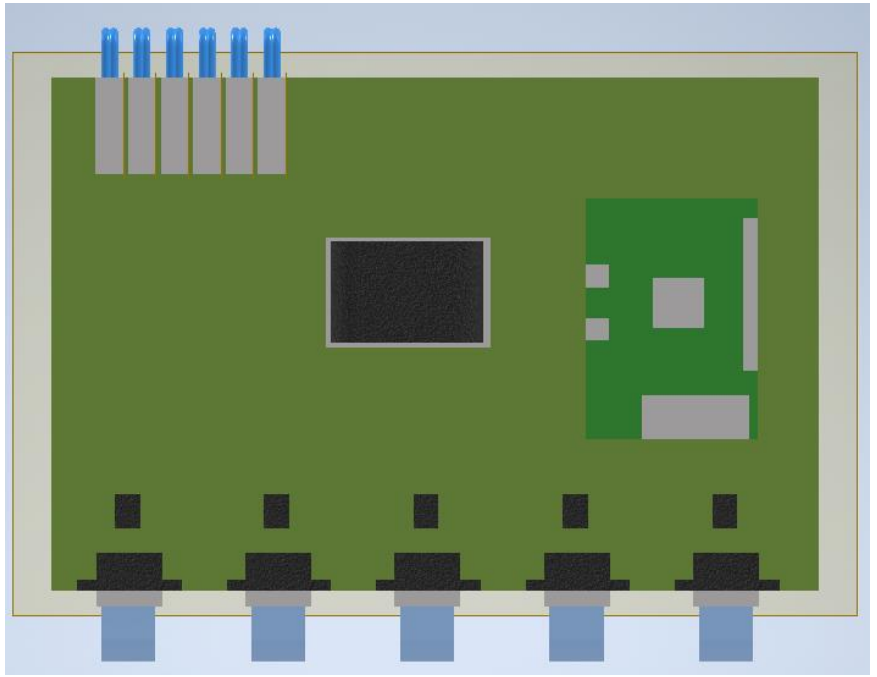


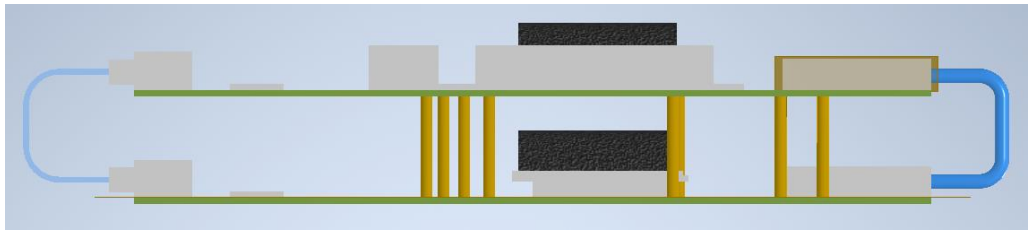


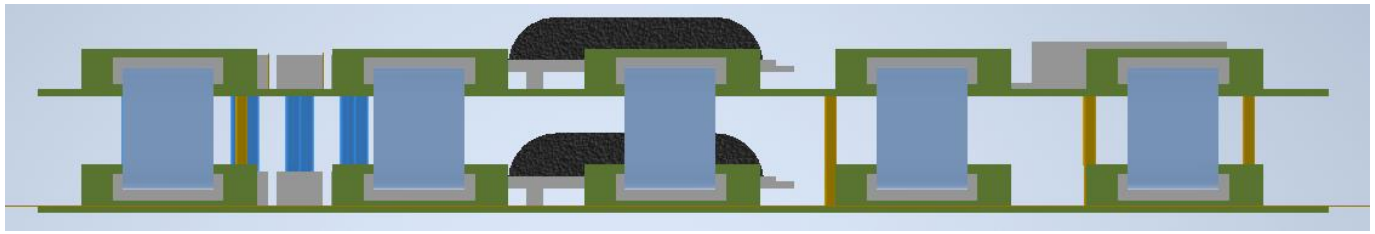
Concept design











Thank you!