# Commissioning of the Mu2e Data AcQuisition system and the Vertical Slice Test of the straw tracker

Intern: Sara Gamba Supervisors: Pavel Murat, Simone Donati



Fermi National Accelerator Laboratories

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DAQ & VST

### Mu2e experiment at Fermilab

### $\mu^- + \mathrm{Al} \rightarrow e^- + \mathrm{Al}$



- Looking for Charged Lepton Flavour Violation;
- Mu2e will improve SINDRUM II limit  $(7.0 \cdot 10^{-13})$  by 4 orders of magnitude;
- Momentum resolution: 2 MeV/c FWHM (SINDRUM II) to 1 MeV/c (Mu2e);
- Three years of running:
  - $3.6 \cdot 10^{20}$  protons;
  - Expected background level below 1 event.

### Signals and backgrounds



$$E_{CE} = m_{\mu} - E_{rec} - E_{bind}$$

Sources of background  $e^-$  (around 105 MeV/c):

- Cosmic particles, CRV;
- DIO of  $\mu^-$  entering the DS;
- $\bar{p}$  by the proton beam and annihilation (absorption elements in the TS);
- RPC: rapidly falls in time. Requirement: delayed live-time window with respect to the proton pulse arrival at the production target.
- $e^{-}$  entering the DS and scattering in the Al (delayed live-time window and an excellent proton beam extinction);
- RMC, similar to RPC, but with a lower maximal energy.

### RPC and timing



- Proton pulses, separated by a time window of 1695 ns;
- RPC rapidly falls in time;
- Selection window after 640 ns.

### The tracker

- 3 m long tracker, 18 stations;
- 3 m downstream of the stopping target in the uniform 1 T region of the DS magnetic field;
- 5 mm diameter and 40-110 cm long straws;
- straw tubes filled with a 80%:20% Ar:CO<sub>2</sub> mixture at a pressure of 1 atm;
- the whole detector will be in vacuum;
- covering radii between 38 cm and 68 cm;
- 96 straws per panel;
- 6 panels per plane;
- 2 planes per station;
- 18 tracking stations: 216 panels.





- Mu2e is starting commissioning;
- To commission the tracker we need the DAQ working;
- DAQ needs to be commissioned first;
- The rest of the talk is about DAQ;

• We are learning about things that are working and things that do not work.

### Tracker readout

- Signals are readout from the ends of each straw on the panel and amplified;
- Signals sent to digitizer electronics;
- From each straw we get 2 times and a hit waveform (charge);
- DRAC: Digitizer Readout & Assembler Controller.



### Tracker readout-2



• TDCs are implemented in FPGAs.

## Mu2e DAQ components diagram



- ROC: ReadOut Controller;
- DTC: Data Transfer Controller (module). One DTC can read 6 ROCs;
- CFO: Command FanOut (module). It synchronizes and checks DTCs;
- CRV: Cosmic Ray Veto.

- Reading 1 ROC, which is the equivalent of one panel;
- ROC has 96 channels;
- Generator sends pulses to channels at 250 kHz and 60 kHz;
- We vary the event window which is the equivalent of the difference between proton pulses;
- Event window and generator frequency define the number of *hits per event*;
- ROC buffer has space for 255 hits:

• 
$$N_{gen}$$
 < 255:  $N_{readout}$  =  $N_{gen}$ ;

•  $N_{gen} \geq 255$ :  $N_{readout} = 255$ , because the buffer is already full.

### Structure of an event and analysis

data header packet	0×00000000:	0x0c10	0x8050	0x00c0	0x49d4	0x005f	0×0000	0x0155	0×0000
validity of the event	0×00000010:	0x005b	0x9fd8	0x1403	0x9fa8	0x0403	0x0041	Øx5996	0x196e
lenght of the event	0×00000020:	0x5b96	0x396e	Øx5856	0x396e	0x5b96	0x396e	Øx5996	0x396e
	0×00000030:	0x0055	0x9f97	0x1403	0x9f72	0x0403	0x0041	0x4751	0x251d
	0×00000040:	Øx4551	0x1515	0x4551	0x1515	0x4551	Øx1519	0x4551	Øx1515
	0×00000050:	0x004f	0x9f2b	0x1503	0x9f12	0x0503	0x0041	Øxf8be	0x33ec
	0×00000060:	0xf93e	0x33ec	0xfb3e	0x0be2	0xf8be	0x33ec	0xf93e	0x0be2
	0×00000070:	0x0049	0x9fc6	0x1403	0x9fdb	0x0403	0x0041	0xd8f6	0x3763
	0×00000080:	0xd8f6	0x0f63	Øxd8f6	0x0f63	0xd8f6	0x0f63	0xdb76	0x0f63
packet: 16 bytes	0×00000090:	0x0043	0x9f66	0x1403	0x9fa7	0x0403	0x0041	0x7b5e	0x0de3
	0x000000a0:	Øx78de	0x35e3	Øx7b5e	0x35ed	0x7b5e	0x35ed	0x7b5e	0x0ded
2 lines hit data	0x000000b0:	0x003d	0x9f81	0×1403	0x9f84	0x0403	0x0041	Øxbbee	0x1eef
	0×000000c0:	Øxb8ee	0x2ee3	0xb9ee	0x1ee7	0xb9ee	0x2ee7	0xb9ee	0x1ee7
channel number	0x000000d0:	0x0037	0x9f6b	0x1403	0x9f93	0x0403	0x0041	0x06c1	0x2c1b
	0x000000e0:	0x05c1	0x2c1b	0x06c1	0x0c13	0x04c1	0x0c1b	0x04c1	0x0c1b
	0×000000f0:	0x0031	0x9fd2	0×1403	0x9fdb	0x0403	0x0041	0xb96e	0x16ed
	0×00000100:	0xb96e	0x16e5	0xb96e	0x16e5	0xb96e	0x36ed	0xb96e	0x36ed
	0×00000110:	0x002b	0x9f94	0×1403	0x9f98	0x0403	0x0041	0x394e	0x14e5
	0×00000120:	0x394e	0x14e5	0x394e	0x34e5	0x394e	0x14e5	0x394e	0x34ed
	0×00000130:	0x0025	0x9f82	0x1403	0x9f87	0x0403	0x0041	0xba2e	0x22e0
	0×00000140:	0xba2e	0x02e8	0xba2e	0x02e8	0xb82e	0x22e0	Øxb82e	0x02e0

- Analysis of the readout teststands of the motherboard:
  - Sending pulses and trying to understand the output and non-output of the DTC;
  - Validation of event format and failure modes;
  - What rate can we operate and which bandwidth can we reach?

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### First steps of analysis: event size distribution



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## Failure mode: events marked as non-valid



Valid event:

0x00000010: 0x005b 0x0660 0x1409 0x062e 0x0409 0x0041 0x5a56 0x2565

0x00000020: 0x5a56 0x1565 0x5956 0x1565 0x5956 0x1565 0x5a56 0x1565

0x00000030: 0x0055 0x061b 0x1509 0x07fb 0x0409 0x0041 0x4751 0x0d13

0x00000040: 0x4751 0x351d 0x4751 0x351d 0x4751 0x351d 0x44d1 0x351d 0x00000050: 0x004f 0x07b3 0x1409 0x079b 0x0409 0x0041 0xfabe 0x2bea

0x000000660: 0xf9be 0x2bea 0xf9be 0x2bea 0xfabe 0x2bea 0xfabe 0x1be6 0x00000070: 0x0049 0x064f 0x1409 0x0660 0x0409 0x0041 0x380e 0x00e0

0x00000080: 0x3bf6 0x00e8 0x380e 0x00e0 0x380e 0x00e0 0x380e 0x3f60

10 5790 5623 Mean 725.1 867.7 Std Dev Std Dev Underflow Underflow Overflow Overflow 2.046e+05 Integral -1.748-1 358 Skewne 10<sup>2</sup> hyter

#### RUN231: Event size distribution of valid and non-valid events

#### Non-valid event:

0x00000000: cx0610 5x0650 5x0660 0x1b07 0x0000 0x0155 0x0000 0x0000010: cx0600 0x350 0x1400 0x554 0x4000 0x001 0x431 0x2310 0x00000020: cx6531 0x131 0x531 0x531 0x531 0x531 0x531 0x531 0x531 0x531 0x00000000: cx6461 0x531 0x1400 0x547 0x4600 0x0611 0x571 0x161 0x00000000: cx6461 0x521 0x6561 0x561 0x661 0x661 0x571 0x161 0x00000000: cx6461 0x551 0x551 0x561 0x561 0x561 0x561 0x571 0x00000000: cx6461 0x551 0x551 0x551 0x561 0x561 0x561 0x561 0x561 0x00000000: cx6461 0x551 0x551 0x550 0x561 0x561 0x561 0x561 0x561 0x00000000: cx646 0x571 0x571 0x570 0x560 0x560 0x570 0x510 0x0000000: cx60 0x540 0x540 0x540 0x540 0x540 0x561 0x571 0x571 0x571

RUN	nevents	TW [ $\times 25$ ns]	R/O rate $[MB/s]$	nvalid [%]
227	132045	1000	0.94	0.82
231	205801	300	0.75	0.57
247	596522	500	2.5	0.19

• Work in progress.

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### Failure mode: events with extra 16 bytes

RUN247: Event size distribution of non-valid events



 0x00000500:
 0x3d97
 0x3d97
 0xe3396
 0x63396
 0x63396
 0x63749
 0x03397

 0x00000510:
 0x00003
 0x21eb
 0x1402
 0x2305
 0x0502
 0x06391
 0x04396

 0x000006010:
 0x4439
 0x1402
 0x2290
 0x6339
 0x0432
 0x0392

 0x000006010:
 0x4439
 0x0291
 0x0350
 0x0439
 0x329
 0x0392

 0x00000610:
 0x0400
 0x0401
 0x3296
 0x360
 0x360
 0x329
 0x329

 0x00000610:
 0x5396
 0x5396
 0x5960
 0x5960
 0x5396
 0x5596
 <

- : CAL1 (not the last)
- : HV1 (not the first)

- Studying the time of 0x008a, we find a time of 5 ns;
- We think that we had a timing misallignment between channels.

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### Failure mode: non existent channels



RUN247: Occurrences of existent and non existent channels

•••

 0x0000050:
 0x0000f
 0x2329
 0x1401
 0x2355
 0x1558
 0x558
 0x1558
 0x556
 0x1558
 0x5568
 0x2a8
 0x2a955
 0x1558
 0x5568
 0x2a8
 0x2a955
 0x1558
 0x5568
 0x2a8
 0x2a955
 0x1558
 0x5568
 0x2a8
 0x2a95
 0x158
 0x558
 0x558
 0x528
 0x2a8
 0x2a95
 0x158
 0x558
 0x528
 0x2a8
 0x2a95
 0x158
 0x558
 0x528
 0x2a8
 0x2a95
 0x588
 0x395
 0x588
 0x395
 0x38

: value greater than 96 channels



: lenght of the event

- Something that should be fixed in the firmware, work in progress;
- Few events: at most, in one run, 2 events like this.



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### Analysis of logger and boardreader rate



- Rates reported by boardreader (DAQ input) and logger (DAQ output);
- multiple runs, varying:
  - number of ROCs : one or two;
  - number of channels per ROC: 4-96;
  - length of the time window 12.5 50  $\mu$ s.
- $R_{br} < R_l$ : work on understanding in progress;

### Zooming on each RUN

rate:mkt

• rate spikes in RUN281 (longest one - 1 ROC): closing output files.

- RUN294: read 2 ROCs with 96 channels each:
  - the rate dropped down by a factor of 3: work in progress.
- 500MB in 13 min  $\rightarrow$  0.7MB/s but ARTDAQ reports 7MB/s: need to understand why!

## Validation of generator frequency



• Generating hits in each channel at  $31.29 \text{ MHz}/(2^7+1)$  and  $31.29 \text{ MHz}/(2^9+1)$ ;

• Generator frequency validated with accuracy better than 20 ps.

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# Occupancy: number of hits vs channel number



- Mode of overflowing hit buffer;
- Not a uniform distribution of number of hits vs channels;
- Not the same occupancy for all channels.

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# Occupancy: "expected" order



- Tried to change event window and frequency;
- We expected that the buffer gradually fills with channels;
- Probably channels are in a different order.

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# Calibration of the time difference between channels



• time difference between ch00 and ch91 (first channel of first FPGA);

• time difference between ch44 and ch94 (first channel of second FPGA).

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# Monte Carlo simulation of the DAQ system

- From 0  $\mu$ s to  $1/f_G \mu$ s: creation of the first event ( $t_0$ ) (uniform distribution);
- Hits from the same channel are separated by  $1/f_G \mu$ s: creation of the second event  $(t_1)$ , adding to  $t_0$  this quantity;
- If the second pulse is cointained in the time window, we add this hit in the event we are building;
- As soon as we reach 255 hits we stop the fill;
- Changing time window and generator frequency, to better compare each RUN with the simulation and adding FPGAs offsets and channel to channel offsets.

### Monte Carlo simulation: results

#### Channels are not ordered as we expected.



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## Conclusions and goals

### • What did we find and understand?

- Structure of a valid event;
- Different event size distributions;
- 3 types of failure modes;
- Analysis of logger and boardreader;
- Generator frequency has been validated;
- Analysis of the occupancy and comparison with MC;
- Delays between channels.

### • Short/Mid-term:

- We are now able to read 1MB/s (1 DTC and 1 ROC): our goal is to read 600MB/s with one DTC!
- Running tests on one station or more;
- Late fall-early winter: Vertical Slice Test;
- Long-term:
  - Integrating the DAQ system in the whole experiment.

# Thank you for your attention!



### [1] Abdi et al.

Mu2e run i sensitivity projections for the neutrinoless  $\mu^- \to e^-$  conversion search in aluminum.

2021.

[2] Gioiosa et al.

Slow control and data acquisition development in the mu2e experiment.

2021.

[3] MyeongJae Lee.

The straw-tube tracker for the mu2e experiment. 2016.