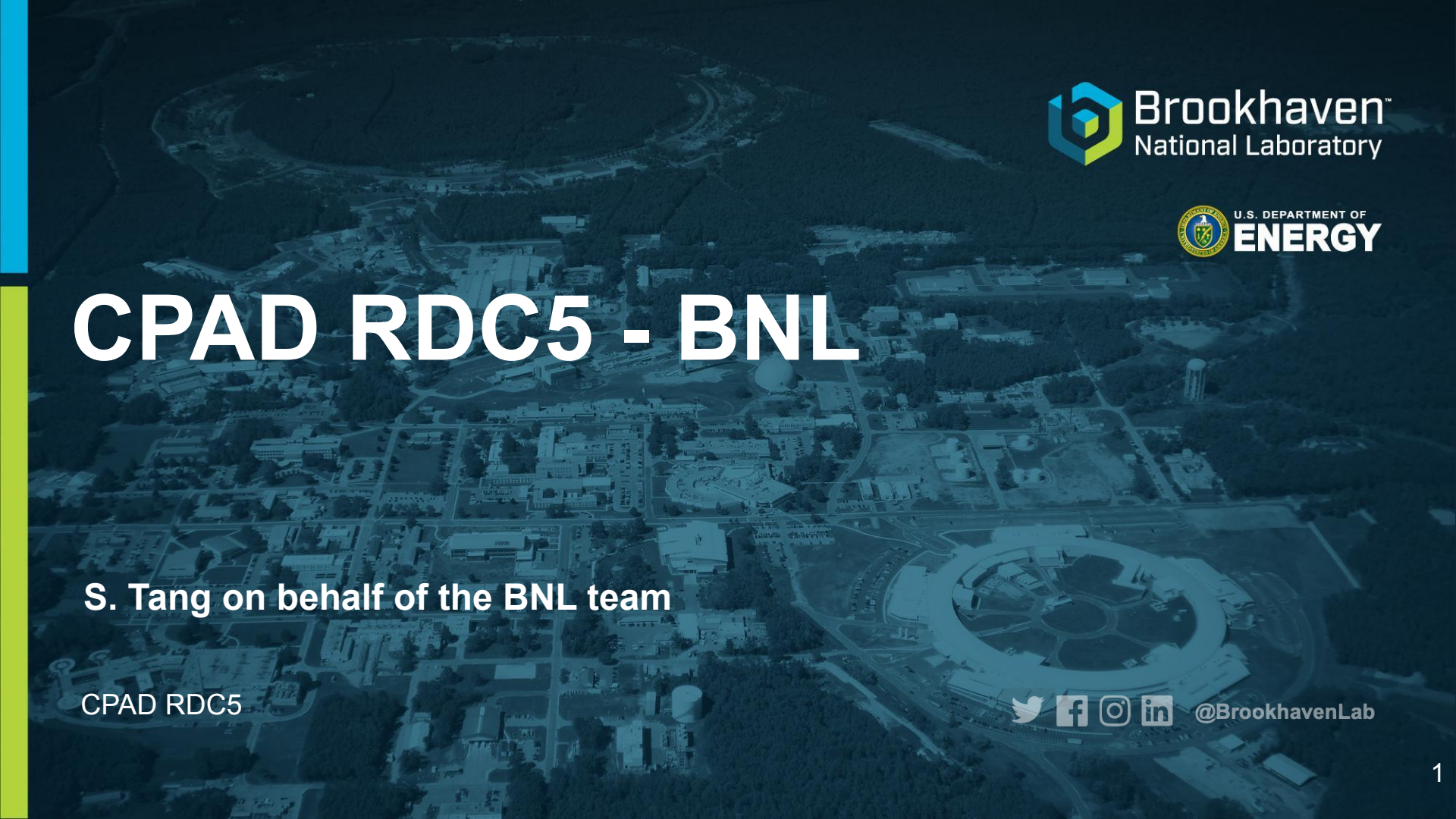


CPAD RDC5 - BNL

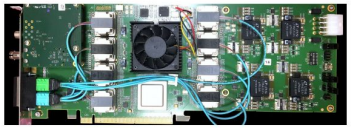
S. Tang on behalf of the BNL team

CPAD RDC5

@BrookhavenLab

Current Research

Front-End Link eXchange (FELIX)



100 FLX 712 cards
up to 48 links (8 minip)
-4.8G and 9.6G
Kintex Ultrascale FPGA
PCIe Gen 3x16 lanes

FELIX Phase-I

60 Host Servers
Intel Xeon E5-1660 v4 @ 3.2GHz
- 32 GB DDR4 2667 MHz memory
- Mellanox Connect-X 25/100 GbE

ITK Pixel 220	ITK Strips 76	LAr LASP 50	LAr LASP TTC 16
LAr LDPB 6	LAr LDPB TTC 2	LAr LTDB 32	LAr LATS TTC 6
L0Calo 8	NSW 120	NSW TP 4	RPC BARREL SL 6
CTP 1	MUCTPI 1	MDT TP 64	GLOBAL TRIG. 11
TILE 16	TGC ENDCAP 8	HTGD 48	HTGD LUMI 32
BCM 2	LUCID 1	ZDC 1	AFP 1
GBT (Gb/s) up:4.809 down:4.809	lpGBT (Gb/s) up:10.26 down:2.57	FULL (Gb/s) up:9.618 down:9.618	Interlaken (Gb/s) up:25.78125 down:9.618

FELIX Phase-II

FELIX 182: Phase II

- FPGA: AMD Versal Prime VM1802
- 16 lane PCIe Gen4 interface (240 Gb/s)
- 4 FireFly transceivers up to 25 Gb/s
- One duplex FireFly transceiver up to 25 Gb/s FireFly TRx
  - new protocol for Timing Trigger & Control (LTI)
  - 100 GbE Ethernet
- Versal Processing system, runs PetaLinux
  - Monitor temperatures & voltages, update flash memory, perform build-in self test (BIST)
- Host server for testing, AMD Epyc 9004 CPU
  - 96 GB DDR5
  - Dual 200 Gb/s Ethernet on PCIe Gen5

Brookhaven National Laboratory

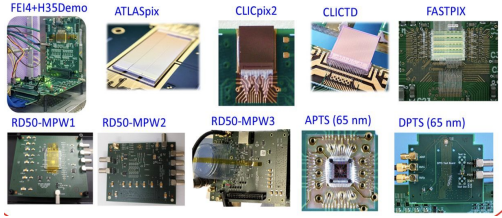
CaRIBOu:

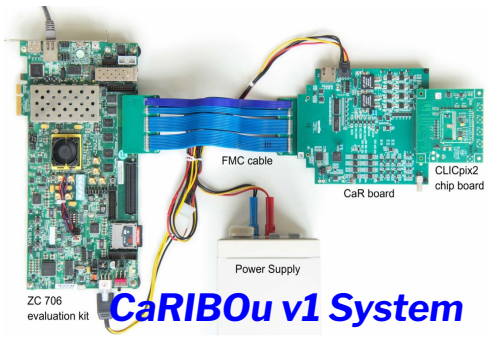
Modular readout system for silicon sensor R&D

Collaboration between BNL and Carleton in the development of the next generation system hardware CaRIBOu v2 since 2022

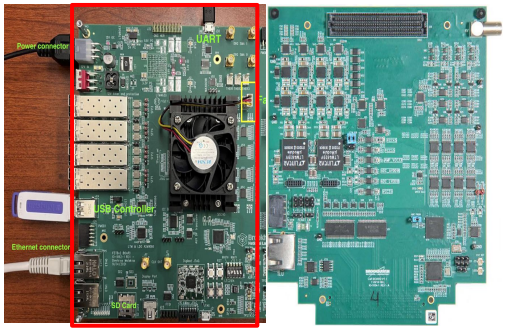
Strong collaboration on CaRIBOu v2 system development and support (BNL,Carleton,CERN,DESY,ORNL, Others)

CaRIBOu has been proposed as the common project in the newly formed DRD3 collaboration





CaRIBOu v1 System



CaRIBOu v2 System

R&D Interests

- The focus of the BNL TDAQ R&D program is the **integration of unique capabilities in detector technology, readout, and signal processing**
- **CaRIBOu** and **FELIX** have been developed with our collaborators and widely used in different experiments by large community
- **The future work of CaRIBOu and FELIX is well planned and the R&D is ongoing**
- **High bandwidth, Low latency, FEC algorithm study**
- **Edge computing and AI firmware in the FPGA**
- **Challenges in thermal and power design for TDAQ hardware**
- **In DRD7 workshop, Generic back-end hardware and No back-end system design for different detectors.**

DRD7 Workshop: https://indico.cern.ch/event/1318635/timetable/?view=standard

Sophie Baron: https://indico.cern.ch/event/1318635/contributions/5552004/attachments/2720917/4727120/DRD7.5b_26092023.pdf

Antonio Pellegrino: https://indico.cern.ch/event/1318635/contributions/5552107/attachments/2721677/4728562/DRD_7.5.c_26Sep2027.pdf