SiPM front-end electronics in NEXT

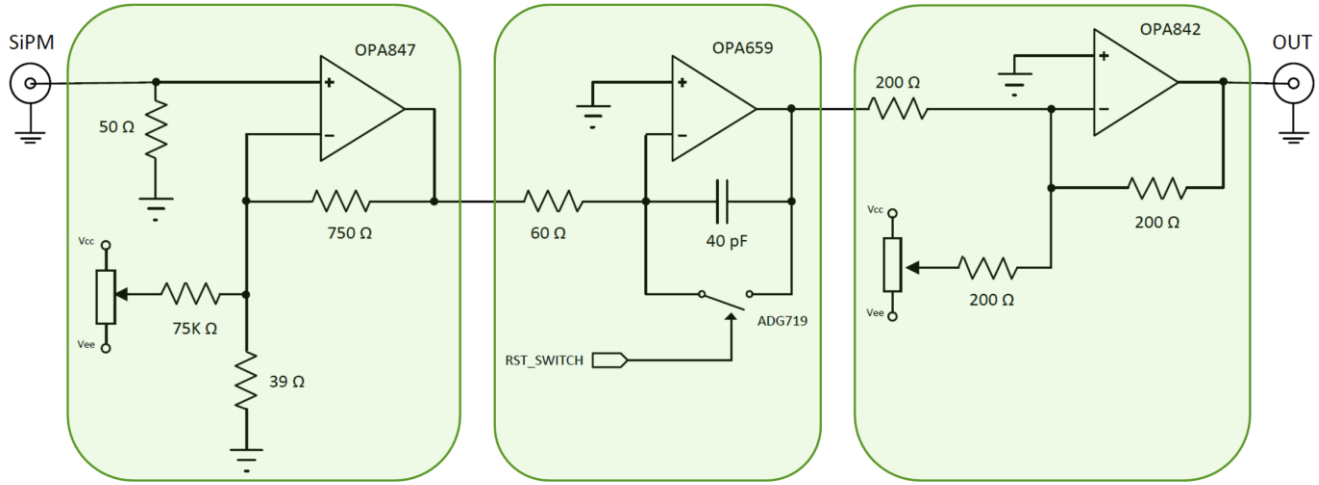
- **An approach based on gated integrators (NEXT-DEMO)**
- **An approach based on pulse stretching & sampling (NEXT-DBDM)**
- **A proposed front-end scheme and board for NEXT-100**

Review of NEXT-DEMO and NEXT-DBDM solutions

Our proposal for NEXT-100 is based on the first results with these two developments

Review: NEXT-DEMO FE-SiPM read out (1/3)

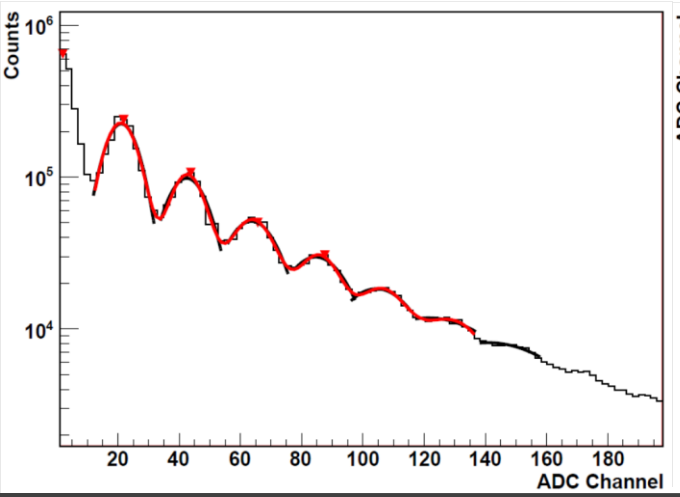
NIM A, Vol. 695, 11th December 2012, Pages 229–232
Readout electronics for the SiPM tracking plane in the NEXT-1 prototype

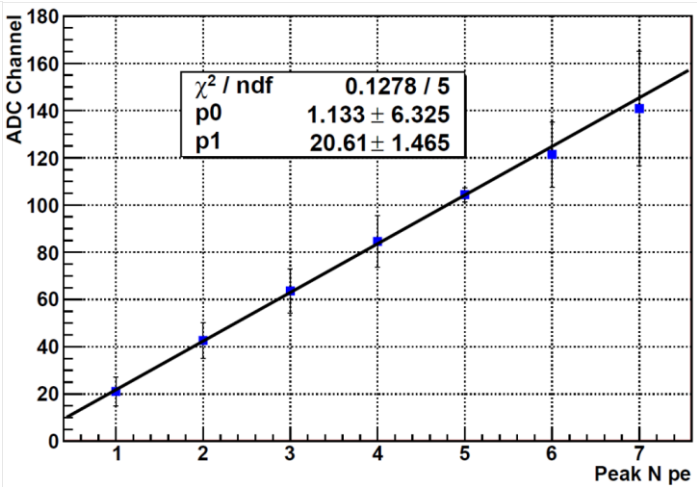


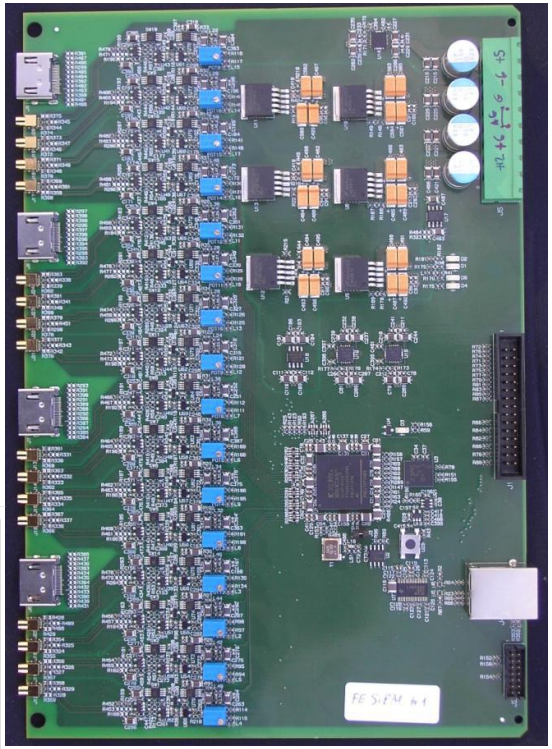
Stage 1: transimpedance amplifier + offset correction

Stage 2: gated integrator

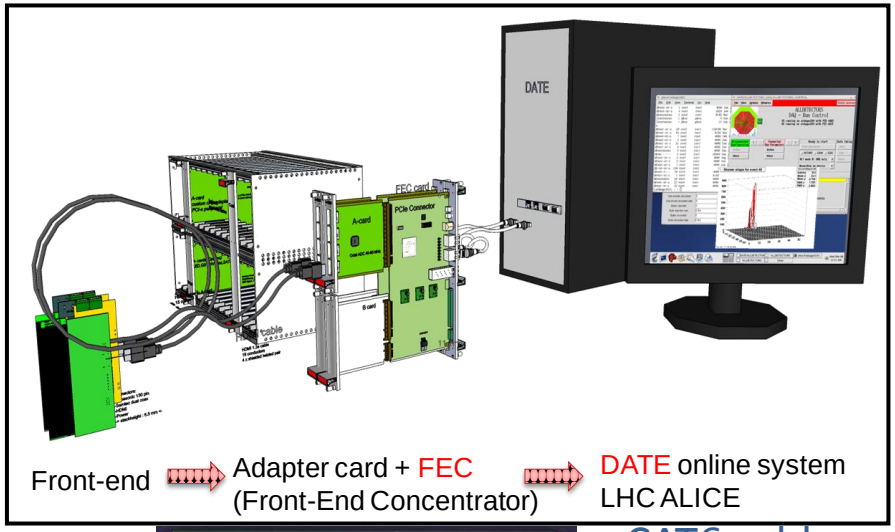
Stage 3: inverter + offsset correction







Review: NEXT-DEMO FE-SiPM read out (2/3)



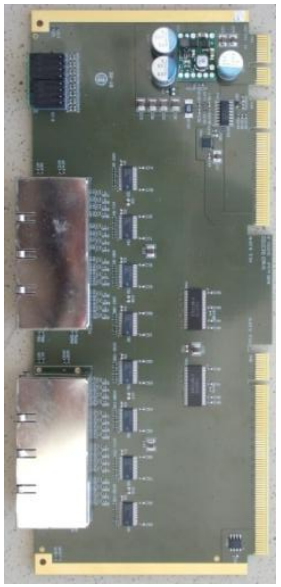
RD51 SRS readout/DAQ chain

16x SiPM-FE boards

CAT6 cable

Data

Clock, trigger, cmd



2x LVDS I/O cards

2x FECs

2x GbE

Review: NEXT-DEMO FE-SiPM read out (3/3)

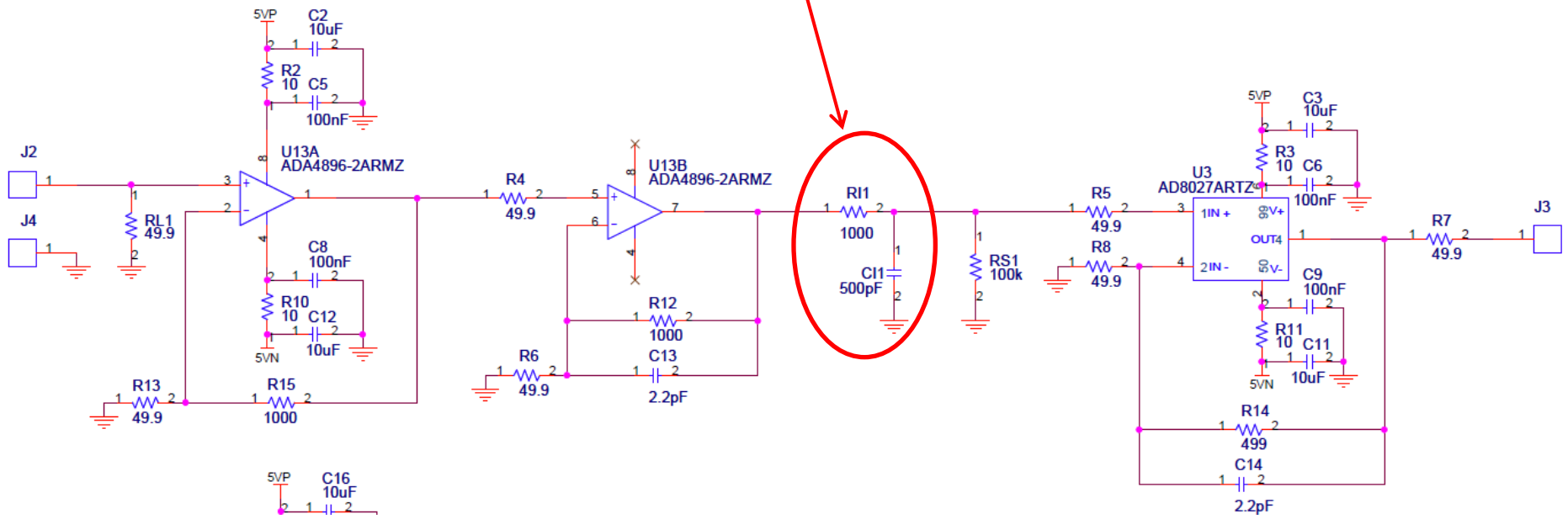
These **amplifiers** will not be used in NEXT-100 because:

- ❑ Power dissipation would be too high (10V*20mA*3 = 600 mW/ch). This requires active cooling
- ❑ Offset adjustment by hand for ~7000 ch may be a nightmare, so we need automatic adjustment
- ❑ Also: gated integrator requires a switch, 6.800 switches may create a large noise

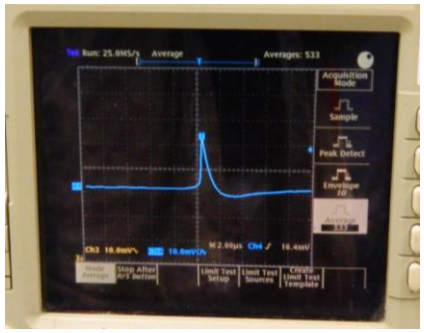
As a result we defined a new scheme (D.Nygren) that has been tested in NEXT-DBDM (next slide)…

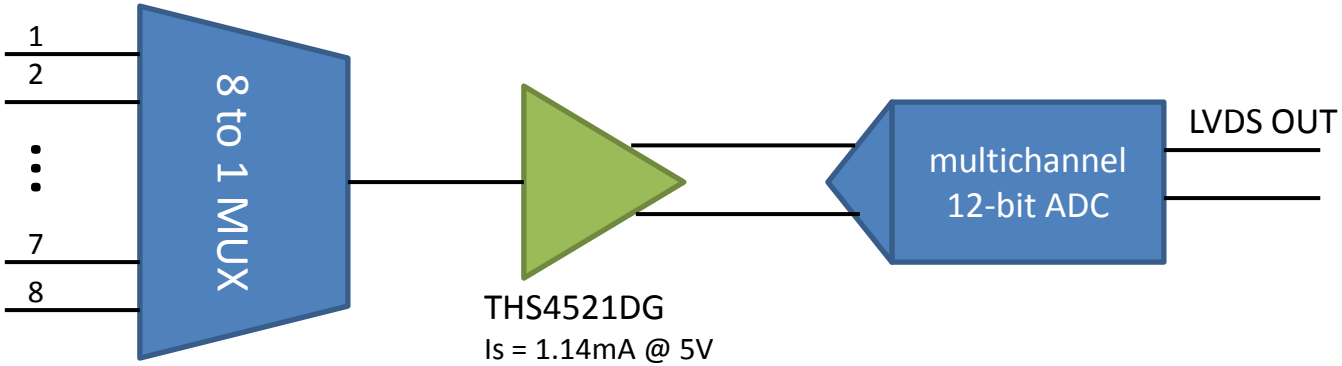
Review: NEXT-DBDM FE-SiPM read out (1/4)

Dave: "Replace the gated integrator with a simple RC and use low power amplifiers"



John Joseph: "Circuitry can be further simplified by using multiplexers before the ADC"





Review: NEXT-DBDM FE-SiPM read out (2/4)

Source: http://www.analog.com/static/imported-files/product_selection_guide/High_speed_amps_sel_table.pdf

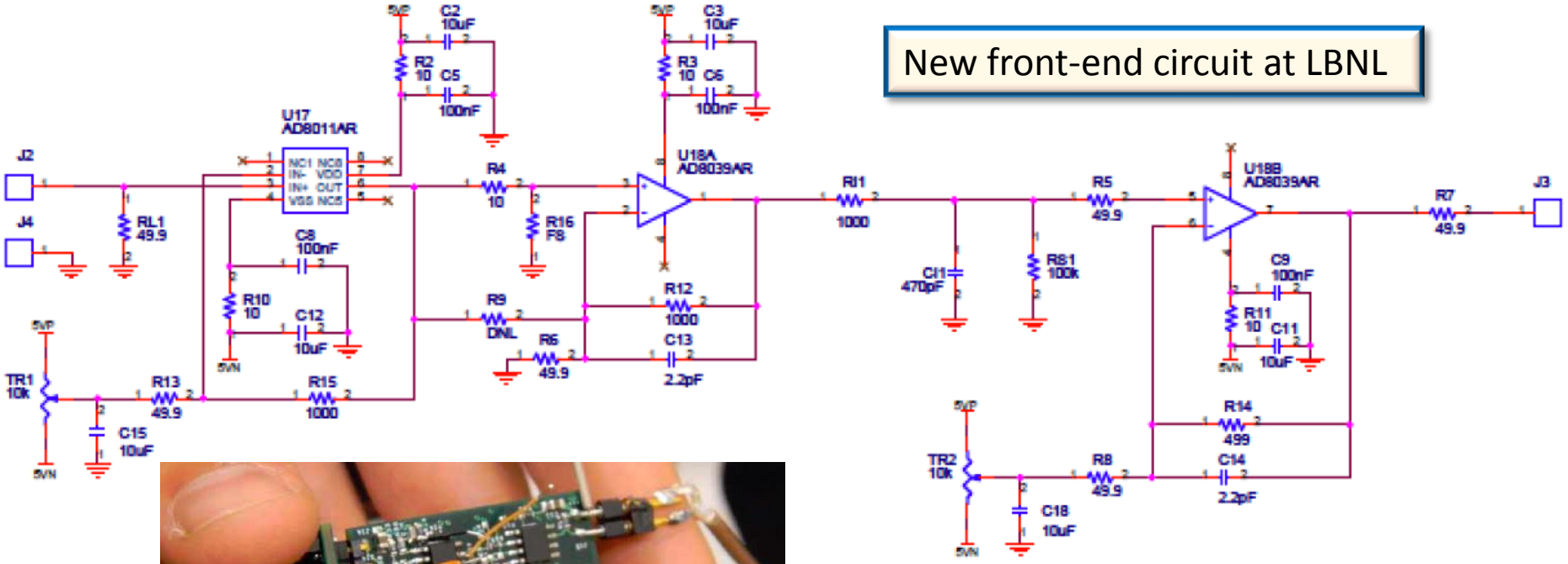
Amplifier	Type	BW 3dB G=1 (MHz)	Noise (nV/√Hz)	V_{offset} (mV)	I_{bias} (μA)	$I_{quiescent}$ (mA)	Cost ($)	Supply (V)
AD8005	CFA, single	270	4	30	10	0,4	1,63	5, ±5
AD8038/9	Single/dual	350	8	3	0,75	1	0,86/1,21	3, 5, ±5
AD8011	CFA, single	400	2	5	15	1	2,27	5, ±5
AD8014	single	480	3,5	5	15	1,1	1,19	5, ±5
ADA4841-1/-2	Single/dual	80	2,1	0,5	5,3	1,2	1,61/2,32	2.7, 5, ±5
ADA4940-1/-2	DIFF single/dual	240	3,9	0,4	1,55	1,25	1,79/2,95	3, 5
AD8029/30/40	Single/dual/ quad	125	16,5	5	1,3	1,3	0,86/1,21/ 1,62	2.7, 5, ±5
ADA4853	Single/dual/ triple	100	22	4	1,6	1,4	0,56/0,7/0,86	3, 5, ±5
AD8012	CFA dual	350	2,5	4	12	1,7	2,5	5, ±5
AD4896-2	Dual	230	1	0,5	17	3	3,2	3, 5, ±5
AD8027/8	Single/dual	190	4,3	0,9	6	6,5	1,2/1,91	3, 5, ±5

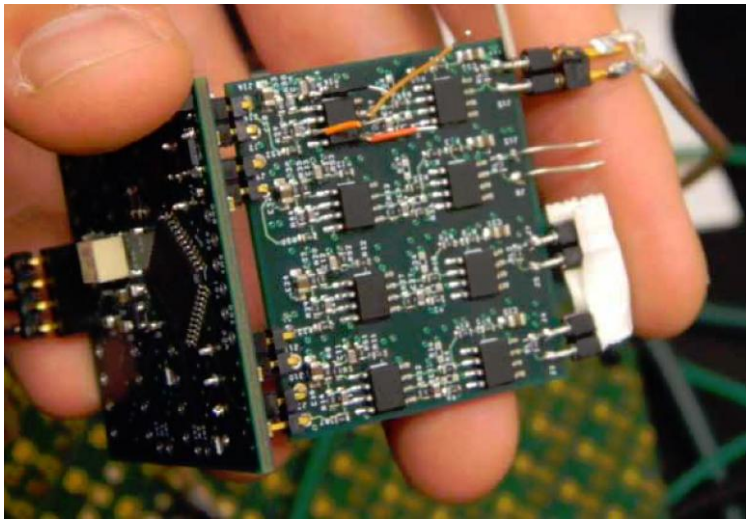
Valencia&LBNL final decision: higher noise and offset voltage but low power (30 mW/ch) and cost ($3,48/ch)

Initial LBLN prototype: higher performance but also higher power (125 mW/ch) and cost ($7,8/ch)

Review: NEXT-DBDM FE-SiPM read out (3/4)

New front-end circuit at LBNL





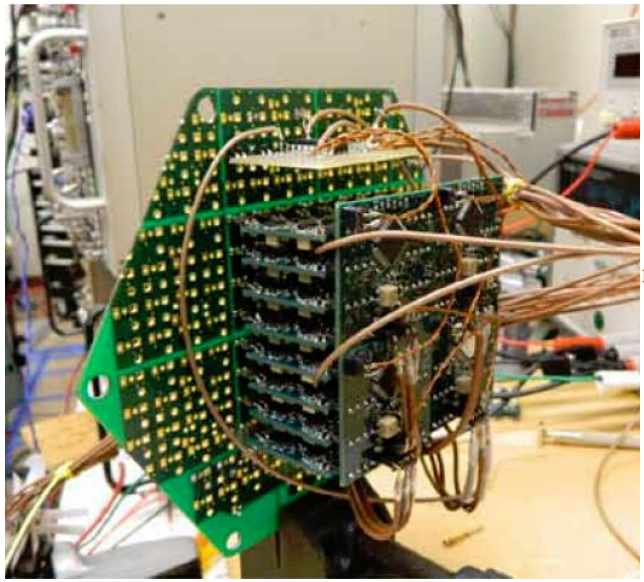
16-ch mux and 4-ch front-end boards

Based on AD8011 and AD8039
Still manual offset control
COTS external digitizer (up to 100 MHz)

Review: NEXT-DBDM FE-SiPM read out (4/4)

Digitized data have been analyzed (Lisa Gerhardt, LBNL) to find out the required sampling rate (and results show that 2-3 MHz is acceptable)

This prototype shows the feasibility of the new readout concept for NEXT-100



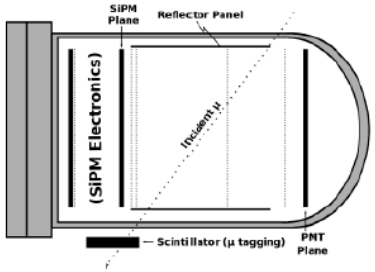
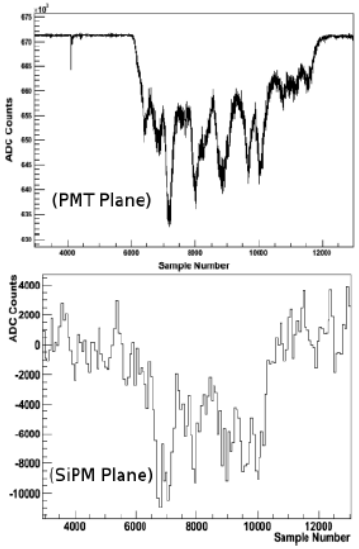
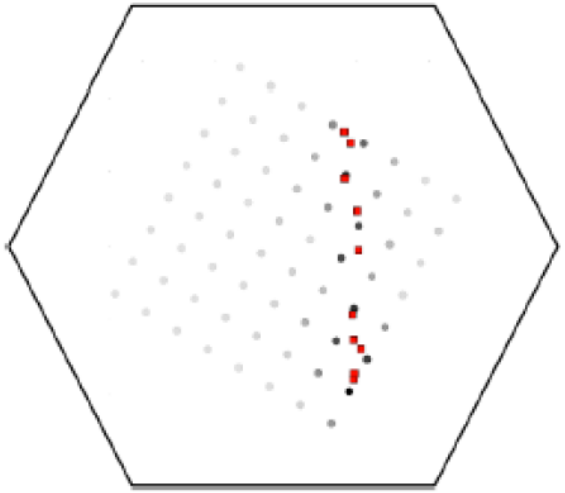


Figure 5: Schematic of the muon tracking test setup for NEXT-DBDM.





Muon tracking

Requirements for NEXT-100

A requirements document is not yet finished, but let's highlight the main desing parameters

Requirements for NEXT-100

A sound front-end design for NEXT-100 should:

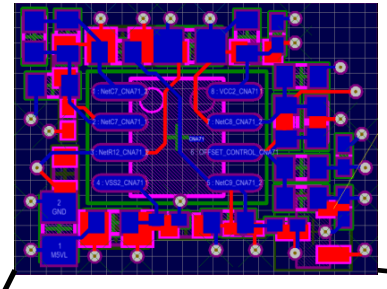
- ***Resolve the single photoelectron to ease calibration***
  - ***The gated integrator allows pe-based calibration***
  - ***The stretching&sampling approach requires a bypasseable filter***
  - ***New LBNL analog stage dissipates 30mW/ch in the amplifiers. We could choose other opamps, trading power for noise, in oder to enhance spe discrimination***
- ***Provide enough time and amplitude resolution (tbd)***
- ***Have an automatic offset voltage compensation***
- ***Be able to perform zero suppression on-the-fly and have an event bufffer (see DAQ requirements)***

Proposal for NEXT-100 (amplifier circuit)

Use NEXT-DBDM circuit topology, add a switch to bypass the filter and an FPGA-controlled offset voltage adjustment

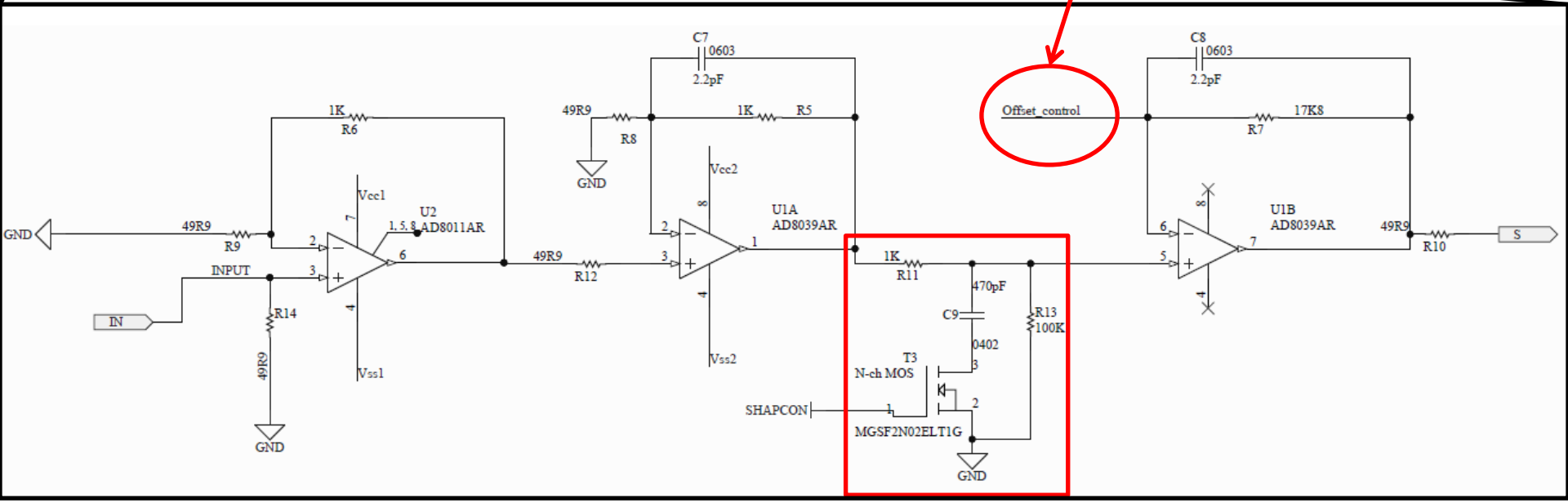
Proposed amplifier circuit

Small PCB area (1,7cm²)



Final opamps will be a trade off between power, noise and cost (AD8011 & AD8039 optimize power and cost)

FPGA-controlled DAC (128 DAC channels)



500 ns shaping filter
Can be bypassed to enhance spe detection

Sampling & offset voltage

On the signal and its sampling:

- **RC time constant is approx. 0.5 μs**
- **Sampling rate is 2-3 MHz**

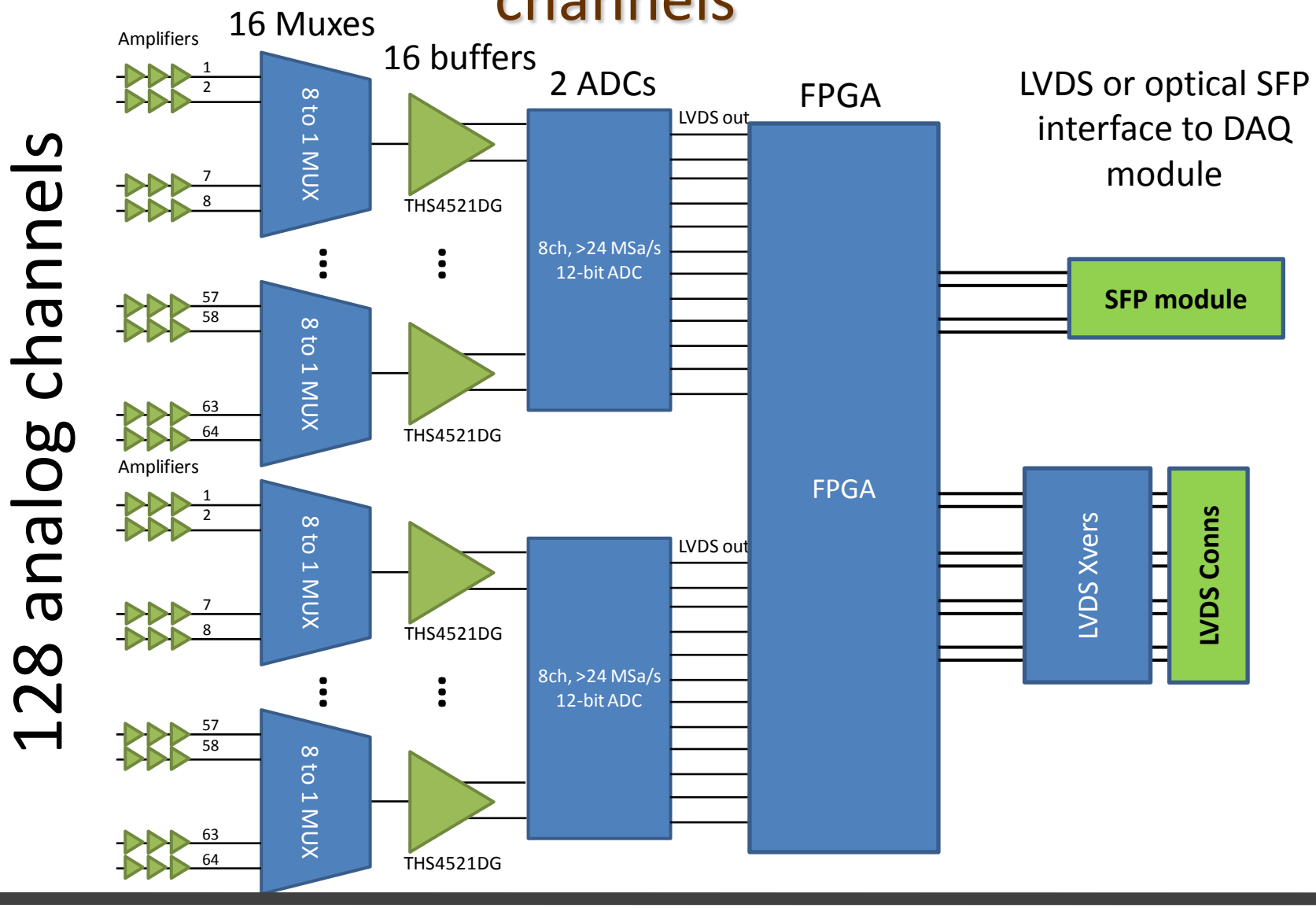
On the offset voltage adjusment: coarse (analog) + fine (digital)

- **Coarse automatic offset adjustment with a DAC (at the 3rd stage)**
- **ADC dynamic range is typ. $2V_{pp}$**
- **Keep signal dynamic range in approx. $1V_{pp}$**
- **Leave the additional ADC range for the residual offset voltage**
- **Correct the residual offset after digitization (fine adjustment) !!**

Proposal for NEXT-100 (front-end board -FEB)

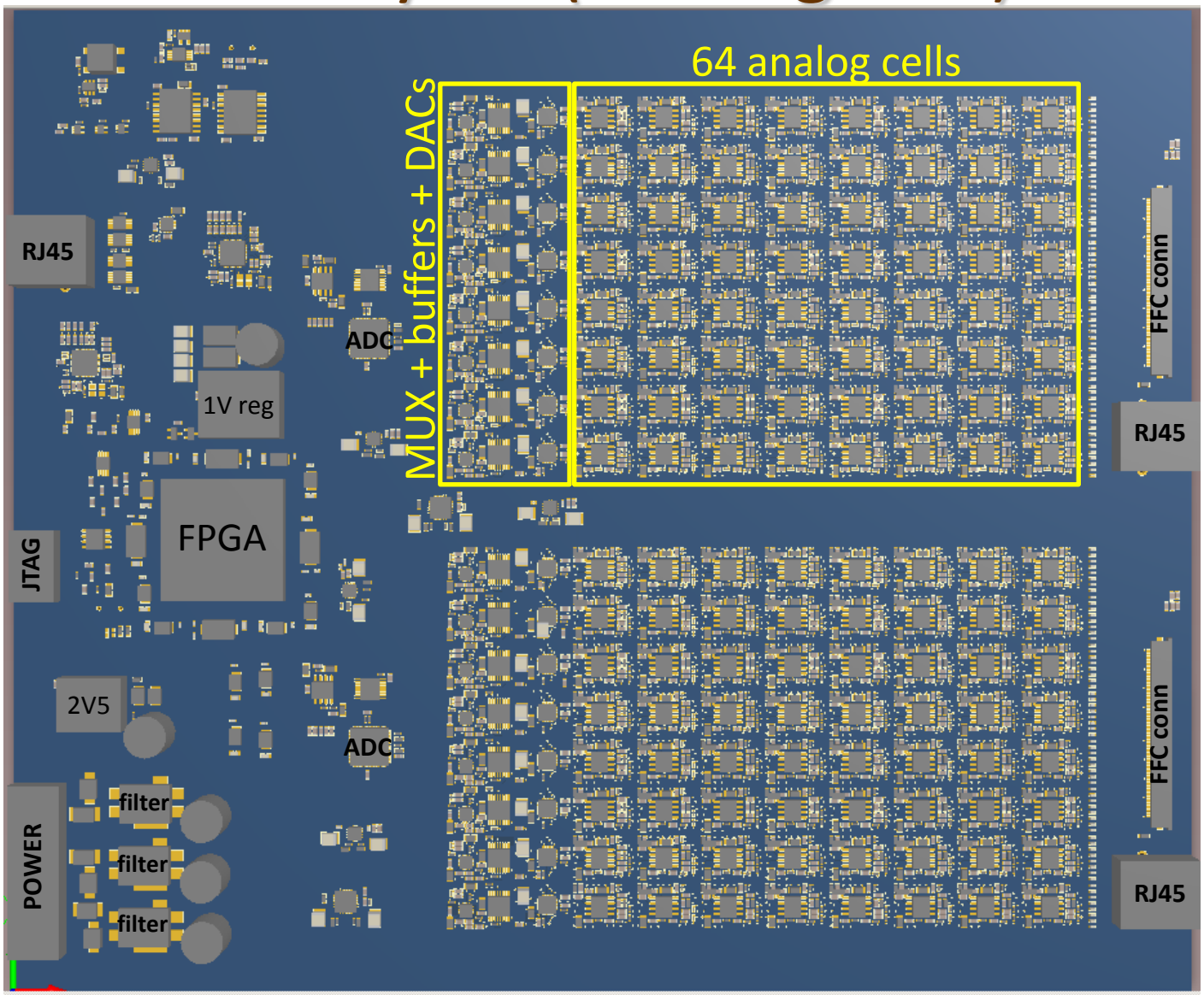
Packing 128 analog stages (amplifiers) and its required multiplexers, buffers, ADCs, FPGA, data transceivers and voltage regulators

The whole mux&samploing chain for 128 channels



FEB layout (missing: SFP)

6U x 280mm Eurocard

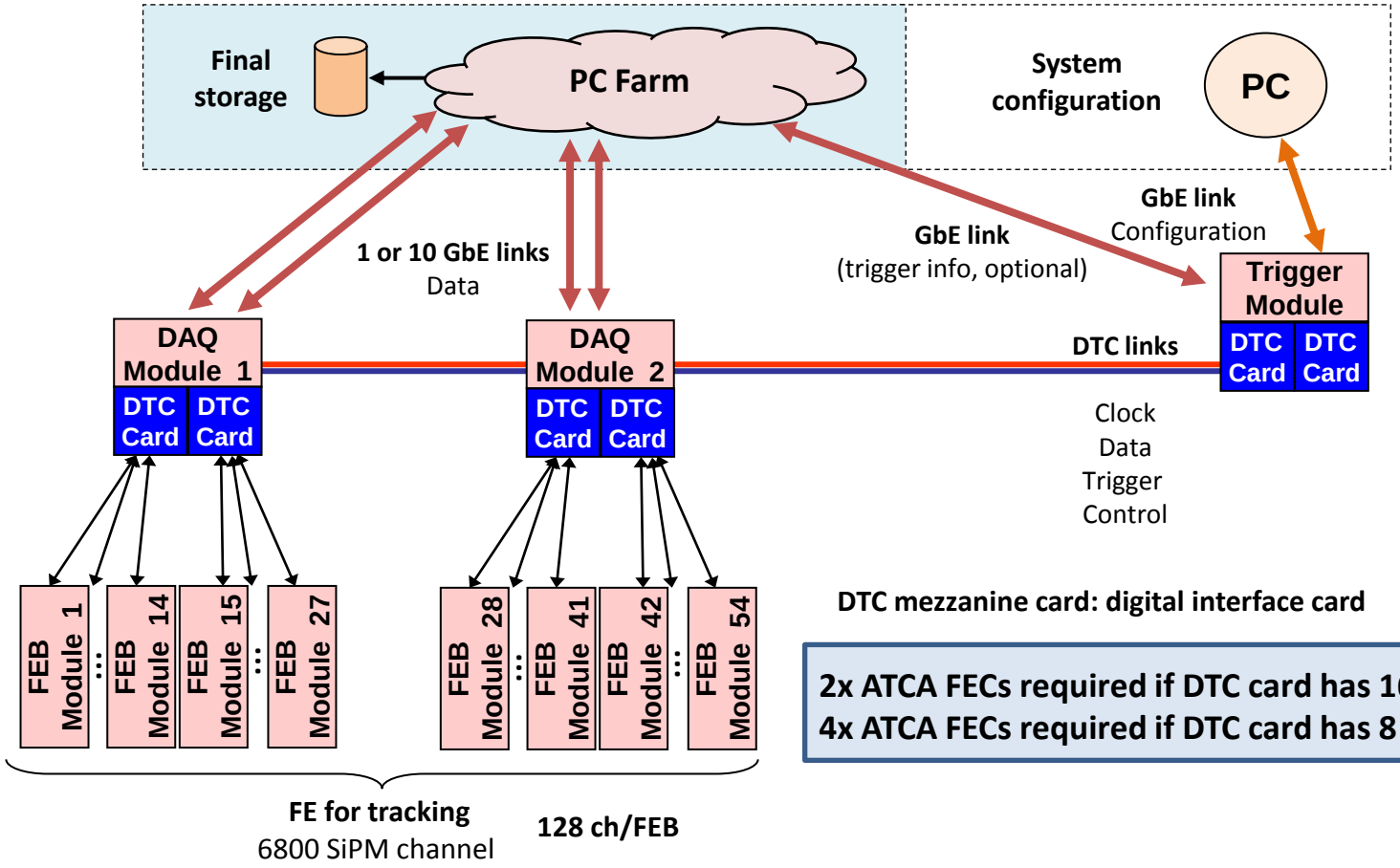


Data handling and buffer in FEB

- ***FPGA***
  - ***estimates signal baseline***
  - ***automatic control for per-channel coarse offset voltage compensation***
  - ***automatic fine correction for offset voltage***
  - ***controls multiplexers and ADCs***
  - ***zero-suppresses data (based on configurable parameters)***
  - ***timestamps and buffers data***
  - ***sends data to DAQ when a trigger is received***
  - ***allows monitoring&control from DAQ module***
- ***Virtex-6 LX130T, 195T or 240T in BGA784 (footprint compatible)***
  - ***same FPGA as in ATCA FEC (DAQ module)***
  - ***internal dual-port buffer size: 9504/12384/14976 Kb***
    - ***This allows 6336/8256/9984 samples/ch buffer depth***
    - ***At 2MHz sampling, 2 chamber drift times, one full raw event needs 6400 samples/ch***
- ***Uplink throughput***
  - ***LVDS: 400 Mb/s (as used in NEXT-DEMO)***
  - ***SFP with simple protocol for clock, trigger, slow controls and data: up to 1Gb/s (currently under development, CERN)***

Proposed FE&DAQ architecture for NEXT-100 (SiPM tracking plane partition)

NEXT-100 DAQ – ATCA Architecture (see presentation on DAQ)



DTC mezzanine card: digital interface card

2x ATCA FECs required if DTC card has 16 links (LVDS)
4x ATCA FECs required if DTC card has 8 links (SFP optical)