# The DAQ system

- **The DAQ system: RD51's SRS review**
- **Classic flavor of SRS**
- **ATCA flavor of SRS**
- **A proposed DAQ architecture for NEXT-100**
- **Trigger system overview**

# RD51's SRS

**RD51**: CERN approved R&D programme for "Development of Micro-Pattern Gas Detectors Technologies"

**SRS**: Scalable Readout System

• A front-end independent (at least very flexible), portable, scalable, multichannel readout system developed for RD51 users. Initially developed by CERN-PH-AID and NEXT

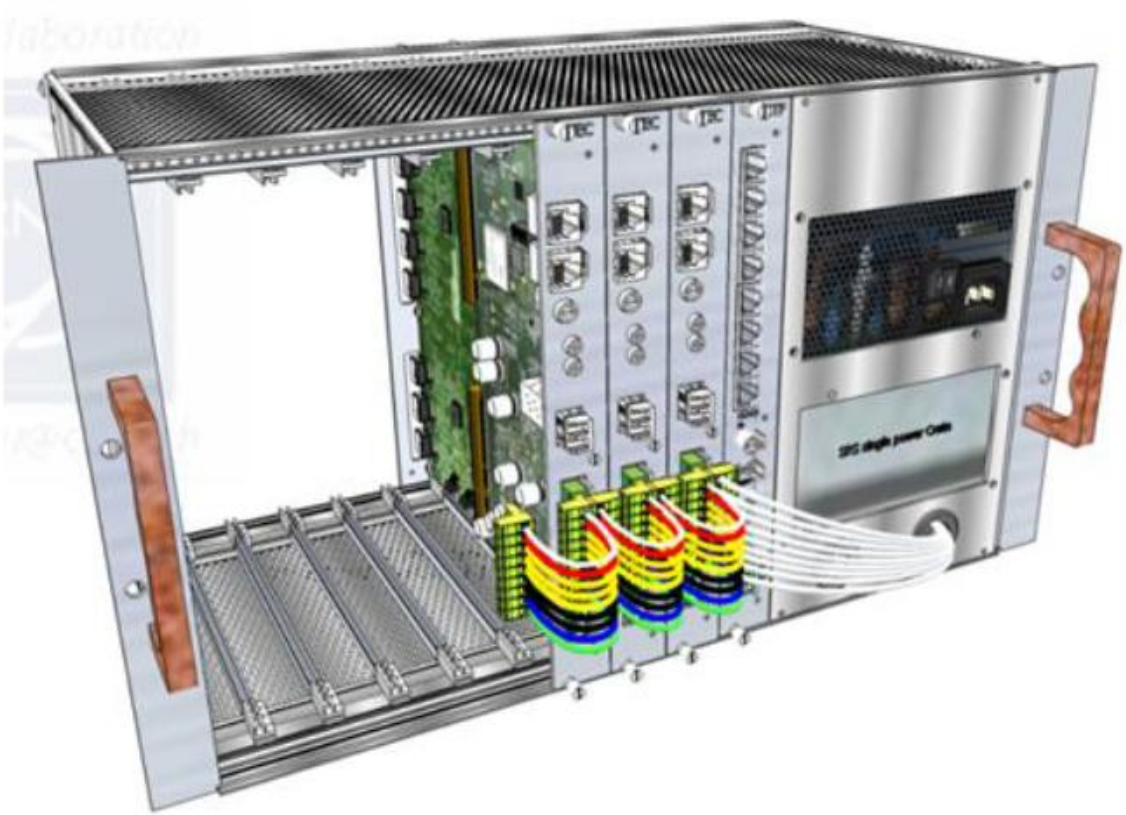
• A growing base of users and developers helps to reduce development, production and maintenance costs

**SRS comes in two flavors**:

- Classic: 6U Eurocard FECs in a 19" crate
- ATCA: industry standard, certified (coming in Q1 2013)

The big clients (ATLAS, CMS) want to go ATCA, so this becomes the right bet for us…

# SRS Classic



- 6U Eurocard FECs in a 19” crate: cooling and power not included in the crate
- Cheap solution (crate costs almost nothing, FEC ~2.5k€, 16-ch ADC card ~700€)
- Currently produced by a Greek company (Prisma) for CERN stores, but we made, and we can still make, our own production batches (design rights have not been transfered!)

# SRS Classic


Front-end → Adapter card + FEC (Front-End Concentrator) → DATE online system LHC ALICE

# SRS Classic – the FEC module

## Current FEC

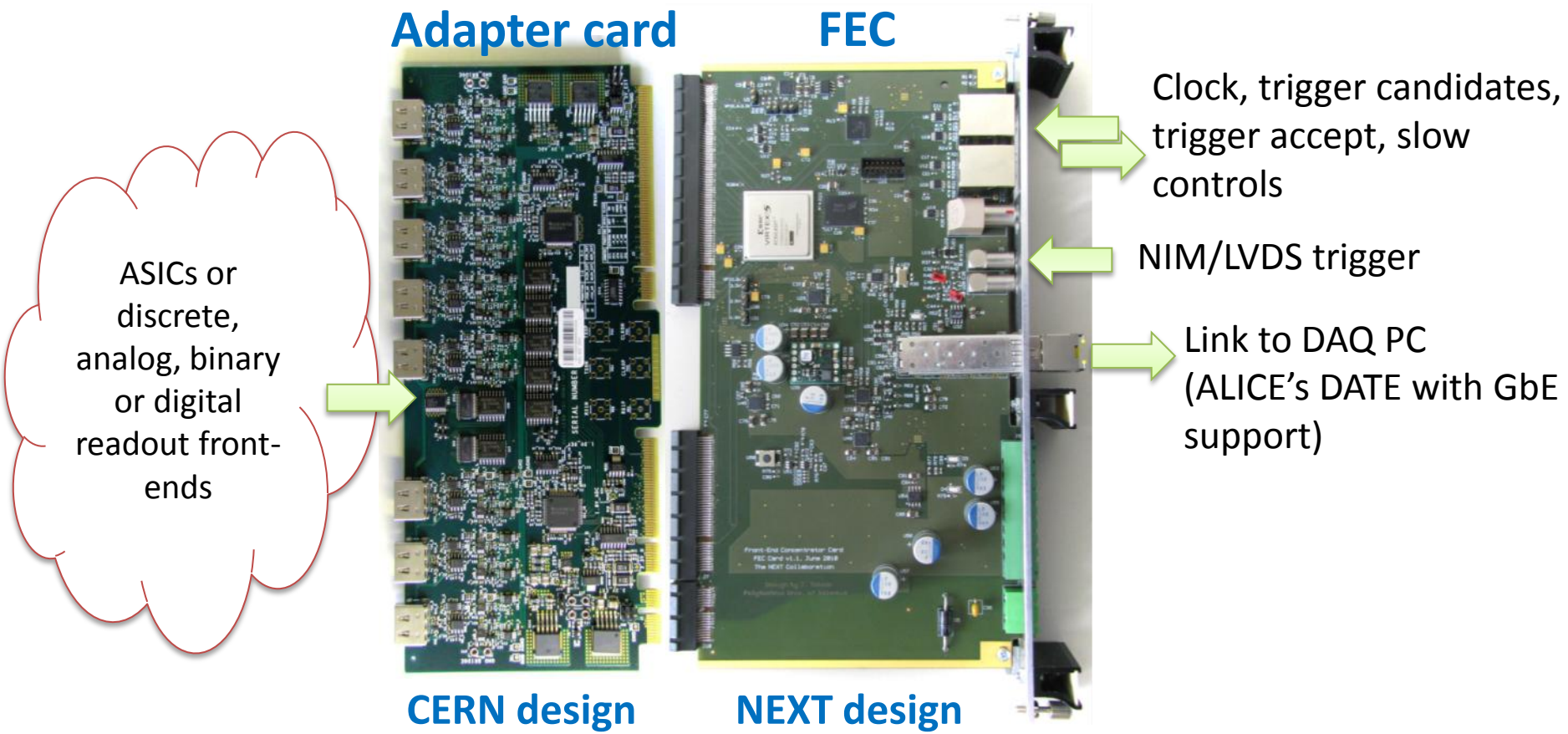
- Virtex-5 LX50T FPGA
- 256 Mbyte DDR2 buffer (16 bit interface)
- 1x SFP for GbE interface
- Switched regulator for FPGA core voltage
- Schematics, PCB design and some production batches: NEXT

## Features for the next version (in ATCA flavor)

- Virtex-6 LX130T/195T/240T FPGA
- Up to 4 Gbyte DDR3 buffer (64 bit interface)
- Dual/Quad SFP+ interfaces (allows Ethernet slows controls)
- Linear regulators for FPGA core voltage (required for operation in high magnetic field)

# SRS Classic – FEC+adapter card

This solution (base FEC + adapter cards) allows to interface any front-end to a common DAQ by simply using the right adapter card

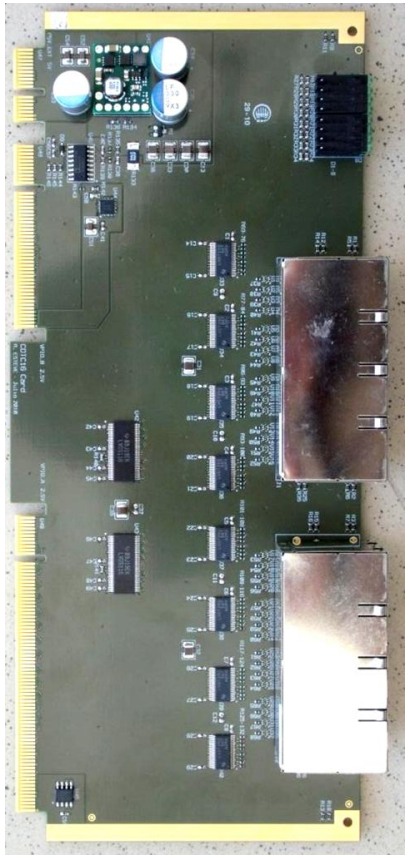


# SRS Classic – Adapter cards

**CERN ADC-Card**, can be used as:

- 16ch 12-bit 50-MHz ADC card
- Interface to the RD51 APV25 ASIC hybrid
- Interface to the RD51 Beetle ASIC hybrid

Application in NEXT-DEMO: PMT readout



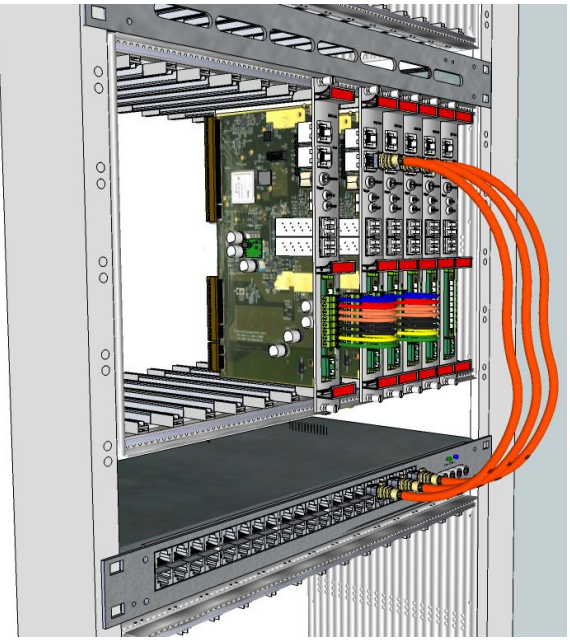
**NEXT LVDS card**, 16xRJ45, 4xLVDS each
Used as:

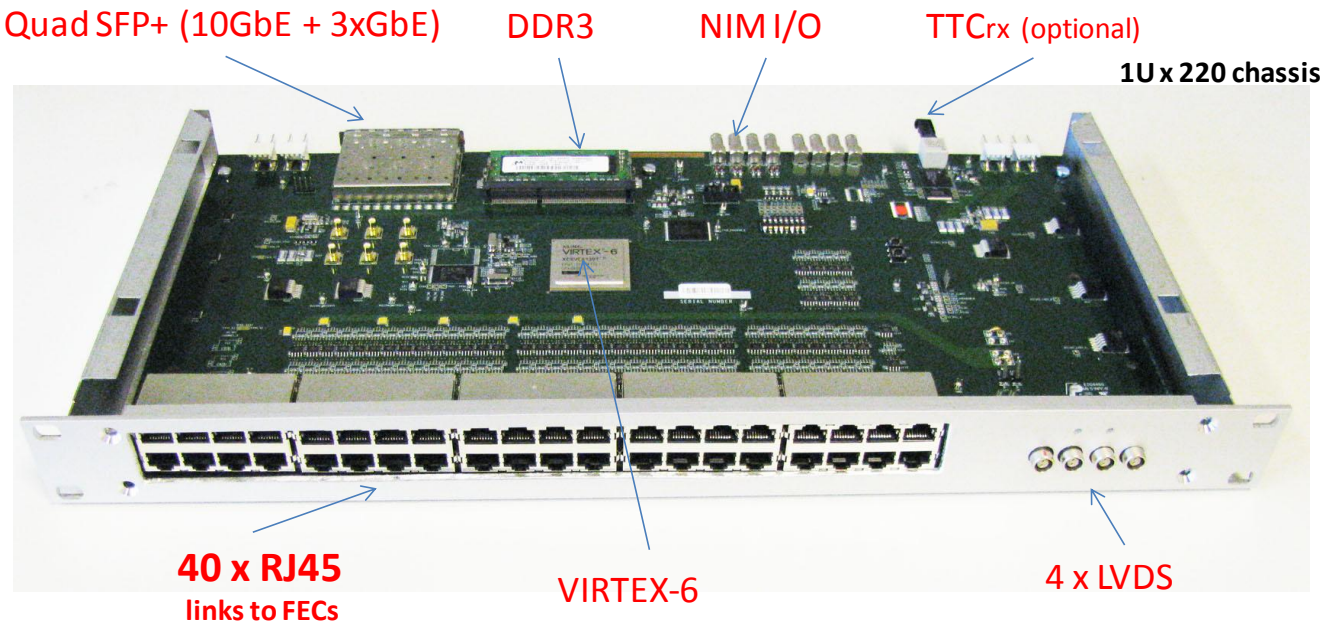
- Interface to digital front ends (SiPM)
- Clock and trigger interface & distribution

# SRS Classic – the SRU unit for large systems

One SRU will arrive in Valencia before Christmas in order to practice:

- 10 Gb Ethernet links to DAQ, DDR3 buffer, Virtex-6 features
- Possibilities: tracking plane readout with new electronics in NEXT-DEMO++, trigger module



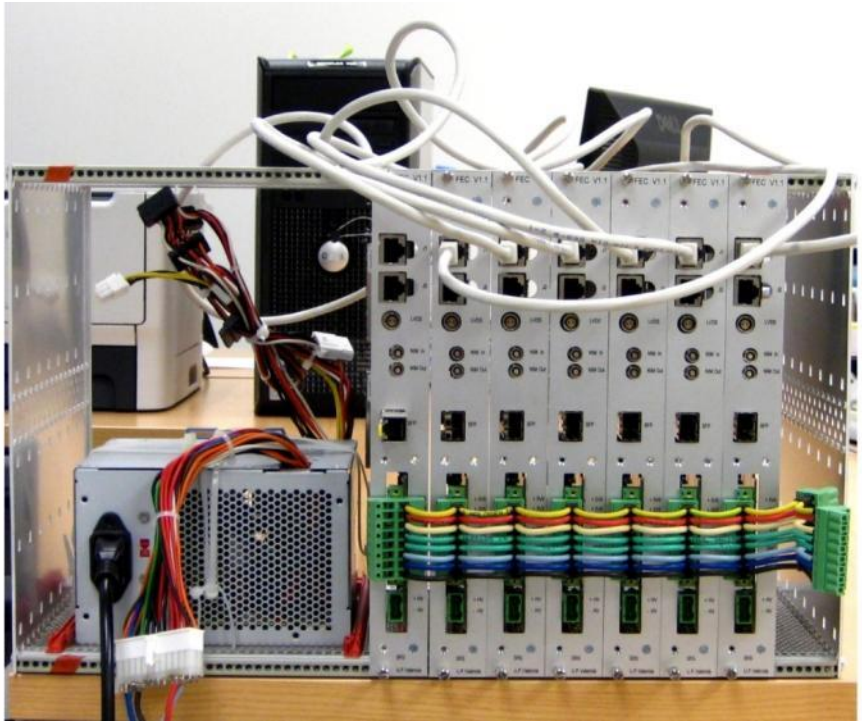



Front-end → Adapter card + FEC (Front-end Concetrator) → **SRU unit** → Online system ALICE DATE

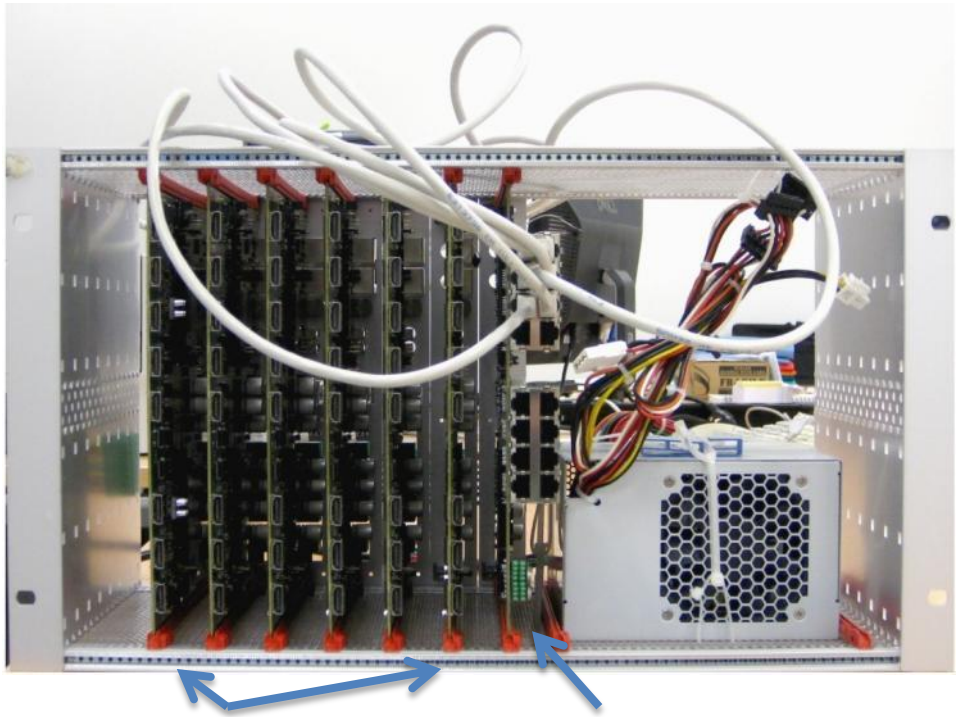
# SRS Classic
# Reading out 48 PMTs in NEXT-DEMO

Clock, trigger and commands sent from Trigger FEC to DAQ FECs
Trigger FEC communicates with a PC via GbE

Front view

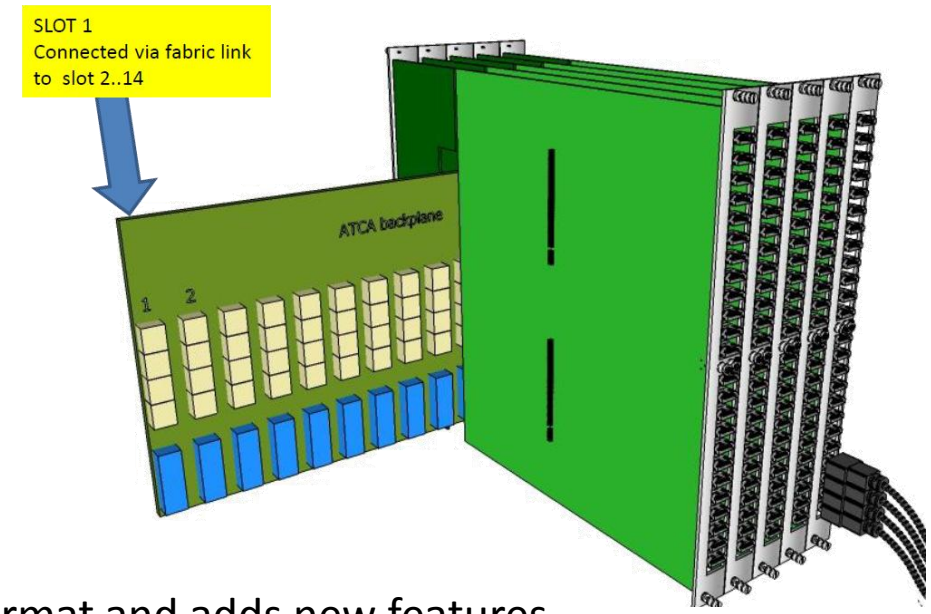


Rear view



# SRS ATCA

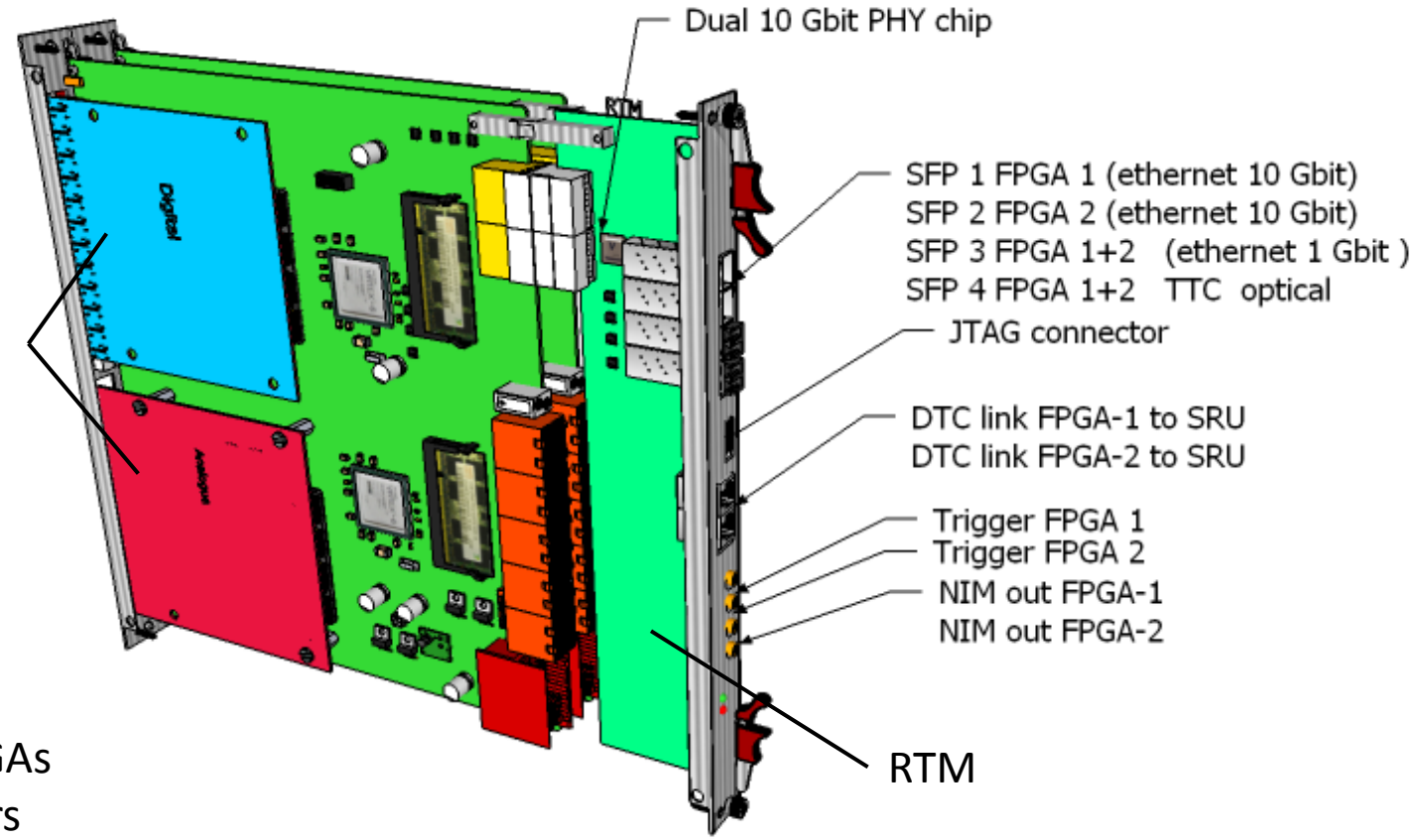
SRS-ATCA partners*: EicSys, UPV-Valencia, IFIN-HH-Bucharest, CERN




- Remaps current SRS cards into ATCA format and adds new features
- Cooling and power included in a certified crate
- Required by large experiments (CMS, ATLAS)
- More expensive solution, designed and produced by a German company
- Our special RD51 developer and early user status (together with ATLAS and ORNL) gives us access to reduced prices and influence on the final design
- Coming in Q1 2013

# SRS ATCA – the FEC module

New
ADC card
or
CDTC16 card




- 2x mezzanines
- 24 ADC ch/FEC
- 2x Virtex-6 FPGAs
- 2x DDR3 buffers
- 4x SFP+ in rear module
- Dual FEC mode: each FPGA controls a mezzanine, DDR3 bank, DTC conn. and 2x SFP+
- Single FEC mode: FPGAs are interconnected

# A possible architecture for NEXT-100

## Requirements

- **6800 SiPM channels**
  - 54x 128-ch FE cards
  - New clock distribution to reduce the number of cables
  - New mode of operation: Trigger mode with internal buffer at the FE level
- **64 PMT channels**

- **Dead Time < 2%**
- **Zero Suppression** to reduce the event size
- Maximum total waveform length : **3.2 ms** – 2 x chamber size
- Maximum throughput (goal)**: 70-80 MBytes/s?**

# A possible architecture for NEXT-100

## Zero-suppression

- We cannot send to disk raw data at the target event rate (10Hz):
  - ~600 MByte/s could be reached (>400MByte/s in the SiPM plane!)
  - **Zero suppression is needed**!
- So, what can be done?
  - **Test Mode**:
    - PMT plane: Raw data
    - SiPM plane: Zero-suppressed data
    - Trigger rate limited to 1-2 Hz
  - **Normal mode**:
    - Higher trigger rate:  up to 10 Hz
    - PMTs:
      - **Events of interest (in a defined range of energy): Raw mode data**
      - Rest of events: zero-suppressed data
    - SiPM plane: Zero-suppressed data

# A possible architecture for NEXT-100

## Simulations

- A VHDL model for the NEXT-100 DAQ system has been written to simulate the **Normal Mode** of operation in the worst case. Assumptions:
  - Treatment of “interesting events”: 1% of the events
  - Total waveform length of 3.2 ms
  - Trigger rate of 10 Hz
  - Sampling rates:
    - PMT channels: 40 MHz
    - SiPM: channels: 6 MHz (although it may be 2-3 MHz in the final HW)
  - Zero-suppressed data reduction factor (pure speculation) :
    - PMT data: 1/4
    - SiPM data: 1/20

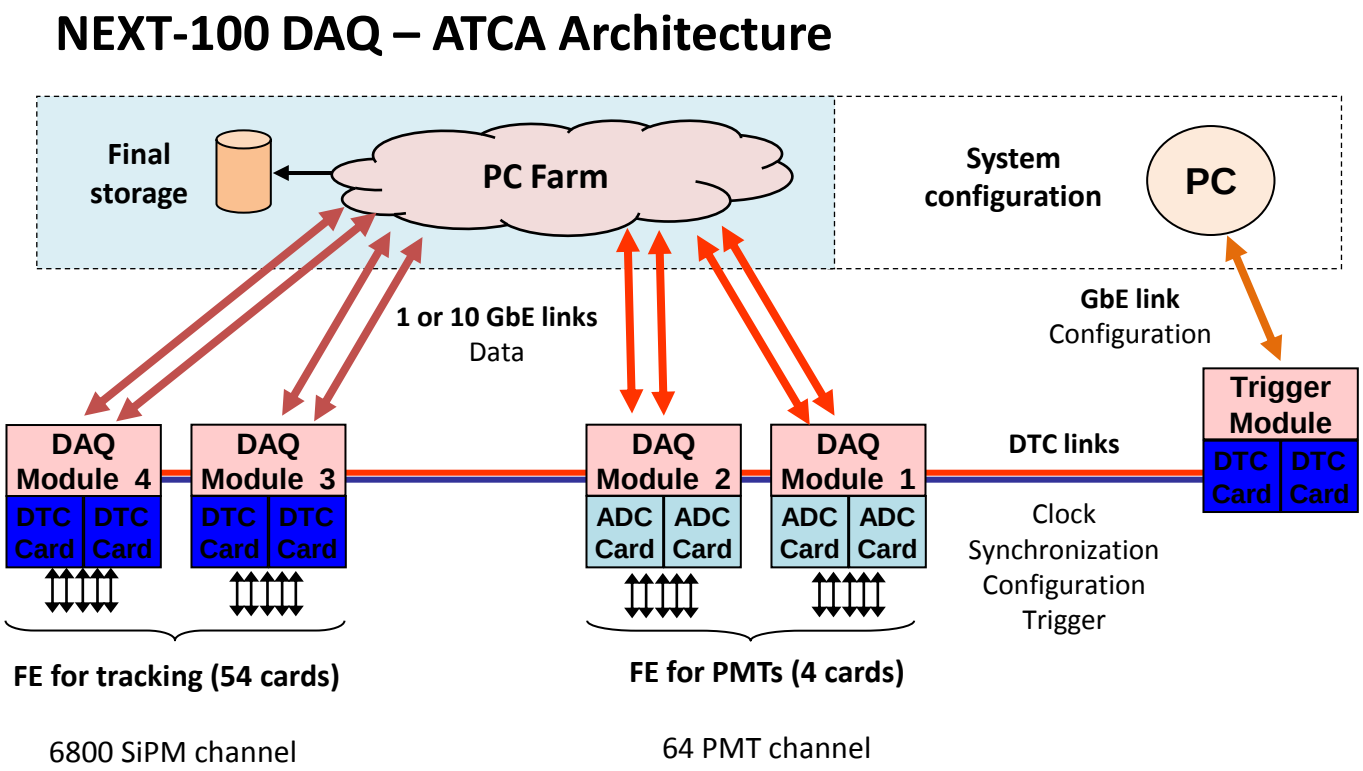
# A possible architecture for NEXT-100

## Simulations

- Conclusions:
  - Normal mode of operation as described could satisfy the needs of NEXT-100 in terms of dead time
  - At least 2Gb/s throughput per FEC is required (so, 10GbE in the new ATCA FEC will be welcome)
  - A double buffer scheme reduces considerably the dead time (so, fast DDR3 buffers in the new ATCA FEC is a must)
  - Giving priority to events of interest reduces the dead time for this type of events to almost zero

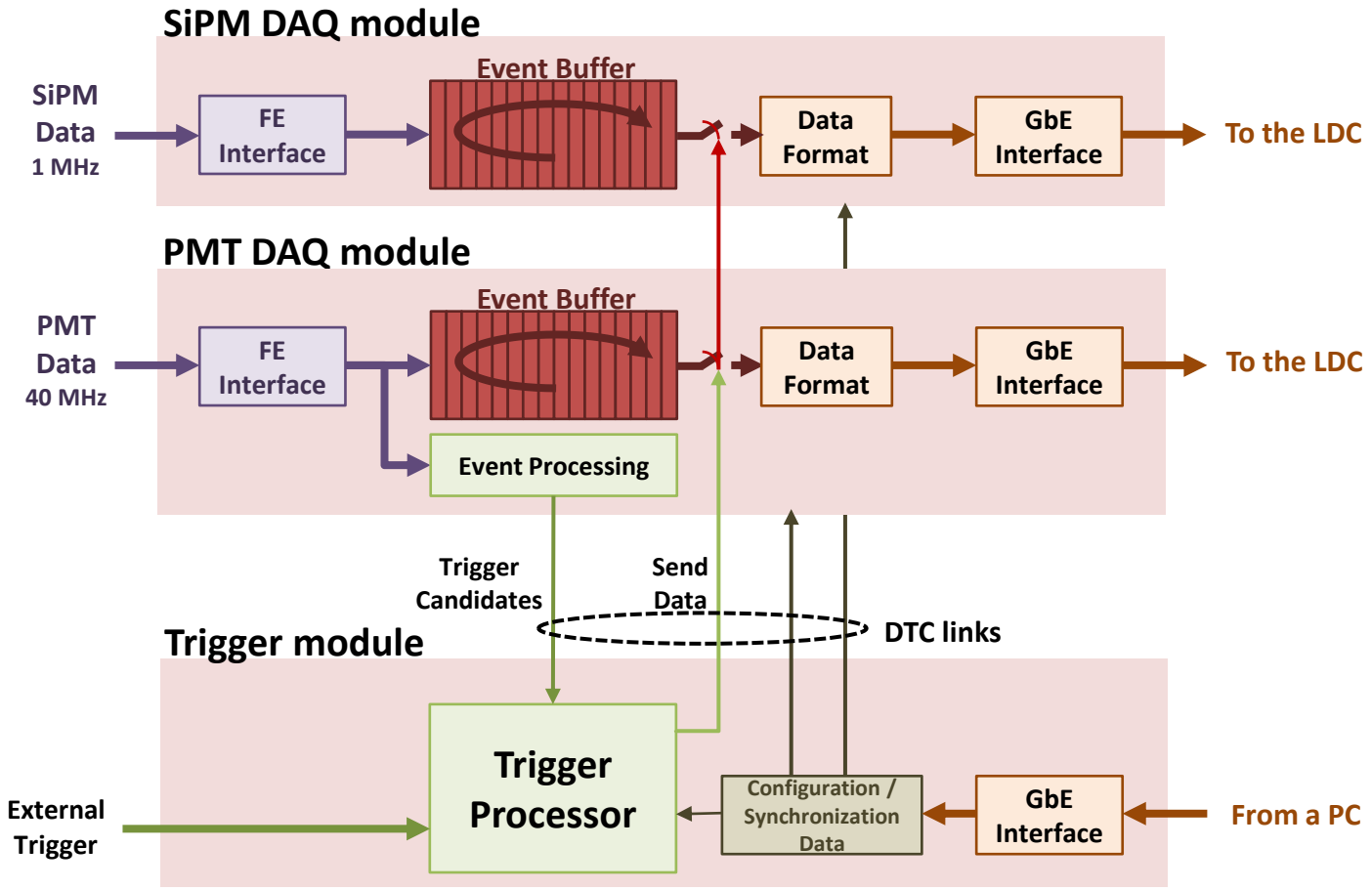
# A possible architecture for NEXT-100

## Single ATCA chassis with 5x FECs



# Trigger architecture

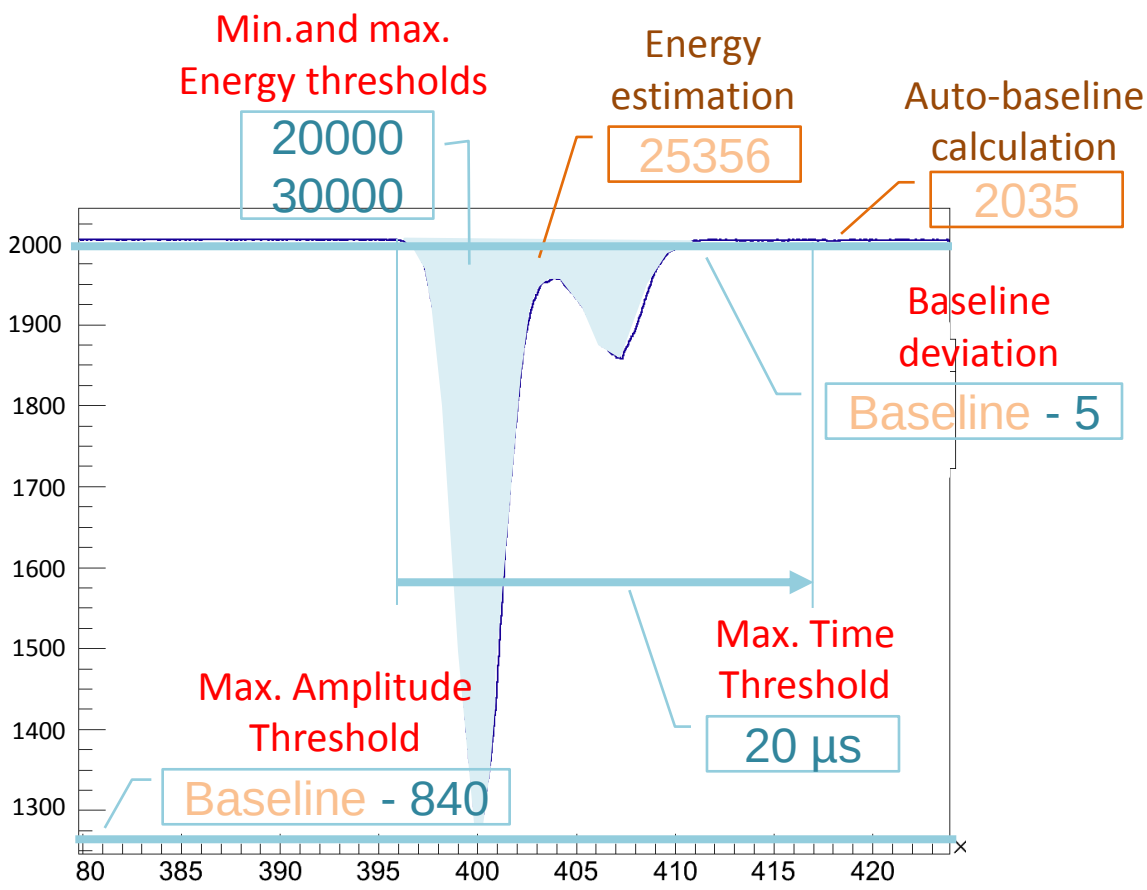
(1) PMT DAQ modules send trigger candidates to the Trigger module
(2) A configurable trigger algorithm takes a decision
(3) A trigger accept is distributed to all DAQ modules



# Trigger candidates

- Configurable (in red):
  - Channel for trigger on/off
  - Auto-baseline calculation on/off
  - Trigger event type: 1 or 2
  - Max and min energy
  - Relative max amplitude threshold
  - Relative baseline deviation
- Internally processed (in blue):
  - Baseline
  - Energy of the pulses
- Algorithm:
  1. Channel ON?
  2. Pulse bellow baseline deviation threshold? → Process event!
  3. Event max. amplitude < max. amplitude threshold?
  4. Event time duration < max. time threshold?
  5. Event energy among energy threshold?
  6. If 1-2-3-4 and 5 → Trigger candidate!
- After detection, trigger candidate info is sent to the TRG FEC: Initial time of the event (FT), channel number and event type

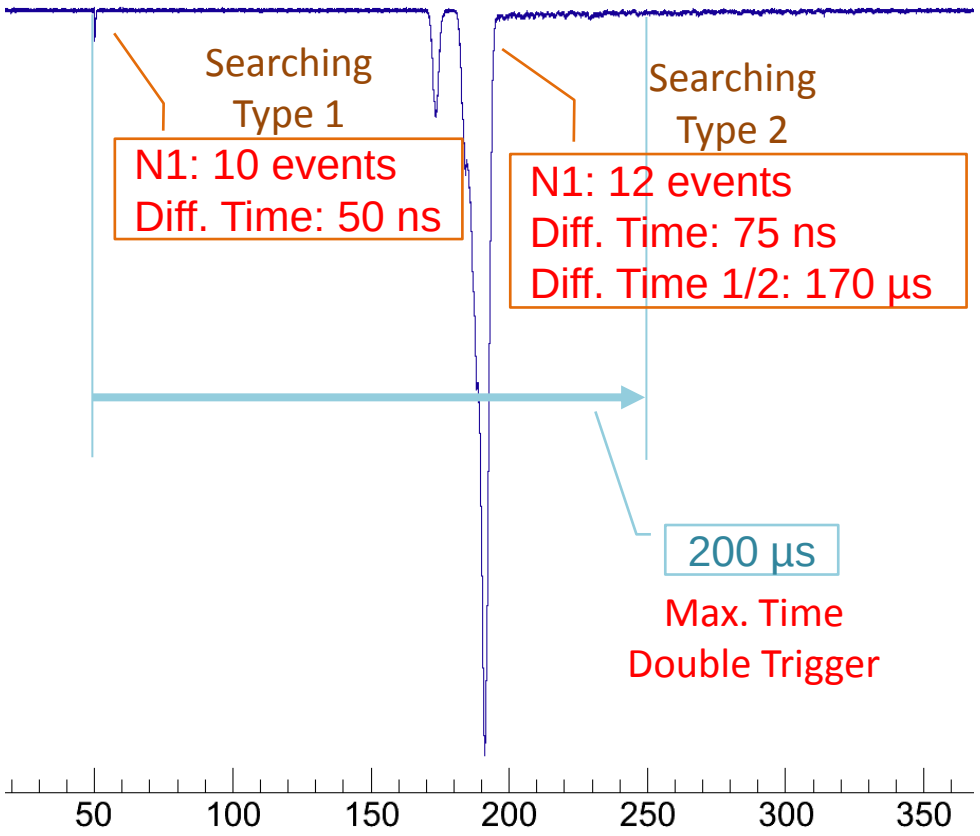
**Internal trigger mode of operation (For every PMT channel)**



# Trigger algorithm

## TRG FEC processing algorithm

- **Configurable (in red):**
  - Pre-trigger and maximum trigger frequency
  - Trigger mode:
    - External
    - Internal simple (event type 1)
    - Internal double (event type 1 and 2)
    - Calibration (external and internal)
  - Trigger candidates for a trigger (N1 and N2)
  - Coincidence window size (CW1 and CW2)
  - Max. time between event type 1 and 2
- **Internal trigger algorithm:**
  1. Number of trigger candidates (type 1) > N1?
  2. Trigger candidates time diff (type 1) < CW1?
  3. If 1 and 2 and Internal simple mode → Trigger accept! → If Internal double mode, go to 4:
  4. Number of trigger candidates (type 2) > N2?
  5. Trigger candidates time diff (type 2) < CW2?
  6. Time between trigger1 and 2 < Max. time double trigger?
  7. If 1-2-3-4-5 and 6 → Trigger accept!
- After detection, trigger accept info is sent to the DAQ: Trigger mode, trigger counter, CT (coarse Timer) and FT (Fine Timer)




| | |
|---|---|
| CW1:100 ns | N1: 5 events |
| CW2: 150 ns | N2: 8 events |