Quality Control for ATLAS Phase 2 Inner Tracker Upgrade at The University of Oklahoma

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Introduction

- To prepare for the High-Luminosity LHC (HL-LHC), the ATLAS Experiment will replace its tracker system with an all-silicon Inner Tracker (ITk) as a part of the Phase 2 upgrade.
- The ITk system is composed of pixels and strips. The University of Oklahoma (OU) will focus on the pixel system
- The pixel system is composed of modules. Each modules consist of
  - Printed circuit board (PCB)
  - Silicon sensor
  - Front end (FE) chip (three or four per module).
- OU is doing quality control (QC) tests of both PCBs (bare and populated) and assembled modules

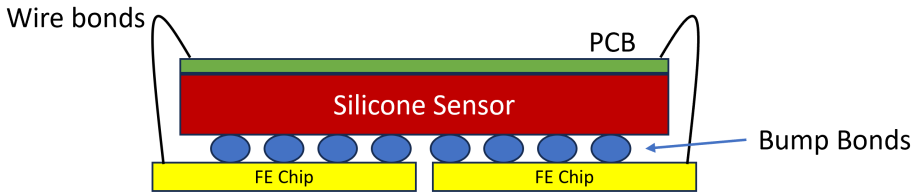

Figure: Structure of an assembled module

Introduction

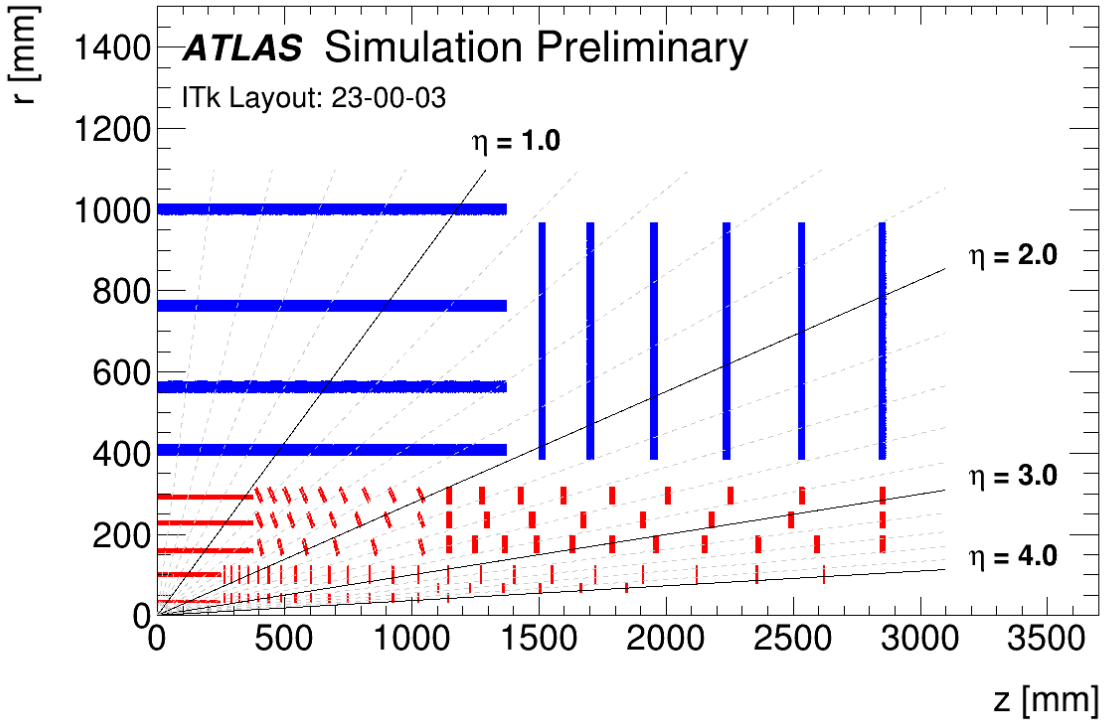

Figure: Layout of the ITk (CDS). The ITk will give extended coverage from $\eta <$ 2.5 to 4.0

QC of PCB

- QC is done on the PCB before it is assembled into a module
- OU is qualified to do the following PCB tests:
  - Thickness measurement
  - Visual inspection (manual method)
  - Low-Voltage/High-Voltage (LV-HV) test
- OU is also developing an automated visual inspection method using convolutional neural network (CNN) algorithm

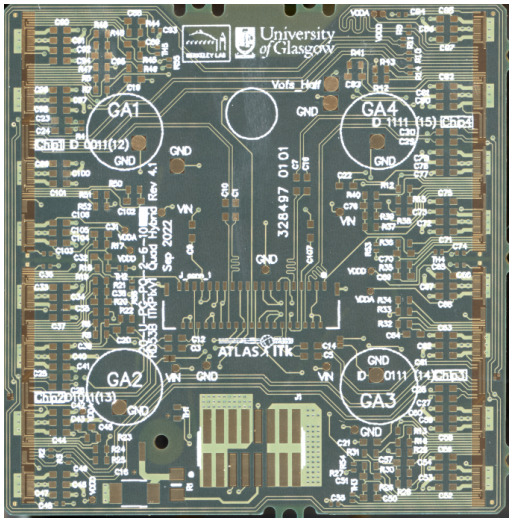

Figure: PCB (bare)

QC of PCB: Thickness Measurement

- Ensure that each of the six layers of the PCB are within specification
  - Thickness of copper layer contribute to power budget
- Procedure: probing sample layer on the frame (not directly probing the PCB)

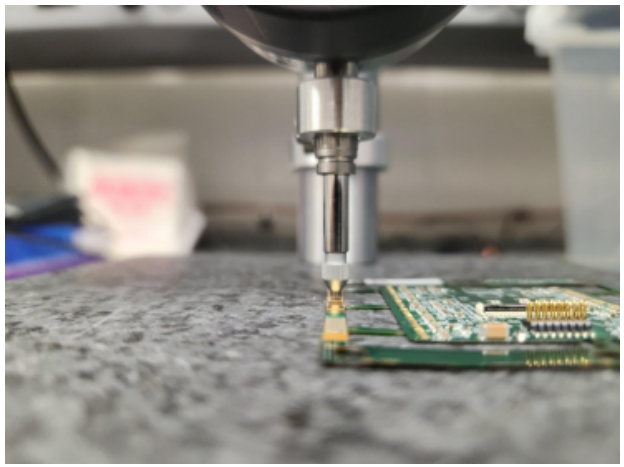

Figure: Thickness measurement procedure using a dial gauge

QC of PCB: Visual Inspection

- Ensure that there are no visible defects on the PCB
- Procedure: take high-resolution picture of PCBs, manually scrutinize, and mark any defects on the PCB
  - Among the most important defects are missing components and scratches and solder spills on wirebonding pads

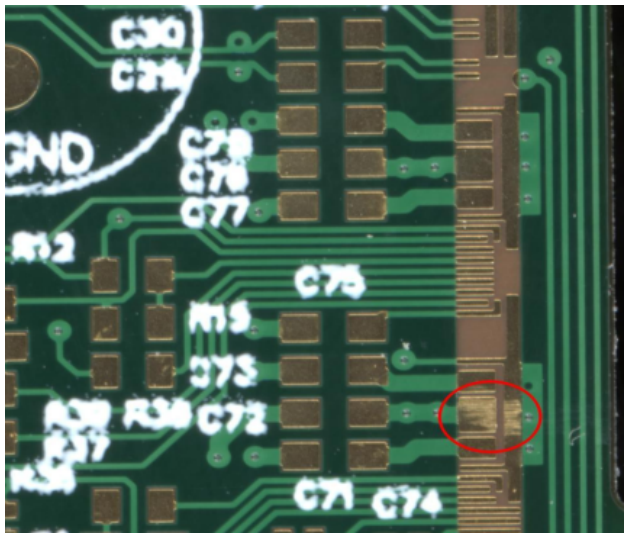

Figure: Example of a defect during visual inspection

QC of PCB: LV-HV

- The test: probes three different PCB characteristic quantities:
  - Leakage current of the high-voltage capacitor in the PCB (HV)
  - Copper layer resistance of the PCB (LV)
  - Sensitivity of the temperature sensor (NTC value) (LV)
- Procedure: connect PCB to a frame with pogo pins, which then is connected to PicoLog data logger to take voltage measurements
  - LV tests are done by simply connecting a PCB to a current supply and measuring voltage to calculate resistance
  - Leakage current measurement (HV) are done by connecting high-voltage source to a PCB (charging the high-voltage capacitor), waiting 15 minutes for the current to decay, and measuring the leakage current output

QC of PCB: Developing Visual Inspection using CNN

- The current visual inspection procedure relies on manual inspection of each PCB (could take up to 15 minutes per PCB)
- Automating the procedure: use machine learning (CNN) to inspect defects
- Strategy (inspired by CMS paper [DOI 10.1088/2632-2153/aced7e]):
  - Take picture of PCB with controlled conditions (alignment, lighting, etc)
  - Preprocess image to remove excess variations
  - Partition of image into segments
  - Equalizing lighting level with referenced "ideal" PCB picture
  - Use CNN-based encoder and decoder
    - Subtract the output of the decoder with the input picture to highlight defect
  - Use anomaly detection classifier to identify defect

QC of Modules

- If a PCB passes QC tests, the PCB will be assembled into a module. Further QC is required on modules
- OU is currently a backup site for module testing:
  - Module electrical testing
  - Thermal cycling
- Aside from testing, OU is also a backup site for parylene coating of the modules

QC of Modules: Electrical Testing

- Ensure that the sensor, FE chip, along with the entire module work properly
- Using an internal calibration system, the performance of every component of the module, including the pixels in the sensor, is evaluated
- The test is done in warm ($20°$C) and cold ($-15°$C) temperature

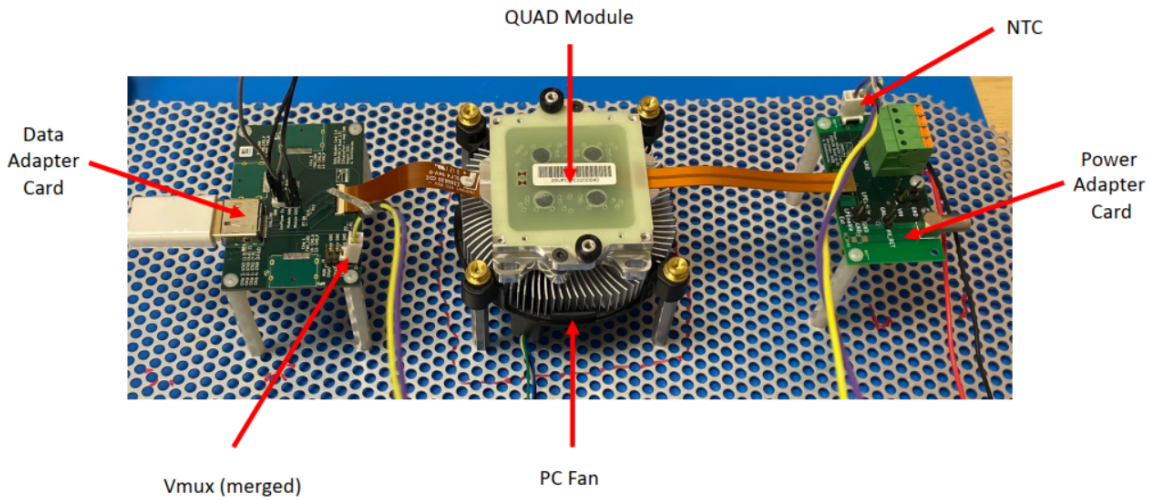

Figure: Setup of module electrical testing

QC of Modules: Parylene Coating

- Parylene coating is the process of coating the module with a thin film of dielectric parylene
- It is done to prevent electrical discharge between sensor and FE chip, and to physically protect the wirebonds

Figure: Parylene coating machine

QC of Modules: Thermal Cycling

- After parylene coating, the module will undergo several endurance testing stages before being electrically tested once again. One of them is thermal cycling
- The test is done by cycling the module between hot and cold temperatures to cause mechanical stress (due to differences in thermal coefficient)
- Temperature is regulated using peltier thermoelectric heat pumps with a chiller system

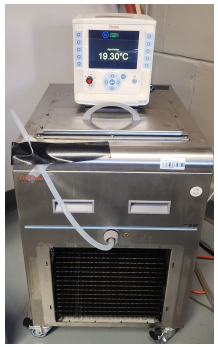

Figure: The chiller used along the peltiers to heat/cool modules

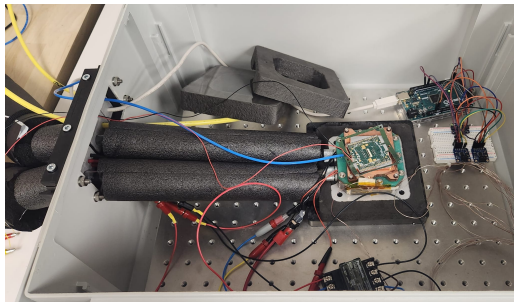

Figure: The setup of the thermal chamber where the module get heated/cooled

Conclusion

- OU is ready to carry out QC tests on PCBs for the ATLAS ITk Phase 2 upgrade
- A CNN method of PCB visual inspection is in development to improve and automate the QC
- OU is also ready support module QC testing as a backup site

Backup Slide: Visual Inspection using CNN

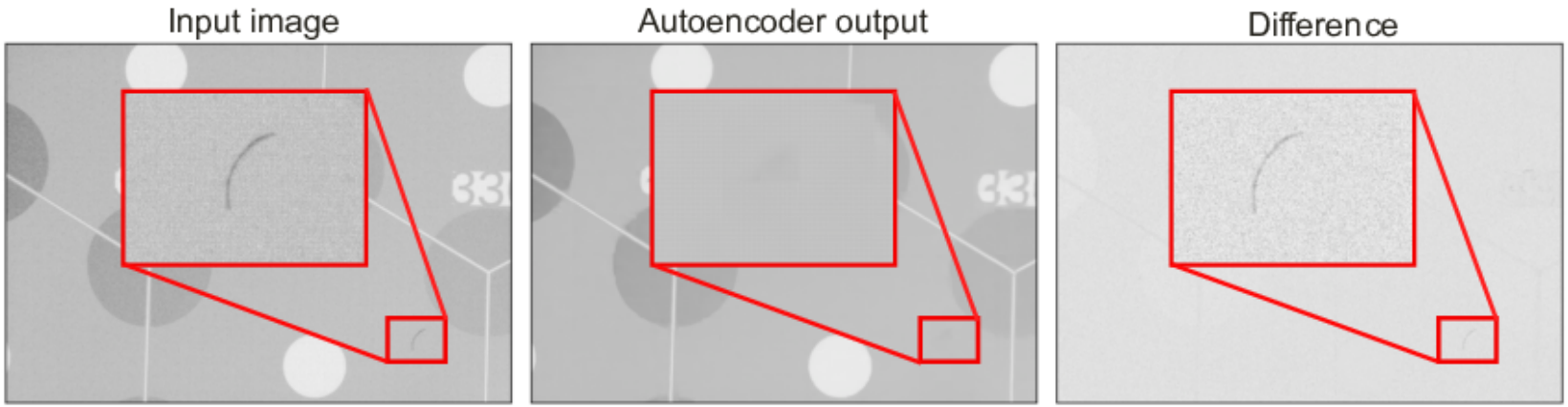

Figure: Picture encoding and decoding procedure (CDS)