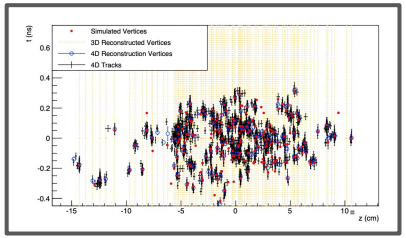
Electronics Development on Endcap Timing Layer for CMS

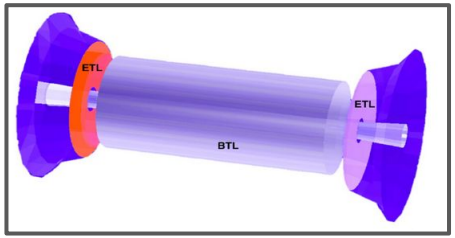
Naomi Gonzalez, Daniel Spitzbart, Indara Suarez

BOSTON UNIVERSITY

Introduction

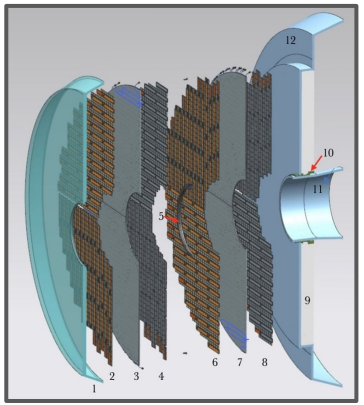
- LHC is expected to have an upgrade to the High-Luminosity LHC (HL-LHC) by 2026.
- Higher Collision Rates → More Data
  - More Radiation; More Pile-ups
- MIPs Timing Detector
  - ~40ps timing resolution
  - Path reconstruction = hit location + time
  - Barrel Timing Layer ($\eta < 1.6$)
  - Endcap Timing Layer ($1.6 < |\eta| < 3.0$)





Endcap Timing Layer

- Disk design of ETL allows for maximum coverage in the Endcap regions of MTD
  - 32,000 silicon LGAD sensors
  - 32,000 ETROCS bump-bonded to LGAD sensors
  - 12,480 Service Hybrid Board (SH)
    - Power Board (PB)
    - Readout Board (RB)
    - Module PCB



- Geometrical constraint →thickness of detector is 4.5 cm

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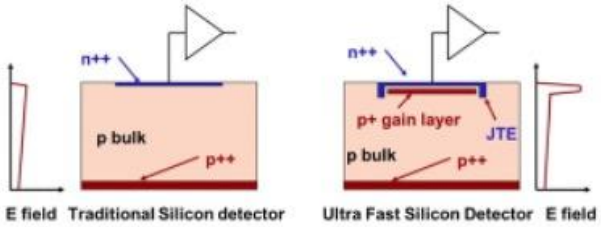
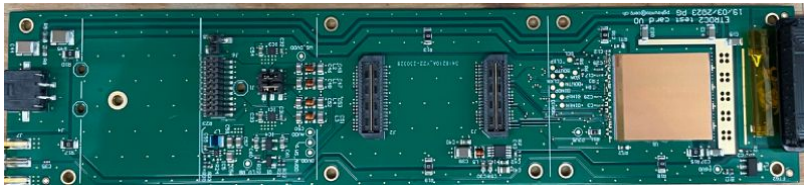
LGAD

- Low Gain Avalanche diode: Ultra fast silicon detector
- Threshold charge gain of 10-30



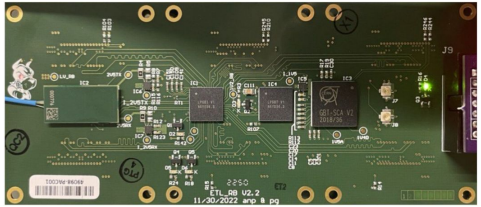
ETROC

- Endcap Timing Readout Chip
- Converts charged signal to digital signal
- Stores precision timing data on hit



Readout Board

- Controls uplink and downlink data to and from ETROC and DAQ
  - Up to 28 ETROCs can be controlled with 1 RB
- Monitors temperatures, and voltages of other front-end electronics
  - Calibration of Electronics
- Slow + Fast Control



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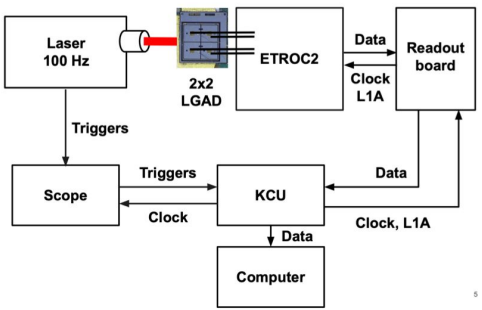
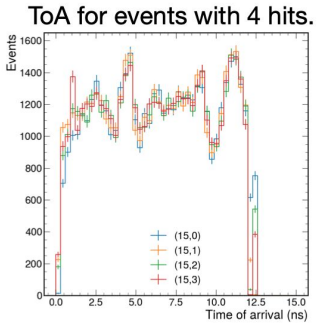
Test Stand

- Test the Integration of front-end electronic detector components (LGAD + ETROC + RB + PB)
- Laser Studies Testing (Fermilab set-up)
  - External Trigger signal (L1A)



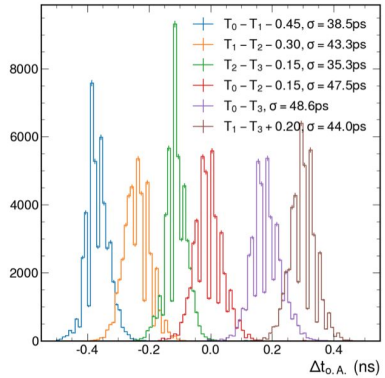


Initial Results

- Can successfully read and collect Time of Arrival Data (TOA)
- Use ΔTOA to calculate system timing resolution

$$\sigma_i = \sqrt{0.5 \cdot \left(\sigma_{ij}^2 + \sigma_{ik}^2 - \sigma_{jk}^2\right)}$$

	(15, 0)	(15, 1)	(15, 2)	(15, 3)
σ (ps)	30	25	30	26



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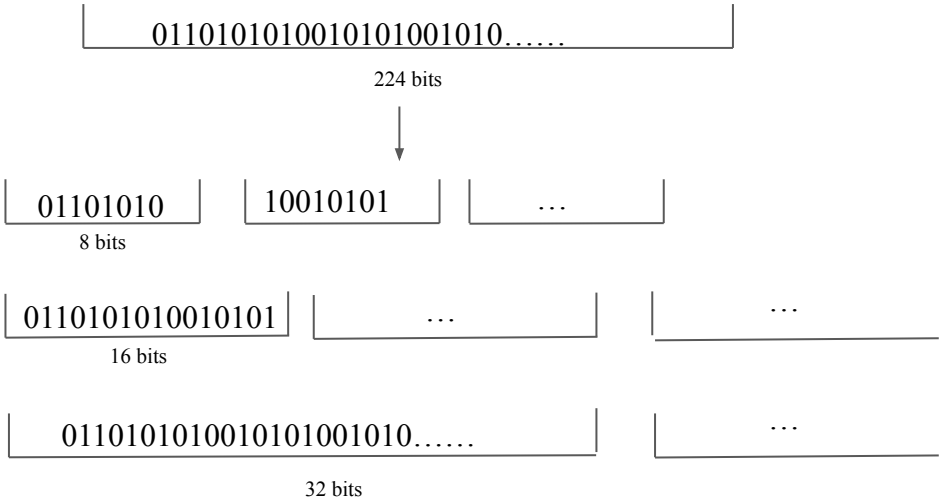
Self-Trigger

- Decodes trigger data stream from ETROC with adjustable bitslip: Send trigger (L1A)
  - Realtime Data Rate Switch (320, 640, 1280 Mbs)



Initial Results

- Successful Firmware Build and initial integration with software
- Tigger rate at about 1Hz
- Initial bitslip working