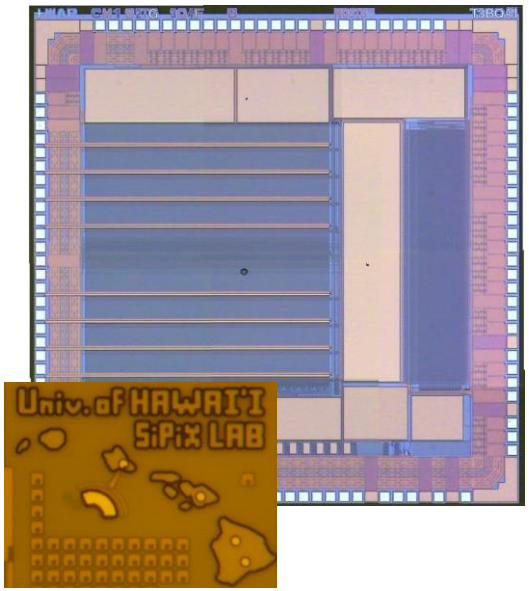
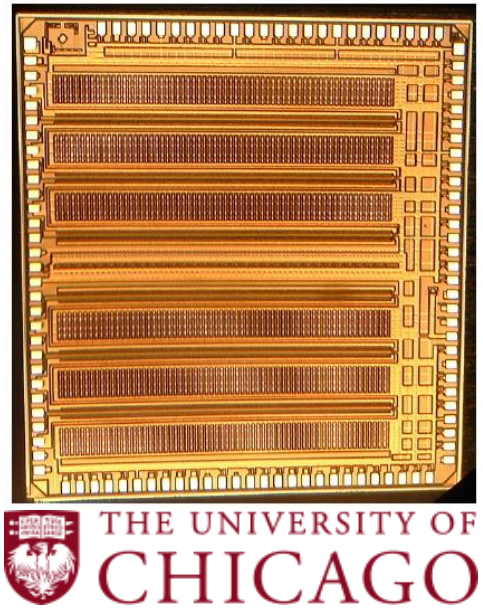
Custom ASICs



Kurtis Nishimura*
SLAC

Cosmic Frontier Workshop
March 7, 2013



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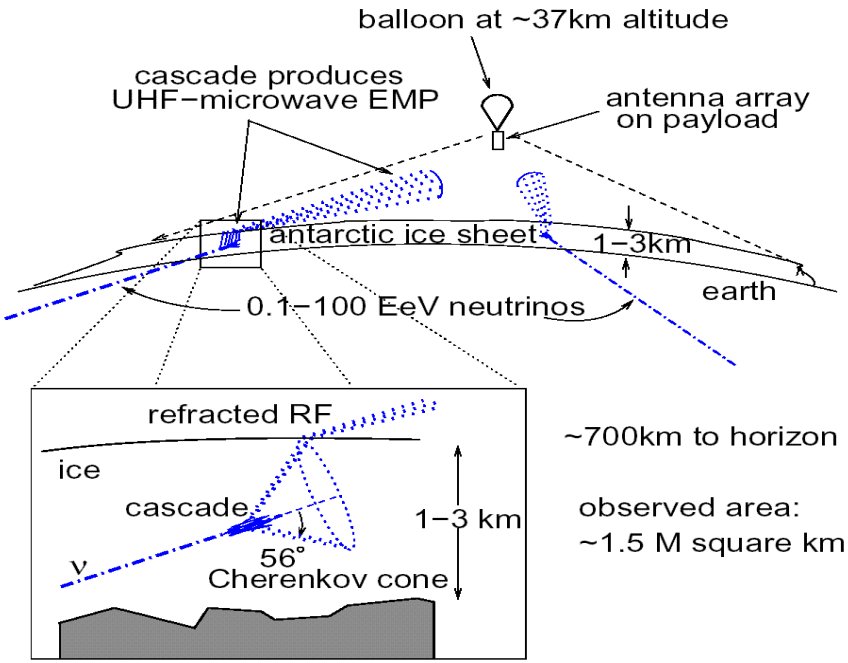
*with contributions from U. of Hawaii, U. of Chicago, SLAC

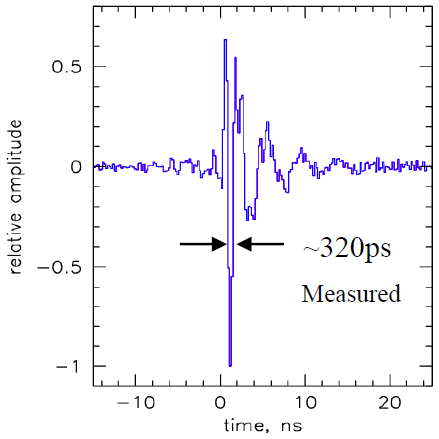
Custom ASICs

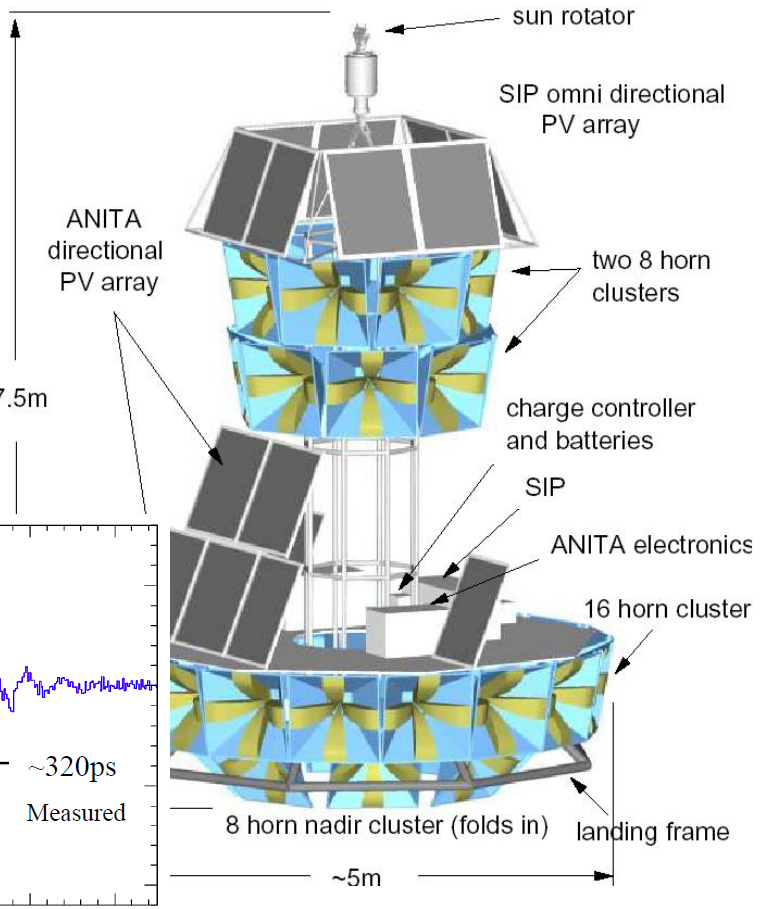
- A potentially extremely broad topic…
  - I will speak to my experience with **fast waveform digitizers**.
  - Typical* features of such ASICs:
    - Multi-gigasample-per-second sampling rates.
    - Hundreds of MHz to GHz analog bandwidths.
    - Relatively high channel densities.
    - Relatively low power.
    - Non-continuous sampling (readout on request ➔ dead-time).
  - Some recent examples:
    - **LABRADOR/BLAB/IRS/TARGET Series [U. of Hawaii]**
    - **PSEC4 [U. Chicago]**
    - DRS4 [PSI]
    - SAMLONG/WaveCatcher [LAL,CEA/IRFU]
    - Many of these chips are already in use on running experiments, or are planned for use in next generation experiments.

Waveform Sampling for ANITA

- Large Analog Bandwidth Recorder and Digitizer with Ordered Readout (LABRADOR) [arXiv:physics/0509023]
  - Developed (and named) by Gary Varner at University of Hawaii as the readout ASIC for the ANITA experiment.
  - TSMC 0.25 um fabrication process.



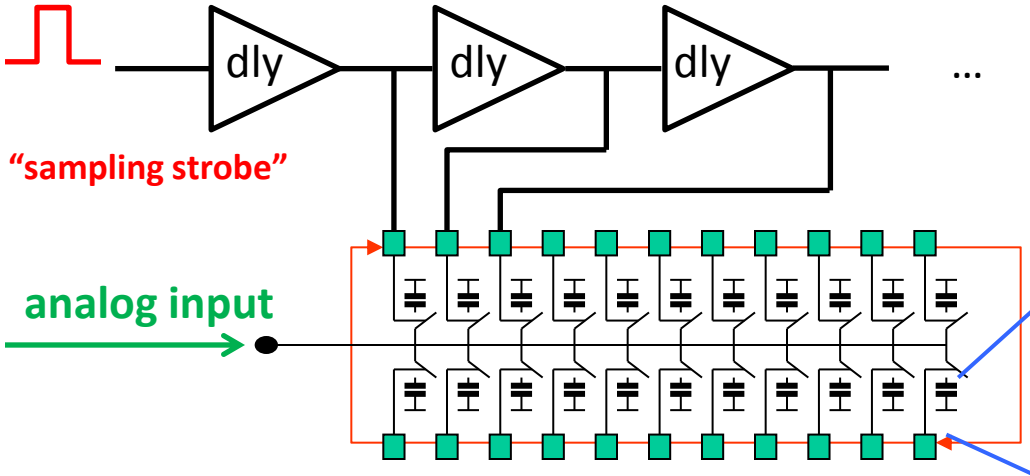


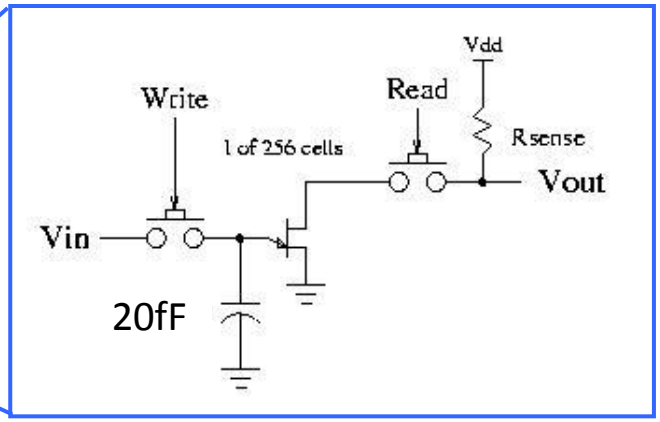


- A balloon-based ultra-high energy neutrino experiment.

➔ Requires **low power**, **fast sampling**.

Switched Capacitor Array Sampling

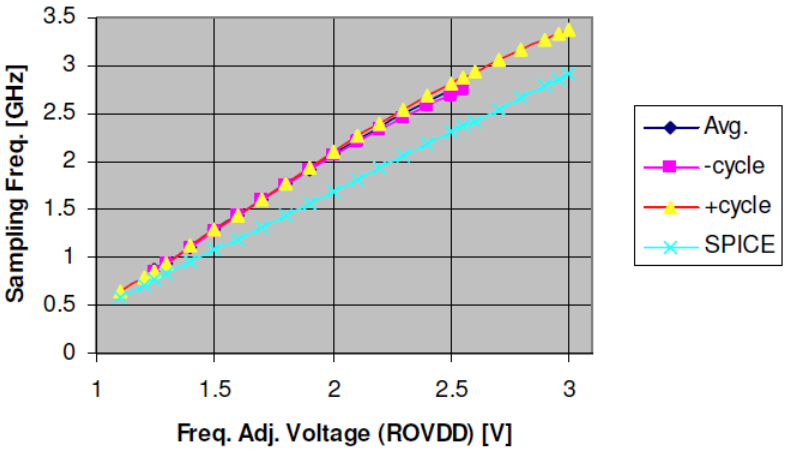




[x8 + 1 channels for LABRADOR3]

Tiny stored charge: 1mV ~ 100e$^-$

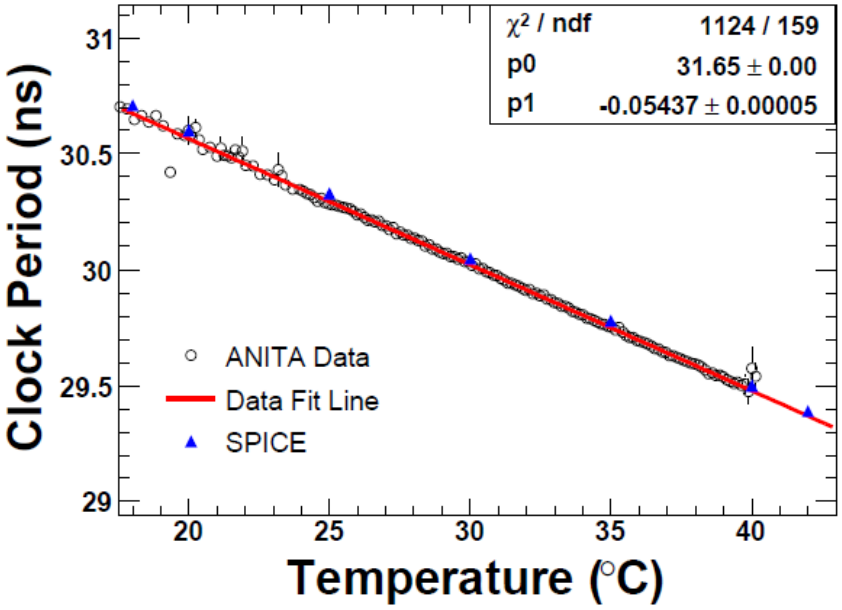
- Switched capacitor array as analog memory.
- Timing of switches controlled by delay line or **ring oscillator**:
  - Sampling rates from ~500 MHz to 3+ GHz.
  - Running the sampling is very low power - 10's of mW or less.
- Sampling stops when a system trigger is received.

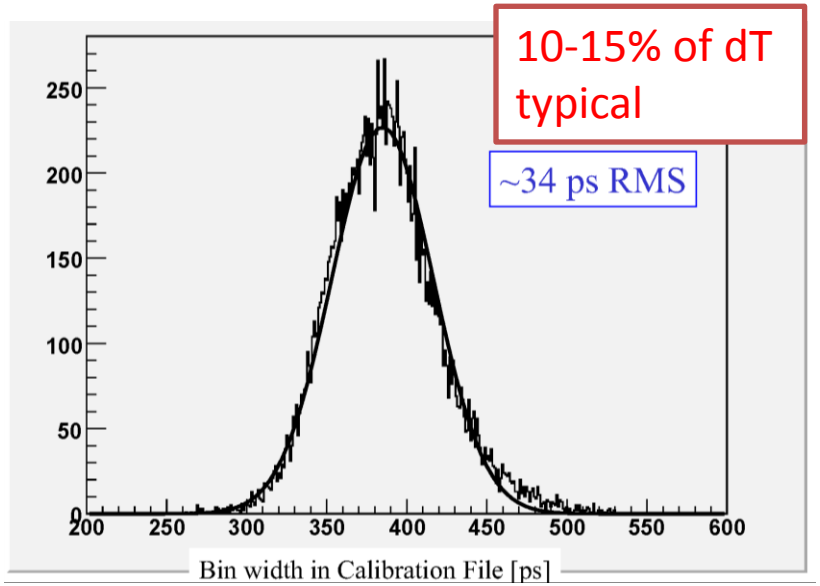


Timing (Non-)Uniformity

- Important difference from commercial ADCs:
  - Delay lines allow fast, low power sampling (not digitizing)… at the cost of timing uniformity.

1. Sampling rate drifts notably with temperature.
   - ~0.2% / °C.
   - Can monitor and servo lock.
2. Sample-to-sample offsets are not uniform.
   - Due to natural process variation between delay stages.
   - Time between samples varies by σ ~ 10-15% relative to nominal.

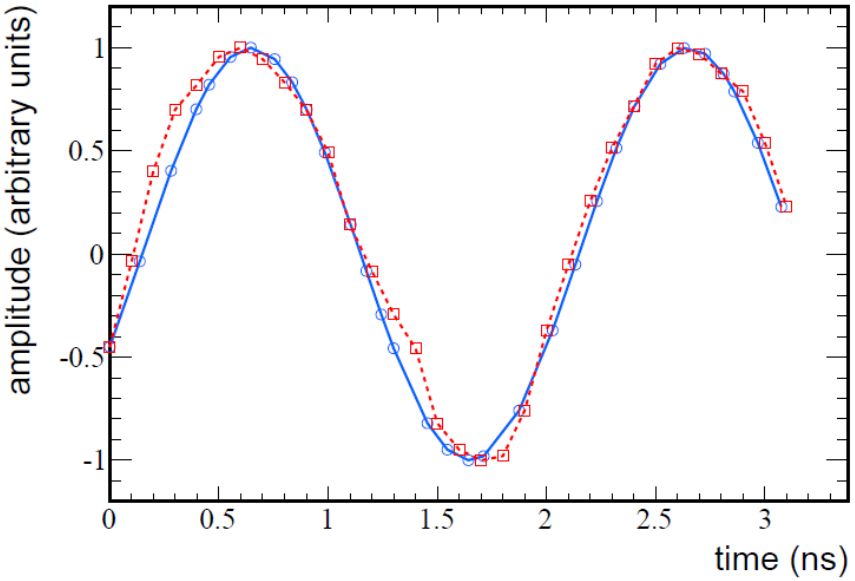




Timing (Non-)Uniformity

- Examples of misreconstruction and timing nonlinearities:

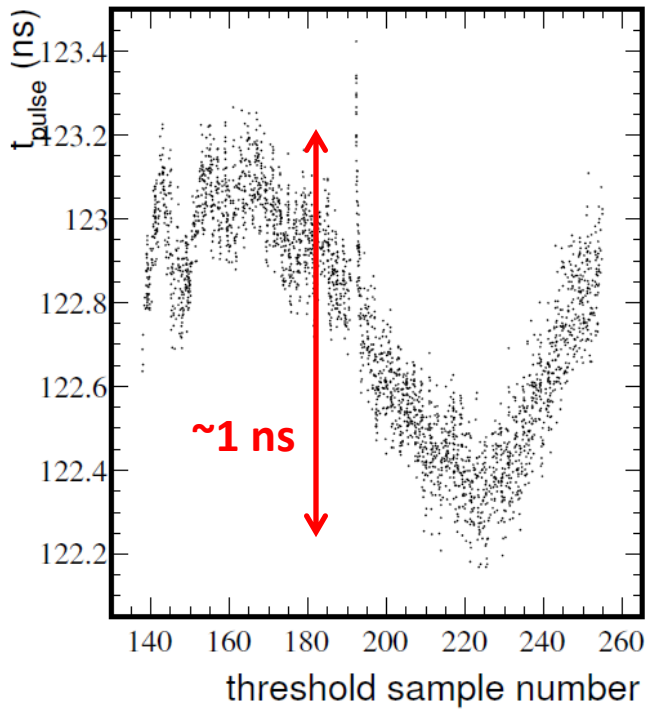
Toy Example



Red – Assumes nominal Δt at each step.

Blue – Uses proper Δt at each step.

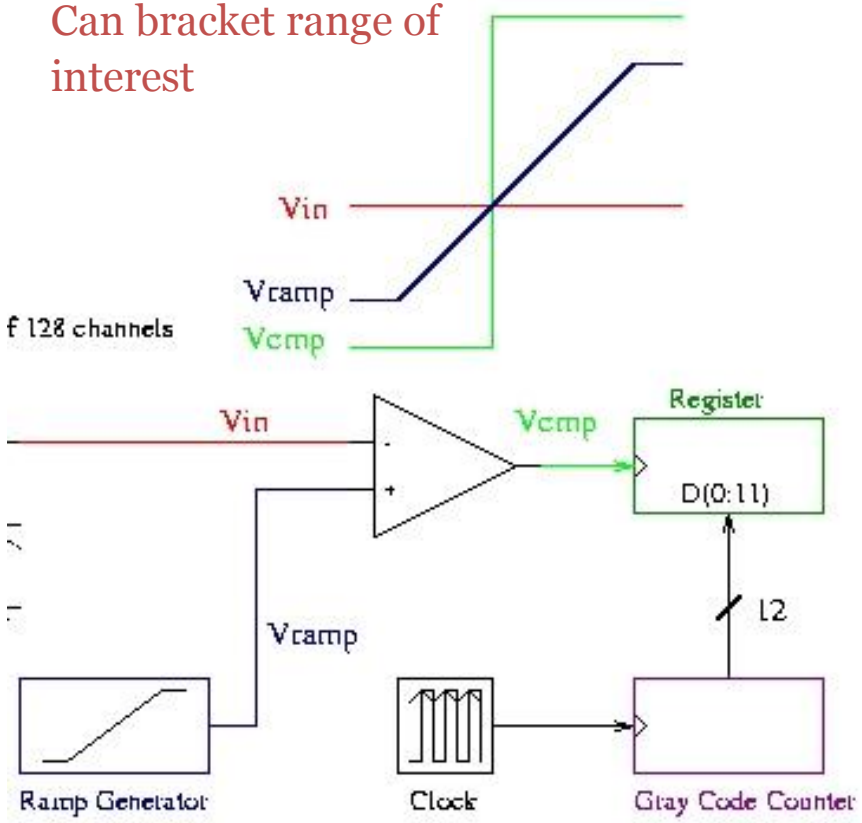
Measured nonlinearity at ~2.7 GSa/s

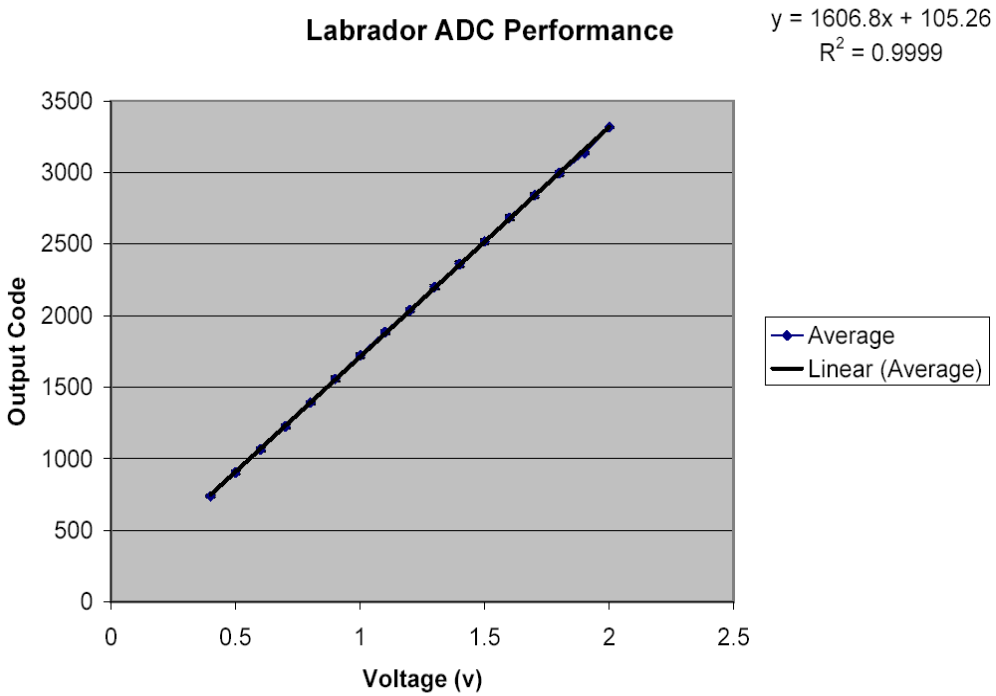


- Calibration of these effects is non-trivial (but a number of procedures are now well known).
- Can complicate waveform processing (e.g., if using FFTs).

Parallel Wilkinson Digitization

- No missing codes
- Linearity as good as can make ramp
- Can bracket range of interest

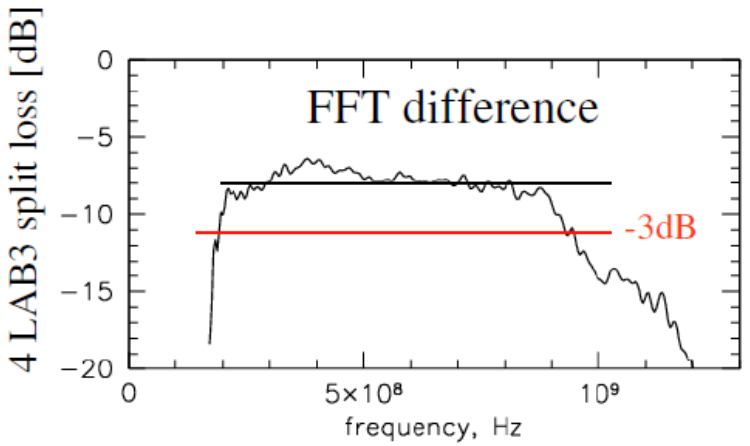


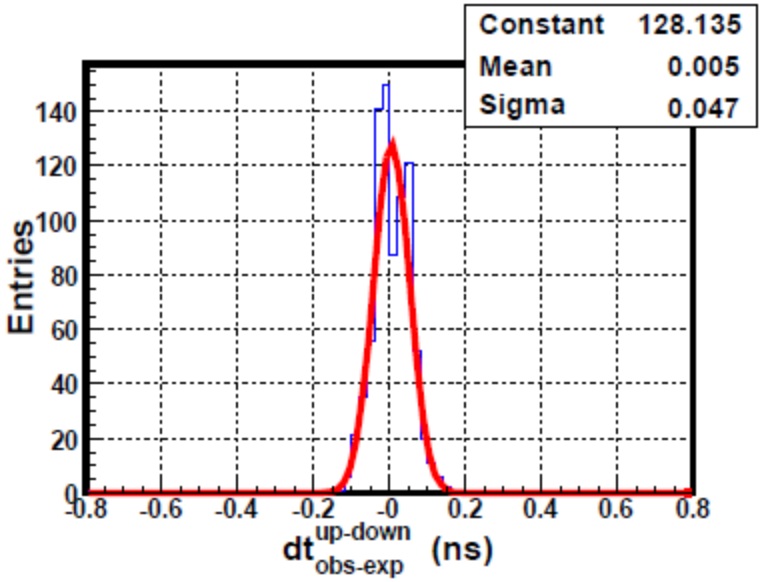


- Excellent linearity.
- Basically as good as can make current source & comparator.
- Comparator ~0.4 – 2.1V; 133MHz GCC max (~31us).

Success and Limitations

- Key enabling technology for two flights of ANITA:
  - Excellent bandwidth: f_{3dB} ~ 0.9 GHz
  - Excellent timing resolution, 10's of ps, allowed sub-degree pointing resolution.
    - But only after intensive calibration of Wilkinson ADCs and timing offsets.
- All done with short buffer depth:
  - 260 samples at 2.6 GSPS ➔ 100 ns





In-flight timing resolution, arXiv: 0812.1920

Success and Limitations

- Key enabling technology for two flights of ANITA:
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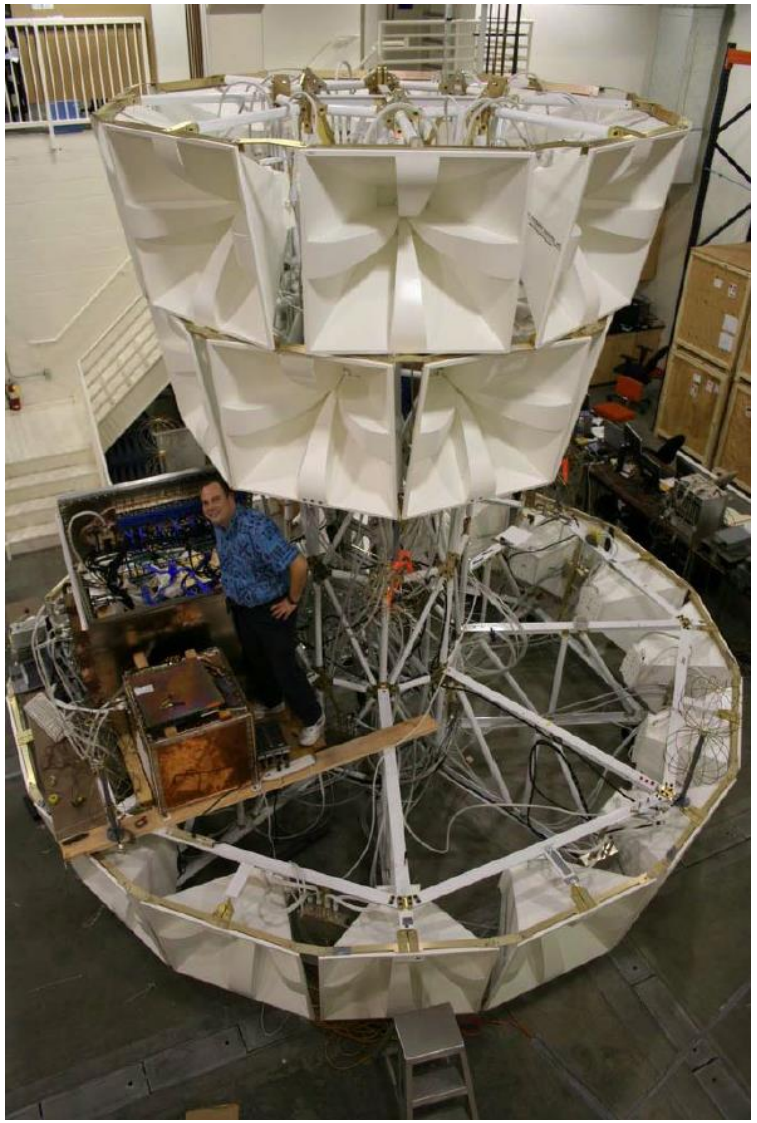
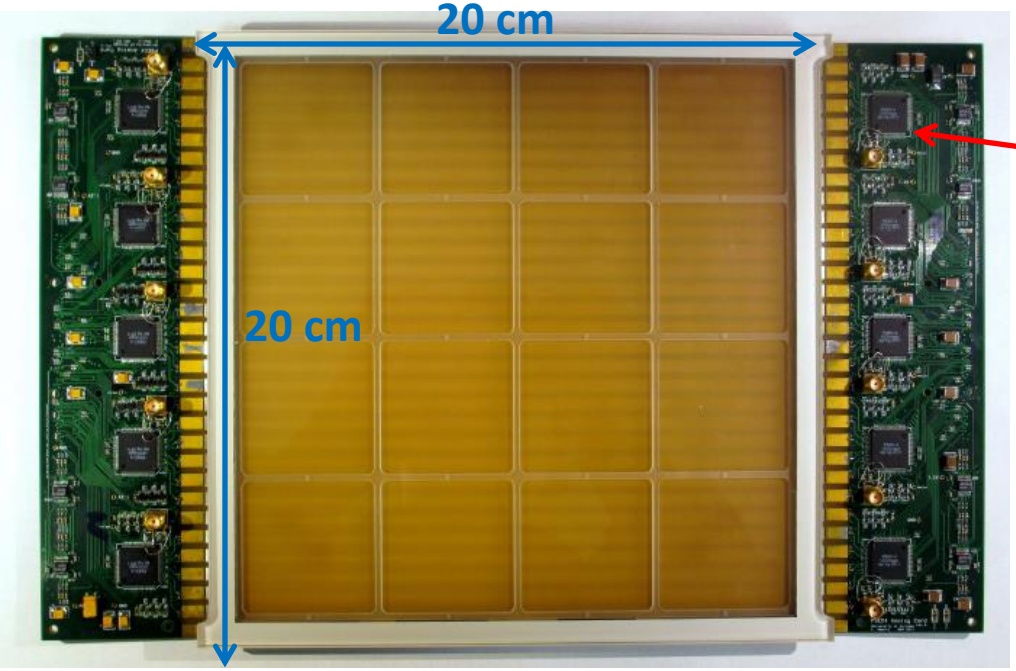
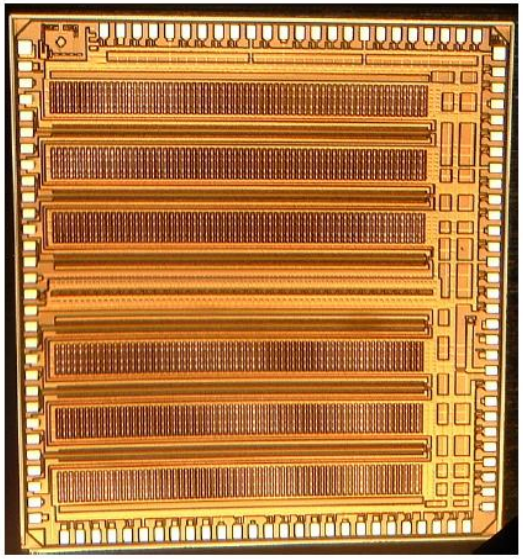
  - Excellent timing resolution, 10's of ps, allowed sub-degree pointing resolution.
    - But only after intensive calibration of Wilkinson ADCs and timing offsets.
- All done with short buffer depth:
  - 260 samples at 2.6 GSPS ➔ 100 ns
  - Compact experiment and impulsive nature of signal made this an acceptable limitation.



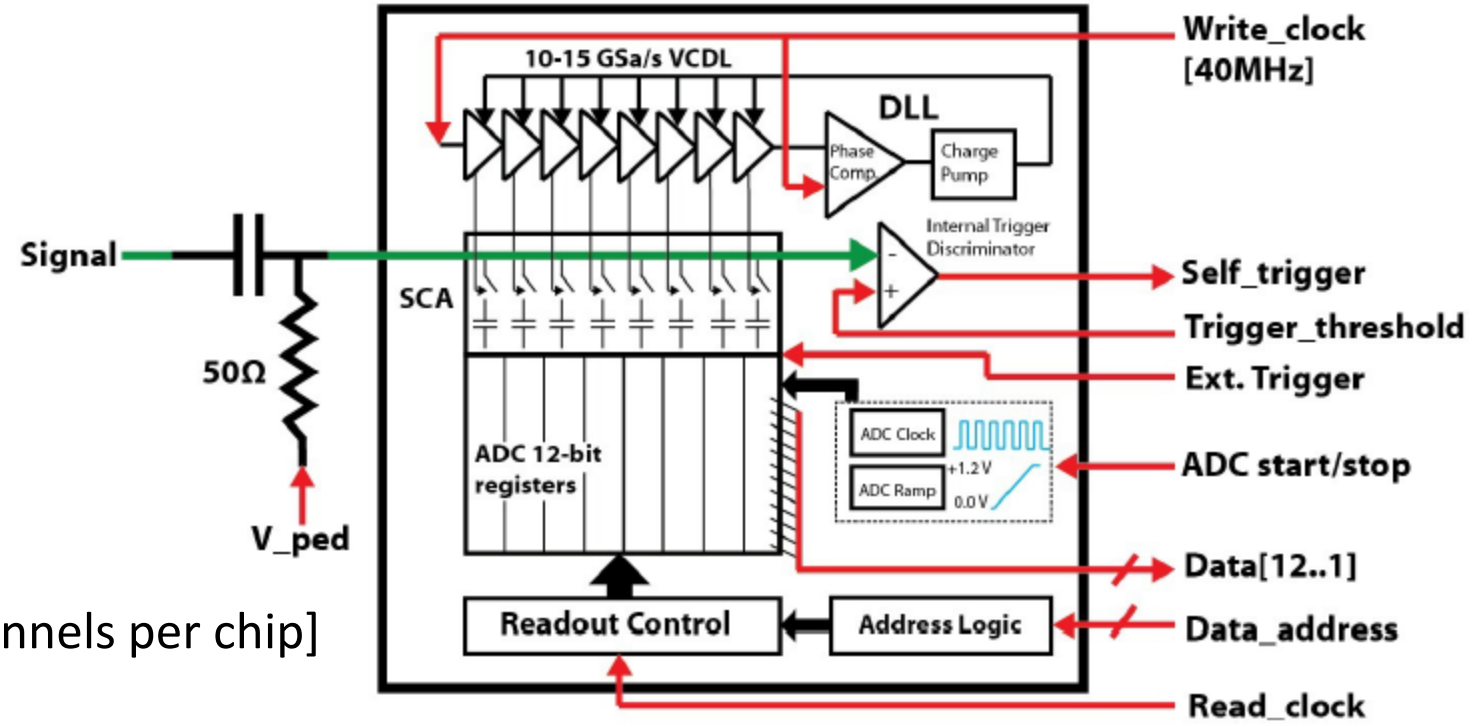
PSEC: Pushing Sampling Rates and ABW





- The PSEC-series of ASICs:
  - Developed at U. Chicago (E. Oberla *et al.*) for readout of LAPPD microchannel plate devices.
    - See talk by Karen Byrum earlier this session.
  - Focus is on fast sampling, high bandwidth.
    - First waveform samplers to be fabricated in IBM 130 nm process.
- Current state-of-the-art: PSEC4

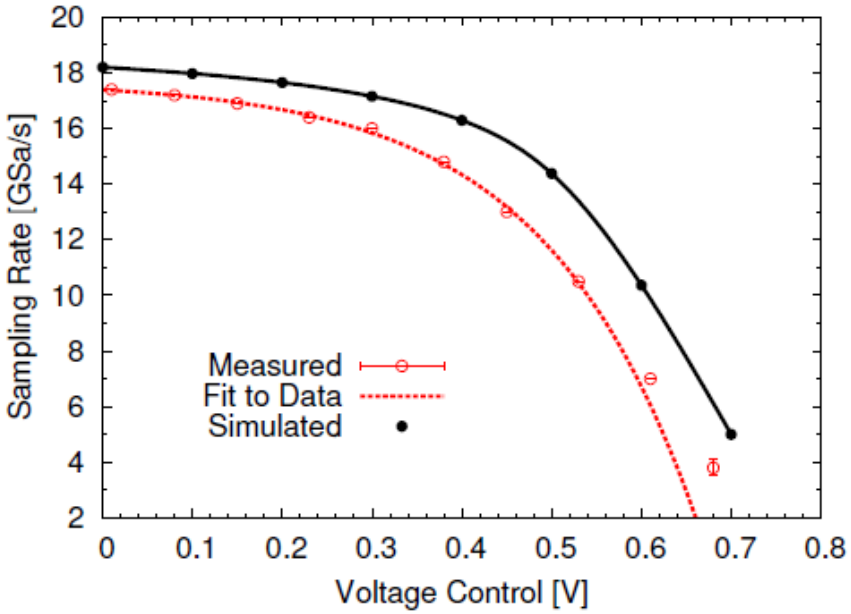
PSEC4 Architecture

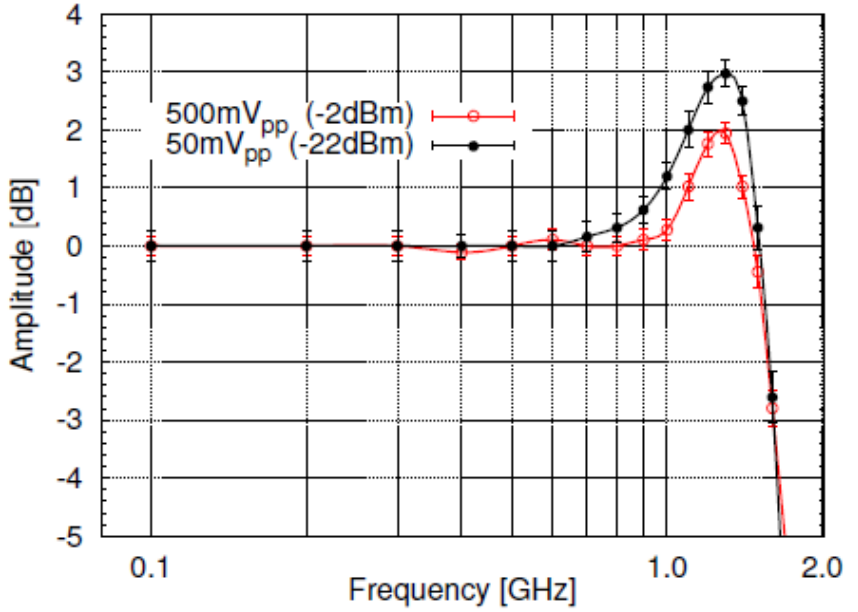


[x6 channels per chip]

- Functionally very similar to LABRADOR3.
  - Delay line sampling strobe generation.
  - Switched capacitor array analog memory.
  - Wilkinson-style ADC.
- Notable differences:
  - Smaller feature size process ➔ faster sampling, higher leakage currents.
  - Delay locked loop stabilizes the sampling rate against temperature drift.

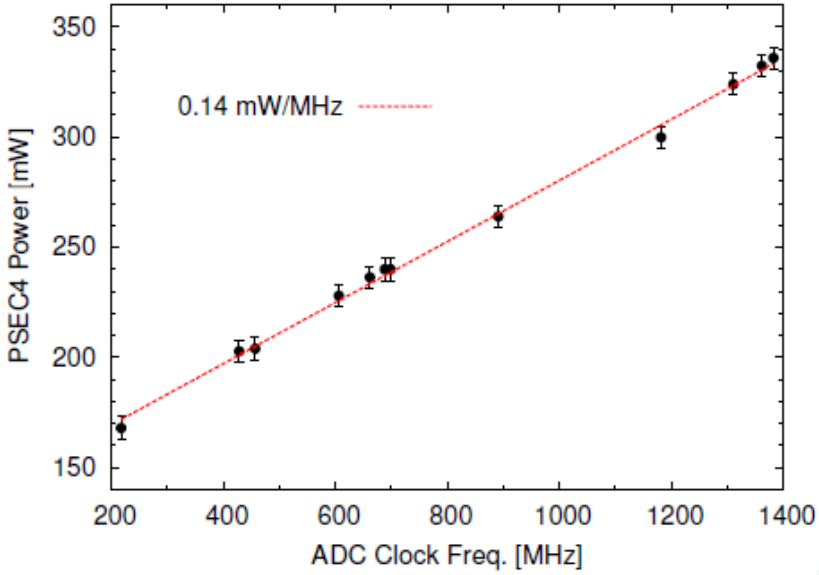
PSEC4 Achievements





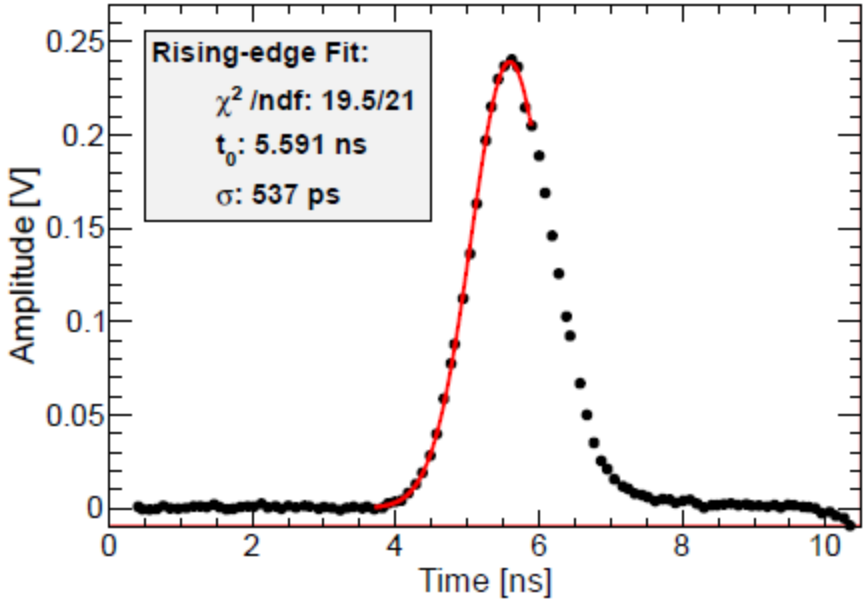
- Sampling rates up to **18 GSPS**!
- Excellent analog bandwidth:

  f_{3dB} = 1.6 GHz.
- Power is a function of digitization speed, but remains manageable:
  - 40 mW / chip quiescent.
  - ~100's of mW / chip while digitizing.

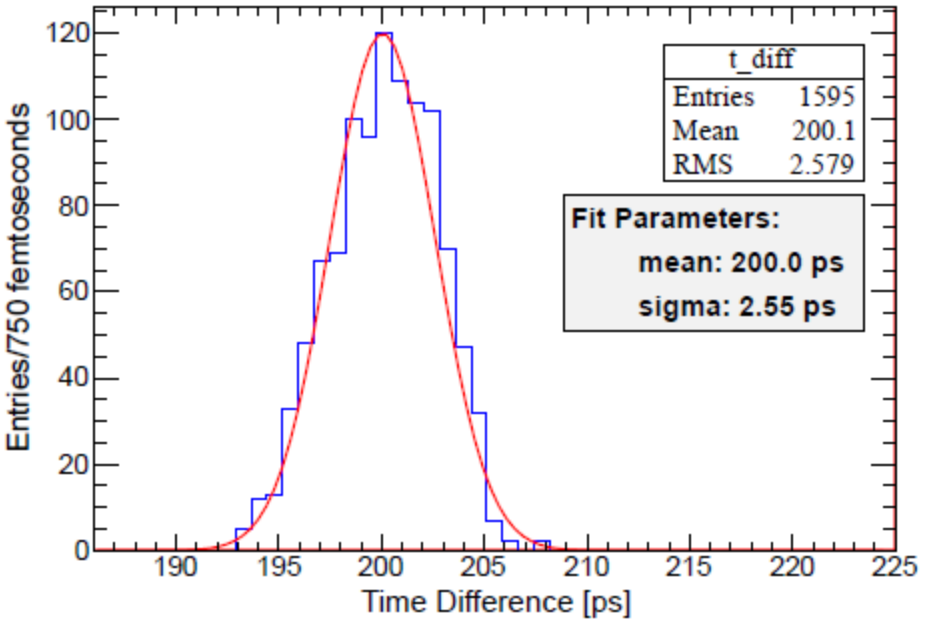


PSEC4: Timing Approaching 1 ps

Example input pulse (1.25 ns FWHM)



Timing resolution between two channels

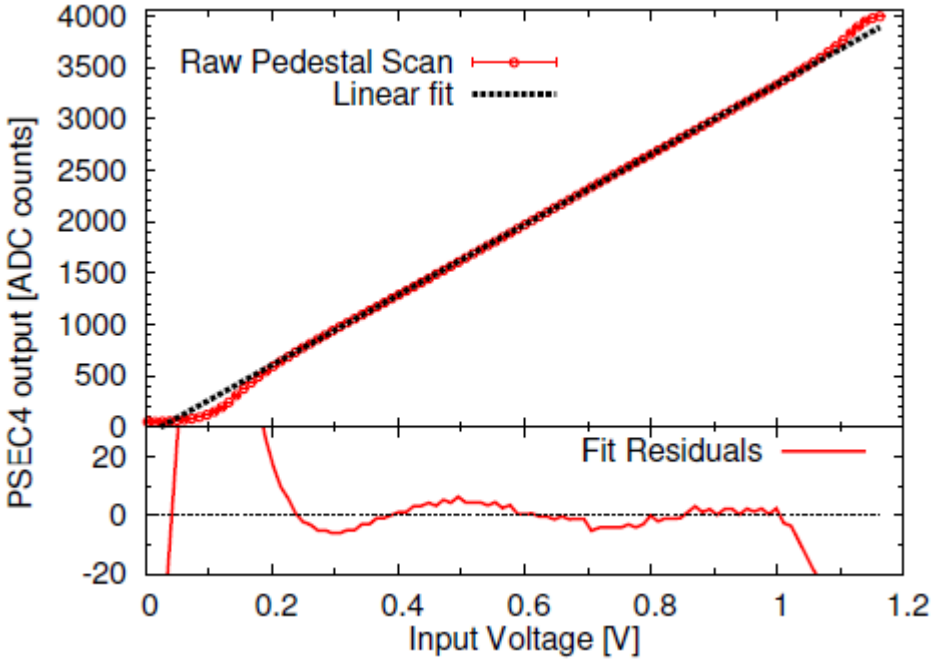


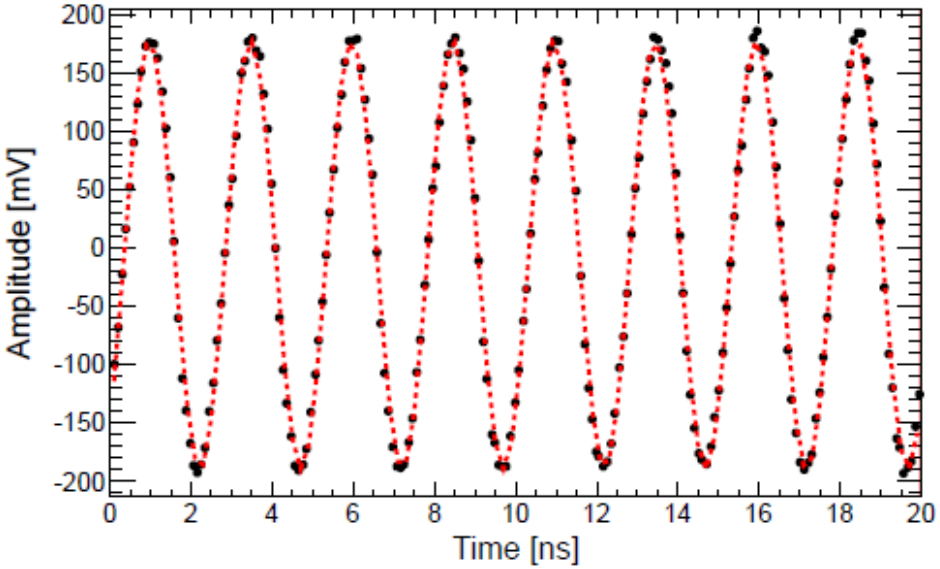
- Oversampling provides many points on leading edge of even fastest expected micro-channel plate signals.
- PSEC4 lives up to its name: provides timing at near ~ps level!

*As in previous discussions, ultimate timing resolution requires significant calibration effort chip-by-chip.

Any Drawbacks?

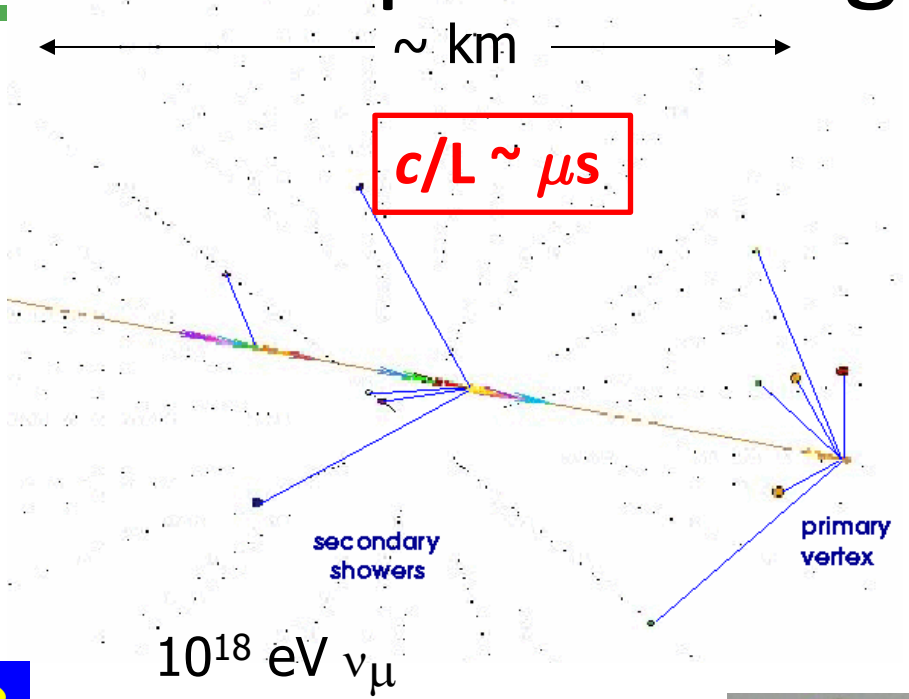
- The 130 nm process has a 1.2 V input rail.
  - This significantly limits dynamic range.
- Each PSEC4 channel consists of 256 sample cells.
  - At 10 GSPS, that gives a ~25 ns buffer.
  - At 18 GSPS, < 15 ns buffer.
- Large leakage currents in the 130 nm process cause signal degradation for long analog storage times (e.g., 10's of mV lost in ~10 μs).



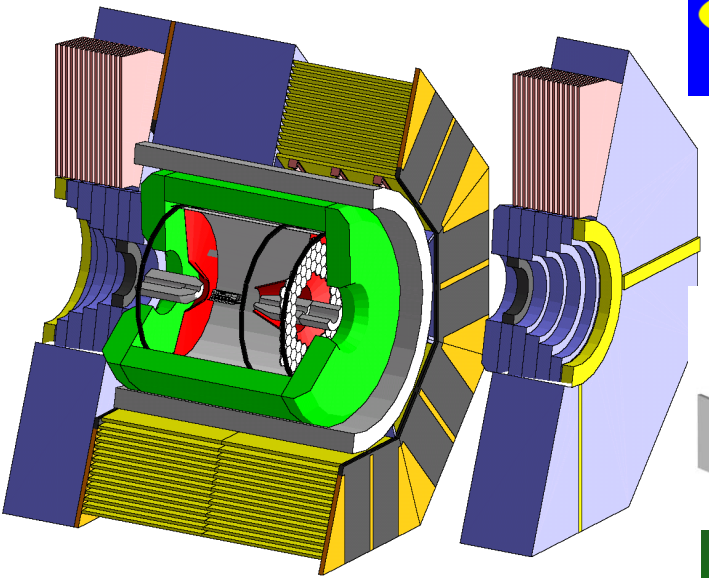


Still, the PSEC series has been very successful. Many others are adopting smaller features sizes for future ASICs.

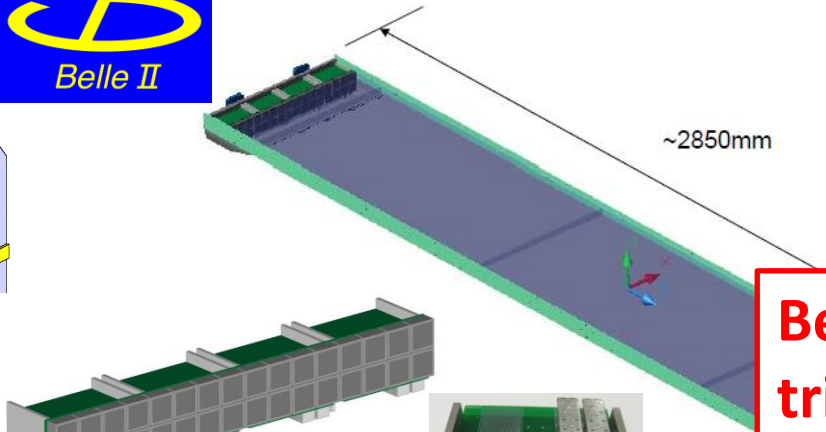
A Different Direction: Deep Buffering

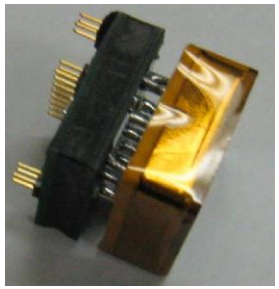


10^{18} eV ν_μ



Belle II

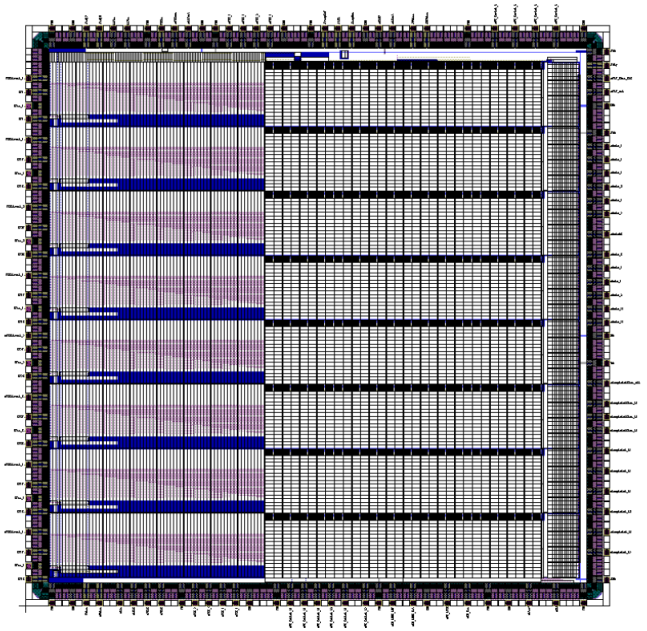


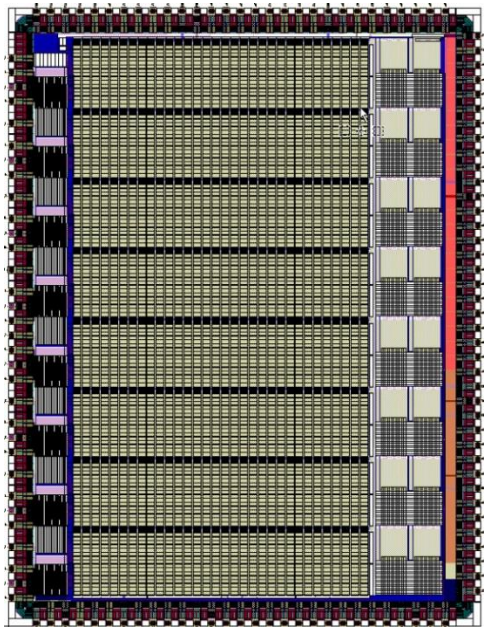


Belle II Max L1 trigger latency ~5 μs

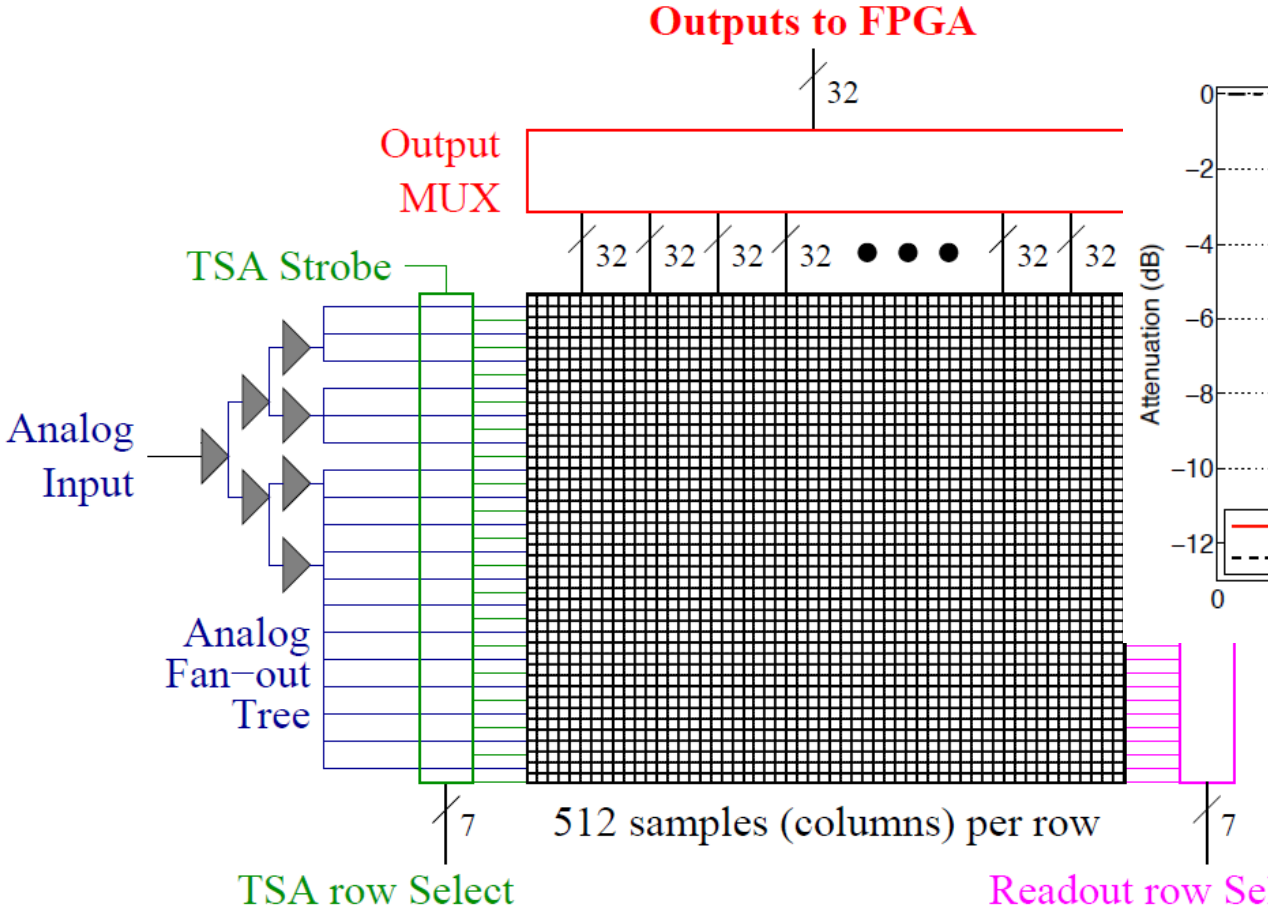
Multi-Stage Sampling (e.g., IRS, TARGET)

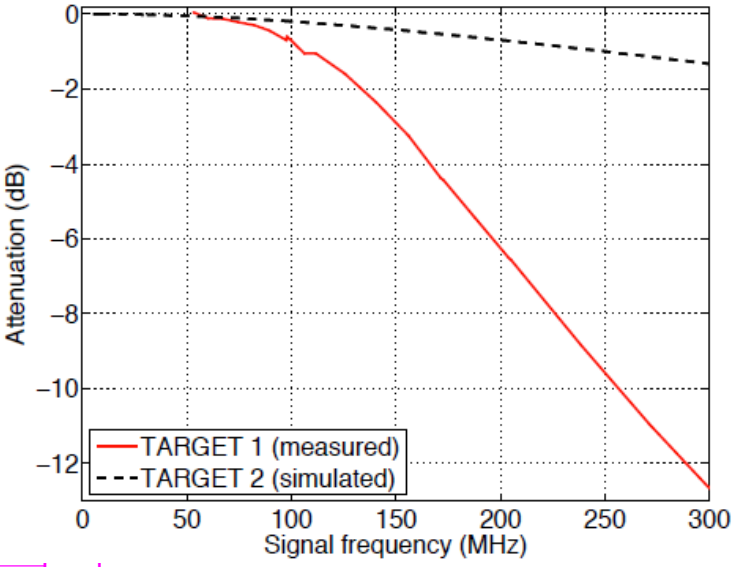
- ASIC series with deep buffers in 0.25 μm:
  - Ice-radio sampler (IRS)
    - Originally developed for Askaryan Radio Array.
    - Same ASIC line will be used for Belle II PID system (MCP-PMT readout).
  - TeV Array Readout GSPS Electronics with Trigger (TARGET)
    - Under development for Cherenkov Telescope Array.
    - Same ASIC line will also be used for Belle II muon system.





Deeper Buffering with Fanouts

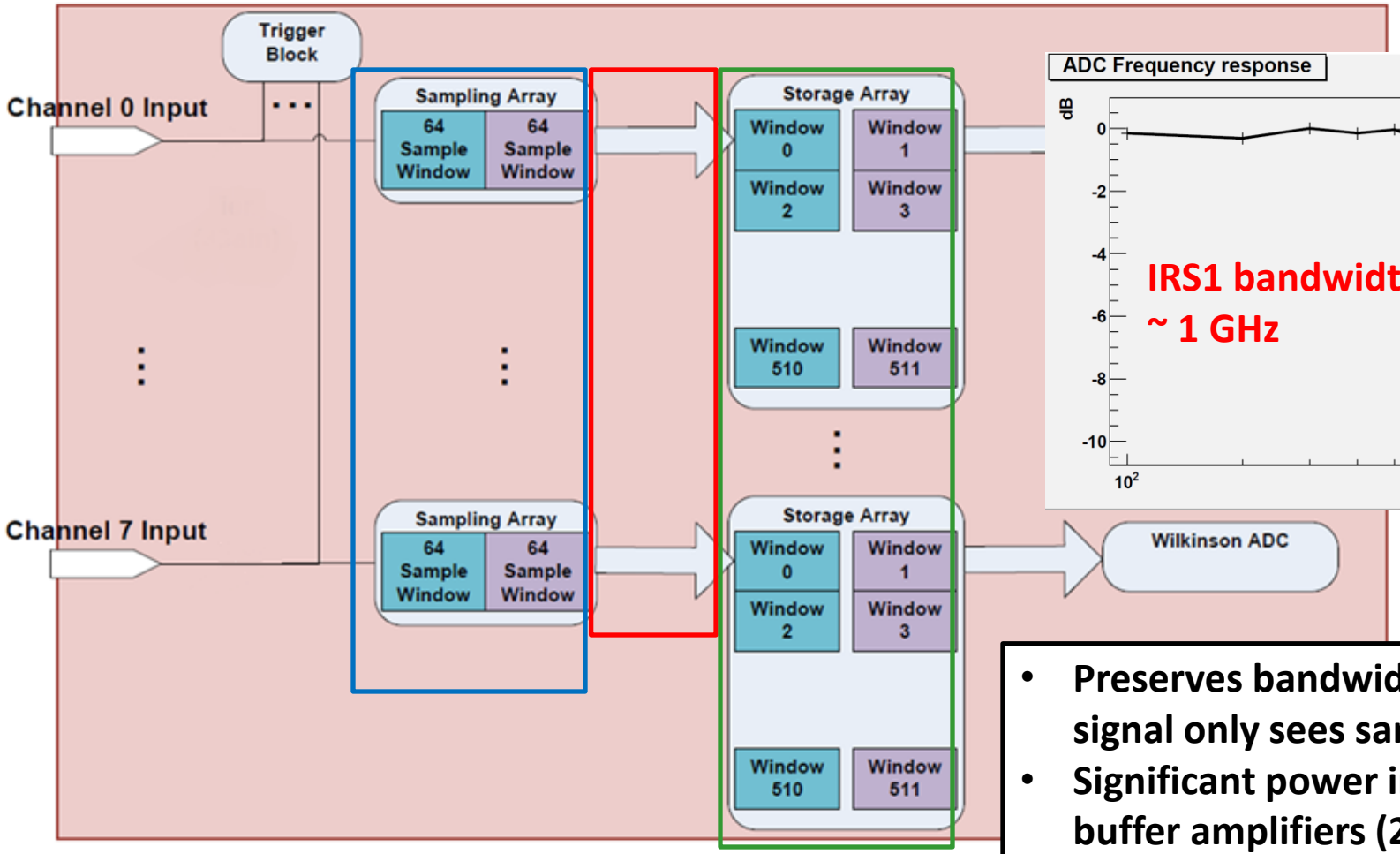




Example TARGET1 bandwidth measurement
arXiv:1105.1832

- Input signals are fanned out to multiple sampling arrays. Arrays are enabled one at a time to provide deeper buffering.
- Tradeoff: chain of input buffers has negative effects on bandwidth.

Deeper Buffering with Multi-Stage Transfer

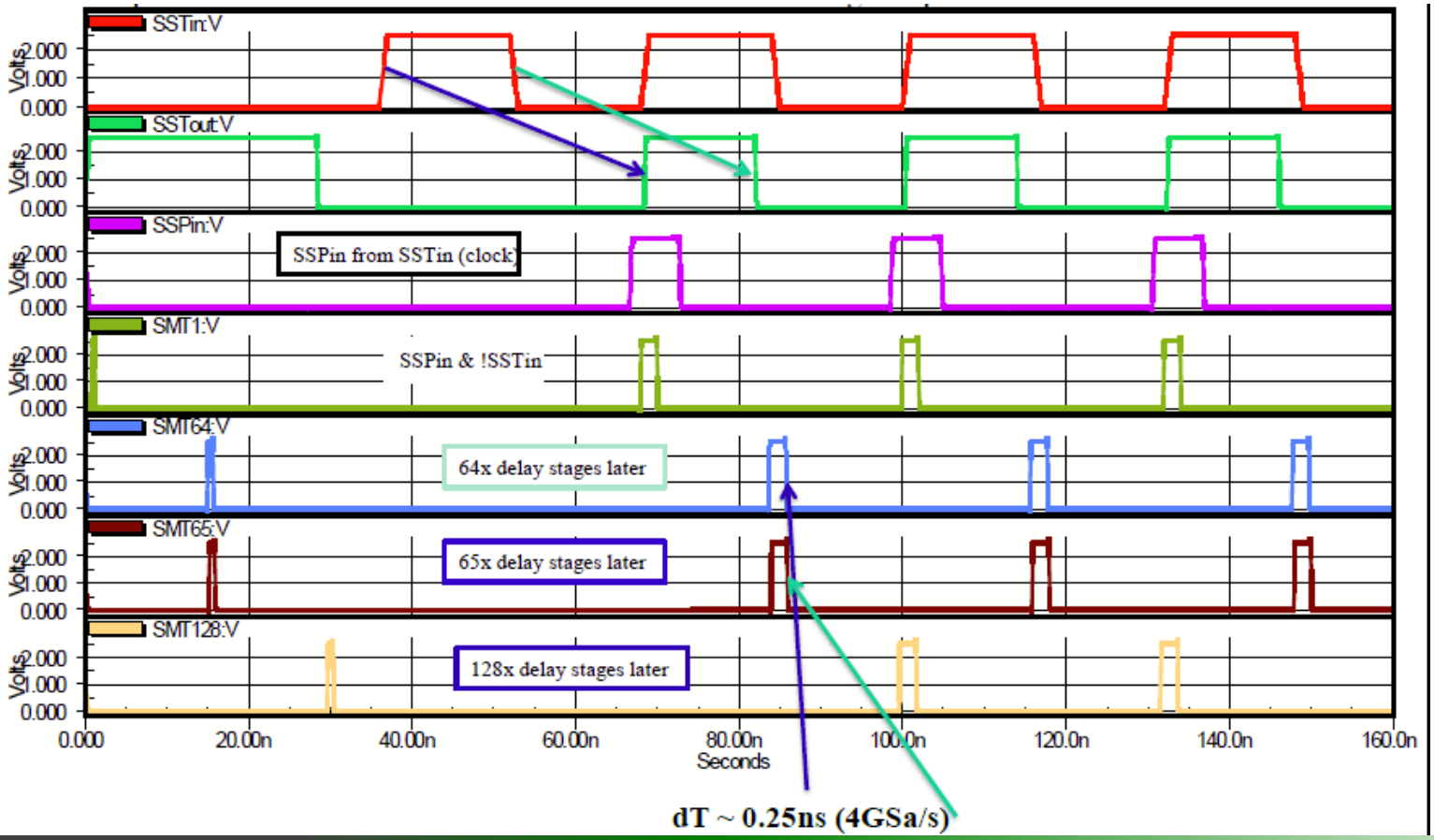


- **Preserves bandwidth (input signal only sees sampling array).**
- **Significant power increase to run buffer amplifiers (256k of them for IRS2/3, TARGET5 ASICs).**

- Multi-stage transfer:
  - Small **sampling array(s)**. While they're not sampling, transfer stored voltages to **storage cells** via **buffer amplifiers**.

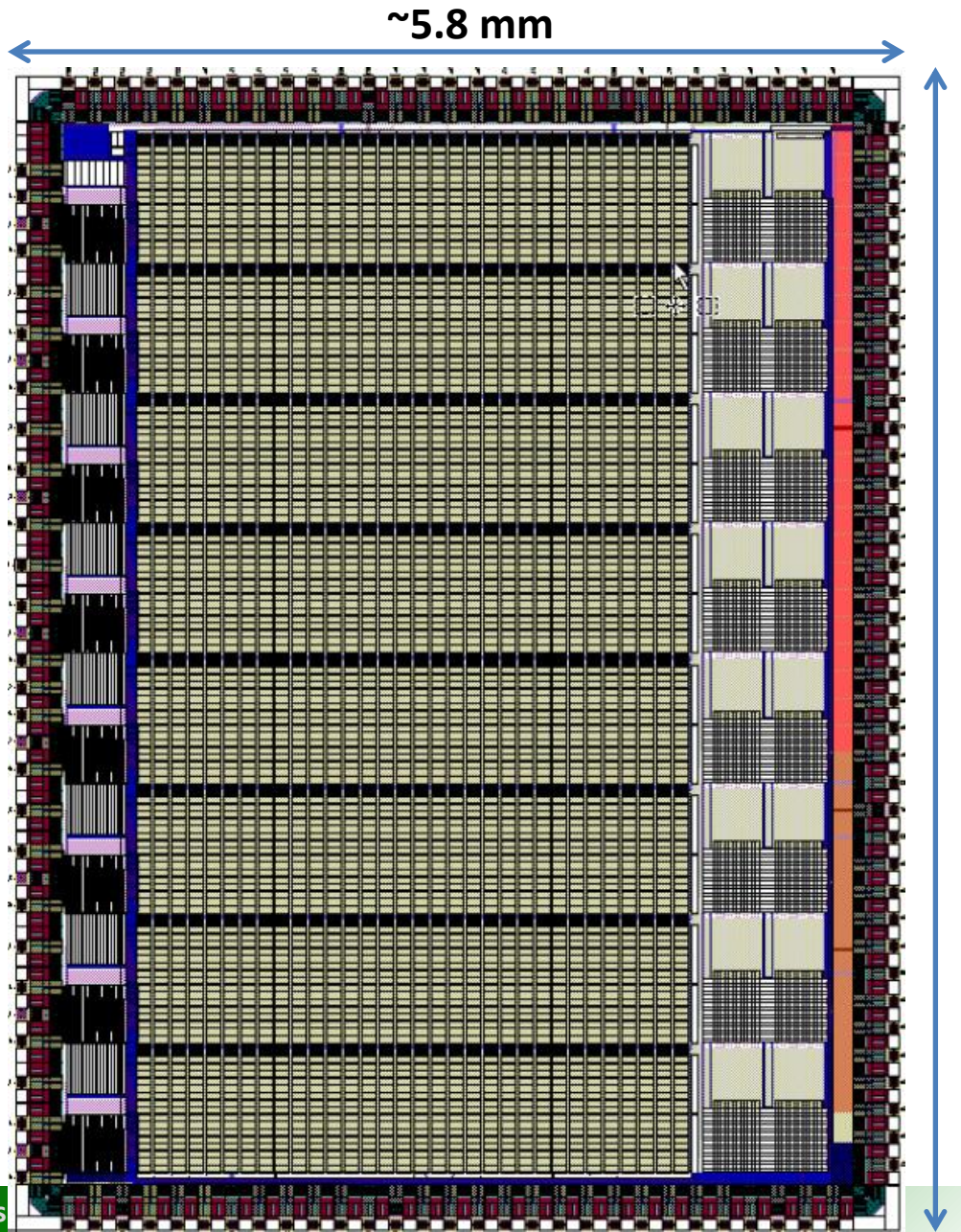
Control of Multi-Stage Sampling

- Large number of precisely-timed control signals are required to keep this working smoothly…
  - Can be handled on companion FPGA (IRS2, TARGET5).
  - Or absorbed into the ASIC (IRS3B).

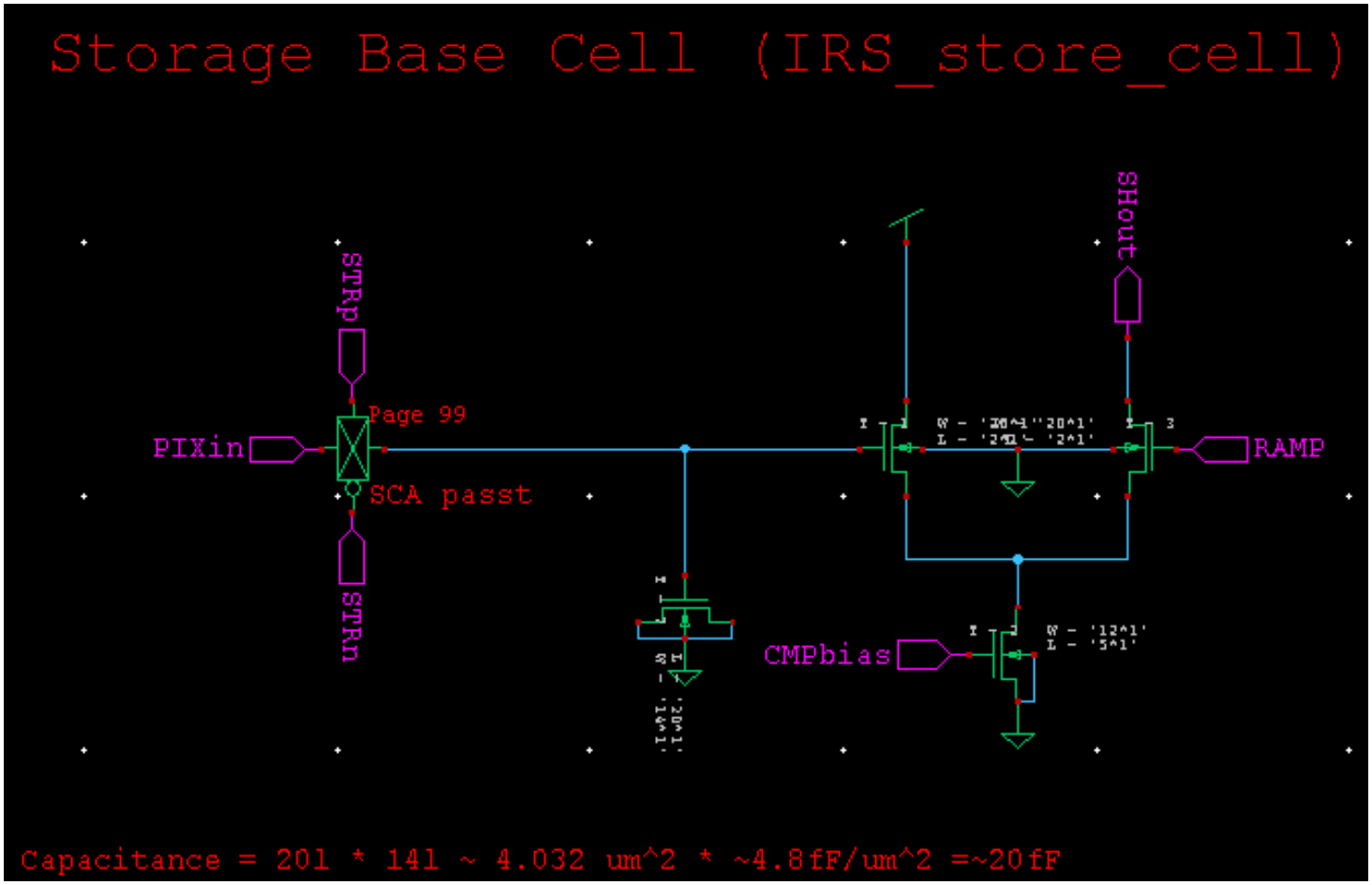


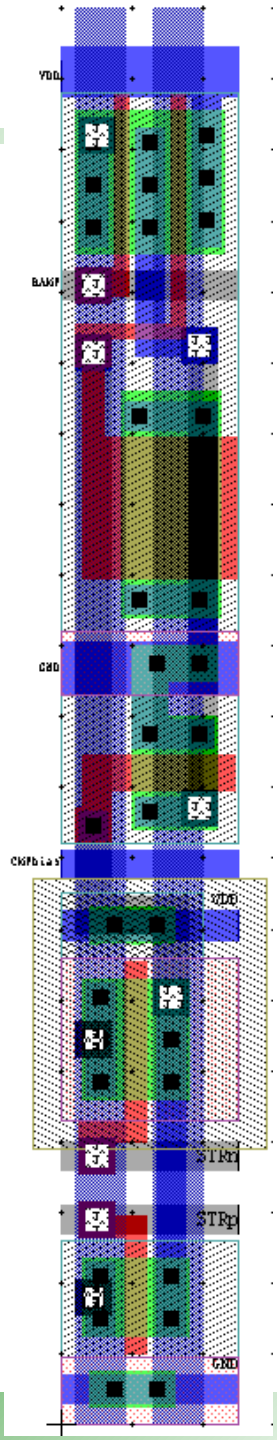
Need Compact Storage Cells!

- TARGET5 has ~256k analog storage cells!
  - 16k storage cells for each of 16 channels.
  - Dominates die size.
  - In order to accommodate, storage cells (with integrated comparators for digitization) must be very small…



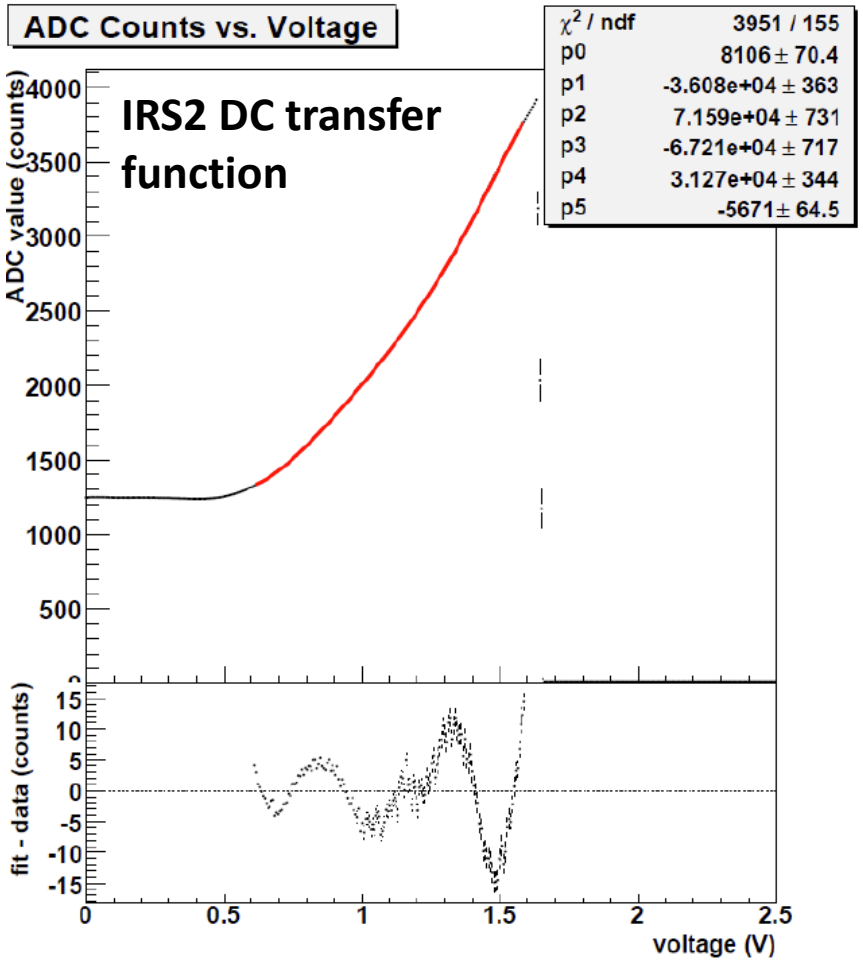
Compact Storage Cells

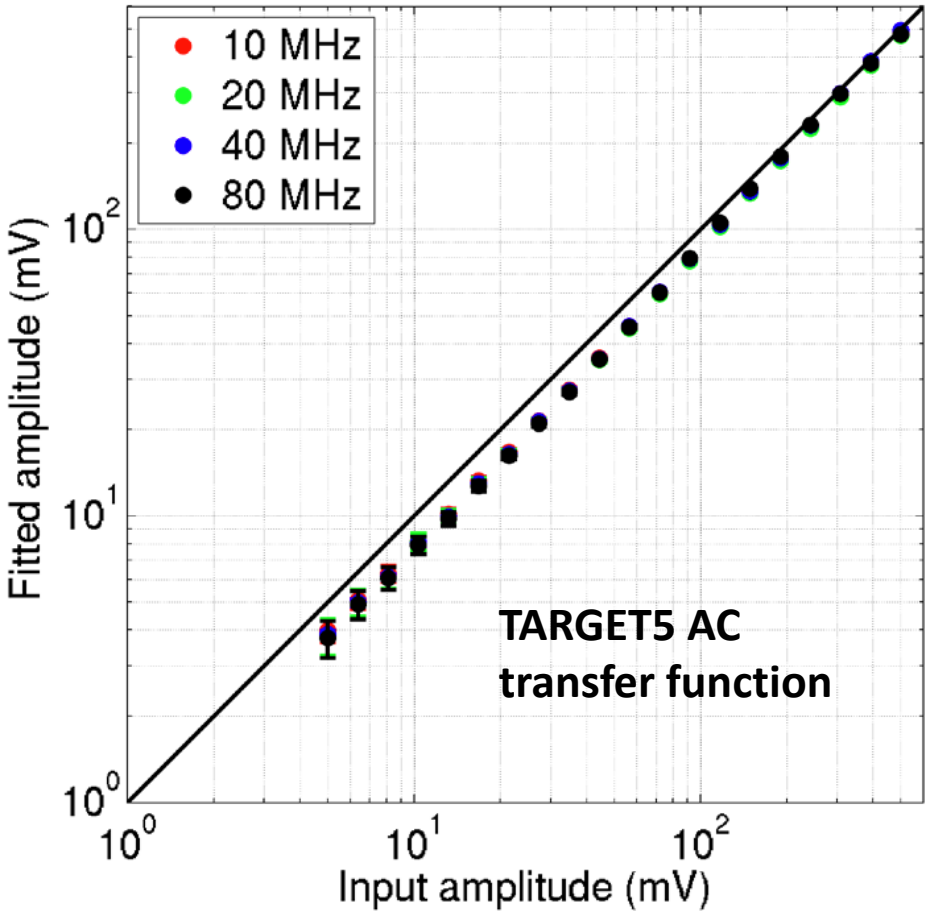




- Differential pair as comparator
  - Density ~ 25k storage cells/mm^2 (0.25um)

Compact Storage Cell Transfer Functions

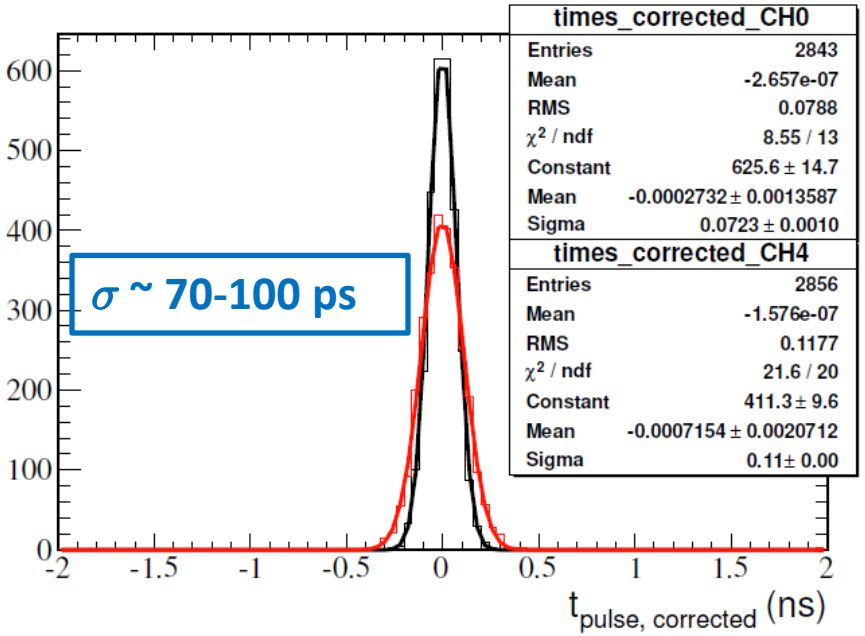




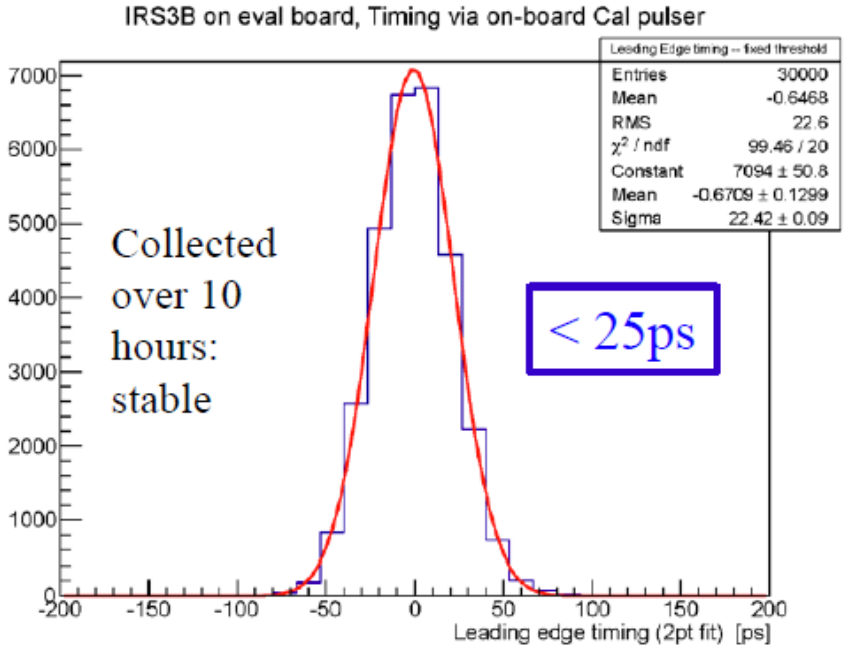
Lower dynamic range, more nonlinearity, increased calibration requirements:

- Each of the 256k storage cells has a different “pedestal” value.
- In principle , transfer function of each cell can vary as well.

Precision Timing Can Still Be Realized



IRS2 pulse time resolution



IRS3B pulse time resolution

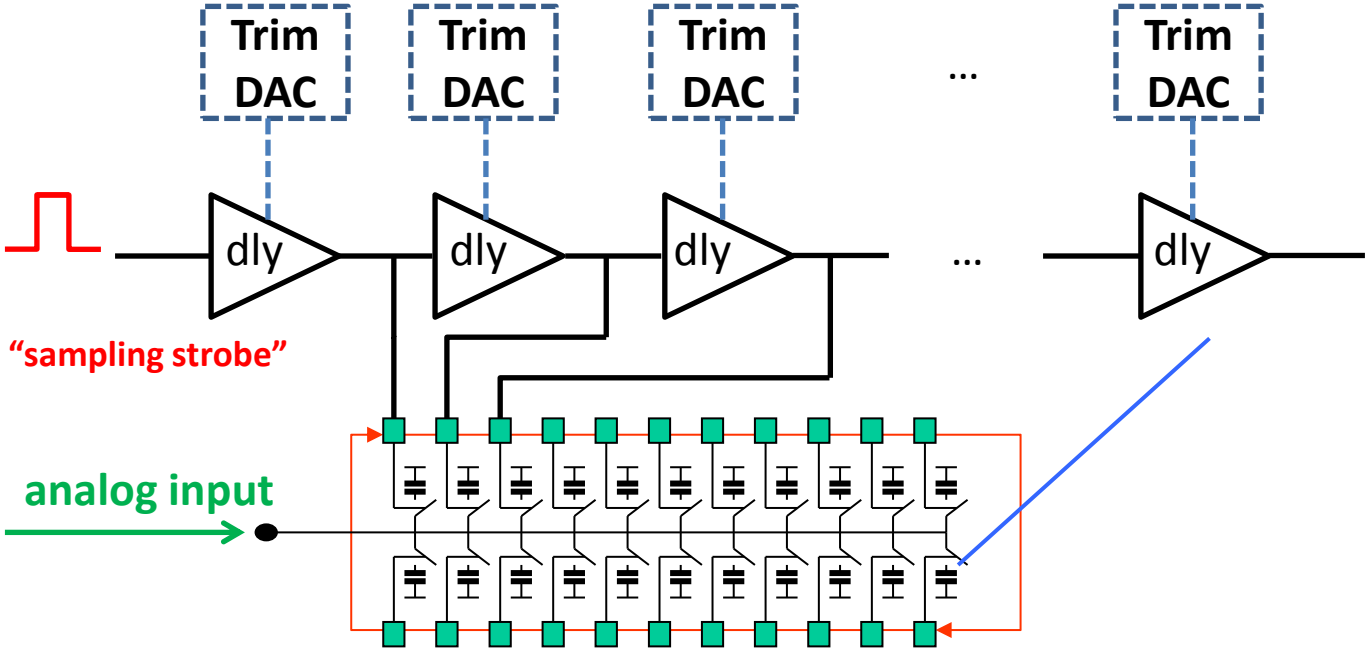
- Nonlinearities of ADC do not spoil timing resolution.
- Many experiments can operate with limited charge / pulse height resolution.
  - Pulse height used only for rejection of noise / cross-talk.

Review of Deep Buffering Tradeoffs

- Deep buffering can be achieved, but at some cost.
  - Increased power consumption and/or analog bandwidth.
  - Reduced digitizer performance due to limited space to implement comparators (e.g., nonlinearity, increased noise).
- Control complexity grows:
  - This must be handled by companion FPGA, or absorbed into the ASIC itself.
- Calibration complexity grows.
- But the potential payoff is huge…
  - Effectively deadtimeless readout for given trigger rate and occupancy.

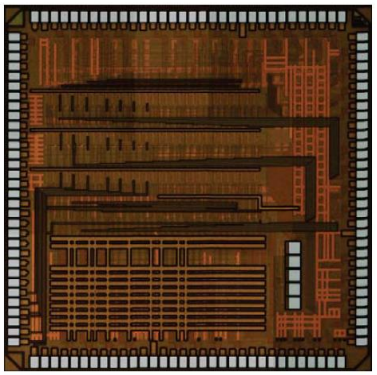
Other Features Under Development

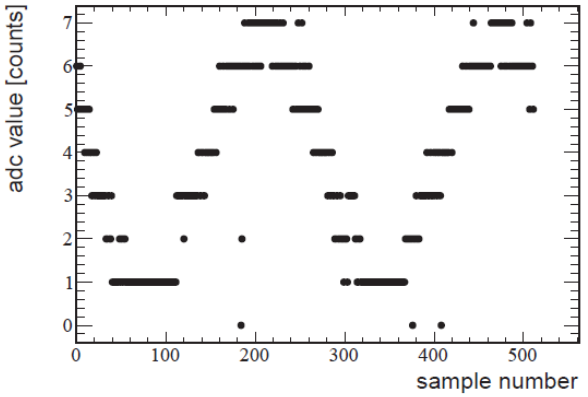
- LAB4B – removing uneven sampling with on-chip trim DACs



- RITC – streaming output at low resolution (3 bits @ 3 GSPS)

IBM 130 nm. Developed for ANITA-III trigger system, serves as a pre-digitizer for identifying coherent signals

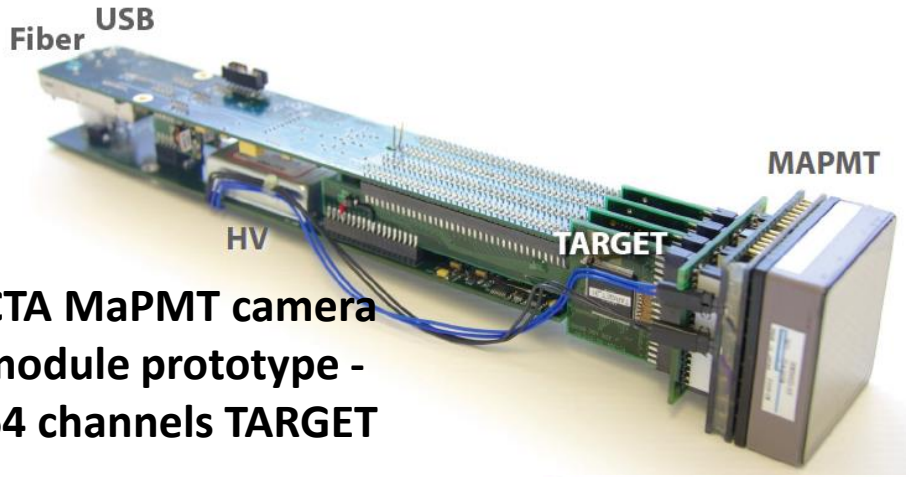




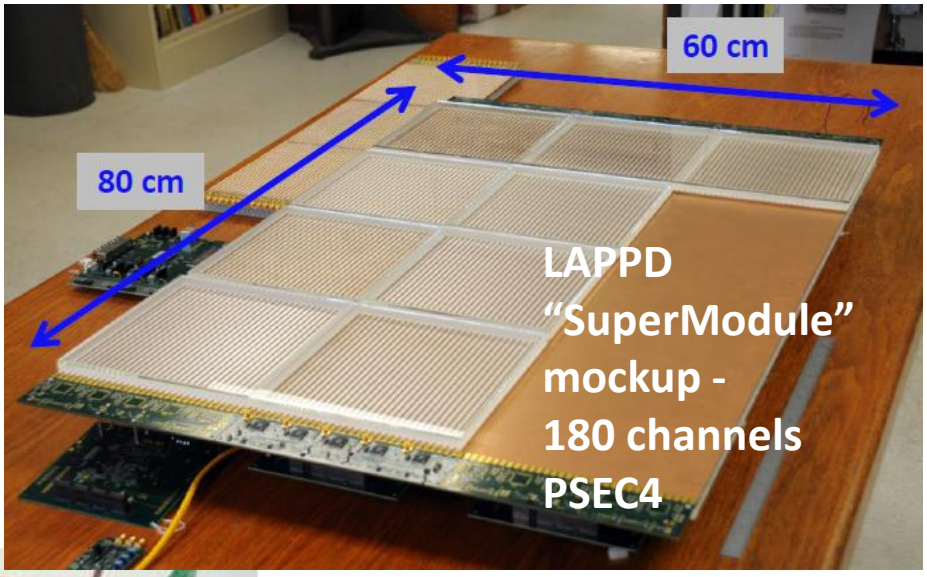
Is waveform sampling for you?

- Custom waveform sampling ASICs have significant potential benefits:
  - Very fast sampling, > 10 GSPS.
  - Excellent analog bandwidth, > 1 GHz.
  - High channel density.
  - Low power, 10's of mW sampling, 100's of mW while digitizing.
  - Excellent timing resolution, toward σ ~ 1 ps.
- They also have some limitations.
  - But various limitations can be traded off against other features.
  - Until now focus has been more on timing than on charge measurements.
  - Small but active community is exploring parameter space.
- Conventional & flash ADCs may be better suited to some applications…
- …but these ASICs are continuously improving!

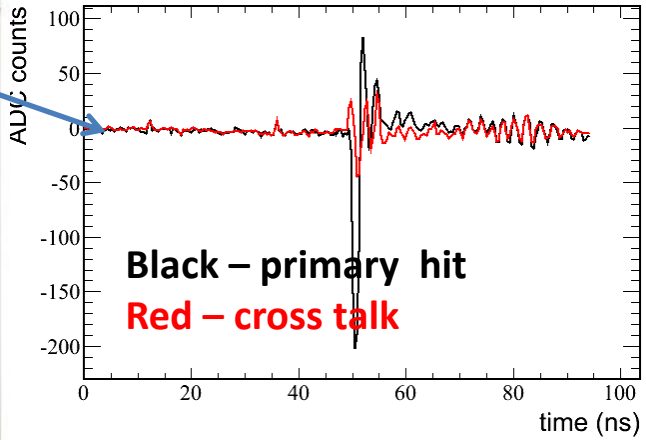
Custom ASICs for Future Experiments



CTA MaPMT camera module prototype - 64 channels TARGET



- This technology is already enabling **compact**, **highly integrated**, **precision timing** readouts.



- **Stay tuned! More ASICs coming soon? TARGET7, LAB4B, PSEC5, DRS5, SAMPIC**

Thanks for your attention!

ASIC	Amplification?	# chan	Depth/chan	Sampling [GSa/s]	Vendor	Size [nm]	Ext ADC?
DRS4	no.	8	1024	1-5	IBM	250	yes.
SAM	no.	2	1024	1-3	AMS	350	yes.
IRS2	no.	8	32536	1-4	TSMC	250	no.
BLAB3A	yes.	8	32536	1-4	TSMC	250	no.
TARGET	no.	16	4192	1-2.5	TSMC	250	no.
TARGET2	yes.	16	16384	1-2.5	TSMC	250	no.
TARGET3	no.	16	16384	1-2.5	TSMC	250	no.
PSEC3	no.	4	256	1-16	IBM	130	no.
PSEC4	no.	6	256	1-16	IBM	130	no.