Updates on DAT board

S.Gao on behalf of BNL CE Team

12/19/2023

Cold Electronics in need

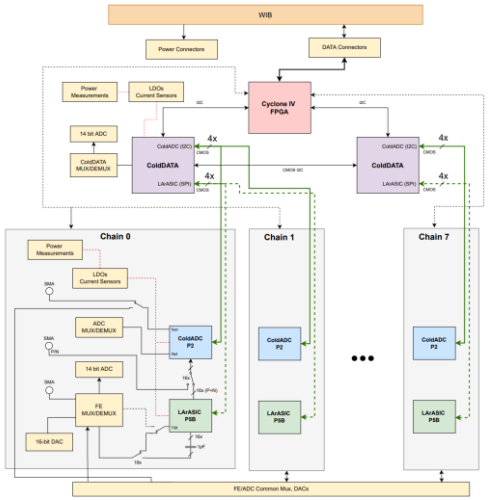
	FD1	FD2
anode unit	150 APA	80 CRP
Electrodes (charge readout)	384,000	245,760
LArASIC	**24,000**	**15,360**
ColdADC	**24,000**	**15,360**
COLDATA	**6,000**	**3,840**
FEMB Assembly *	3,000	1,920
Cold cable bundles	150	80
Feed-through	75	40
CE flanges	150	80
WIEC crate	150	80
WIB	750	480
PTC	150	80
PTB	150	80

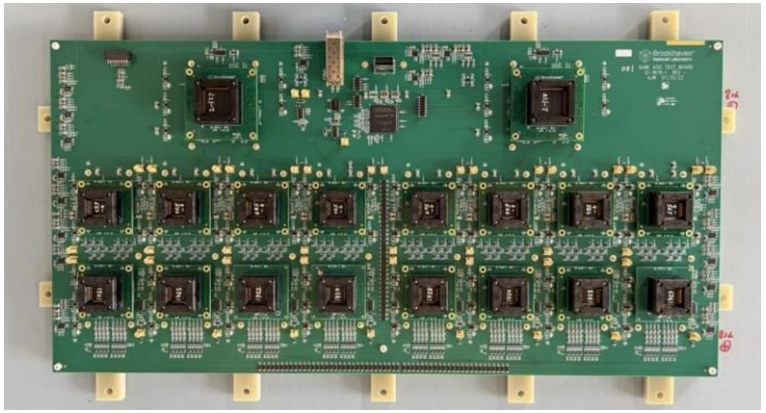
*: require at least 10% spares

DUNE Production has started after FD1 PRR approval in May 2023

Hardware: DUNE ASIC Test Board (DAT)

- DUNE ASIC Test (DAT) Board
  - Unified ASIC test board for LArASIC, ColdADC and COLDATA QC
    - Compatible power and data interface with WIB. It acts as exactly as a FEMB to WIB
    - Can perform QC testing for 8x LArASIC, 8x ColdADC and 2x COLDATA at both RT and LN2 with MSU new RTS
    - Aim for DUNE-FD1 & FD2 ASIC QC carried out in several test sites
  - A single big board solution with ASIC socket mezzanines
    - ASIC socket suffers mechanical degradation through thermal cycling
    - More commercial semiconductor devices have been identified for cryogenic operation
      - Such as Analog MUX: SN74LV4051, Power Monitoring Chip: INA226, I2C Bridge device: PCA9306, DAC: AD5675ARUZ
  - Unified ASICs and FEMB QC with the same software suite
    - Can benefit directly from the WIB and other **analysis software developments**
    - Some extra software effort for ASIC QC can be implemented as a widget to the available software





LArASIC QC Items

Test Item	Description	Reference chips	Chips for QC	DAT doable
Power Consumption	Measure the power consumption on the three rails of LArASIC (VDDP, VDDA, VDDO), for each of six configurations (two baseline references: 200 mV and 900 mV; three configurations of the output buffer: bypassed, single ended, differential)	Required	Required	Yes
Power Cycling	a number (>5) power on/off cycles, measure the pulse response with a certain configuration (e.g., 14mV/fC, gain, 2.0us peak time, 200mV baseline, 500pA leakage current)	Required	Required	Yes
Register configuration	check through SPI interface for register configuration W/R	Required	Required	Yes
Bandgap	Measure the bandgap reference voltage	Required	Required	Yes
Temperature sensor	Measure the voltage of embedded temperature sensor	Required	Required	Yes
Channel response monitoring	Check response of each channel through the monitor pin	Required	Required	Yes
Internal DAC measurement	measure INL/DNL of 6-bit DAC (4 ranges for 4 gains)	Required	subset	Yes
baseline measurement through monitoring pin	Measure baseline through the monitoring pin (4 gains x 4 peak times x 2 baselines x 4 leakage currents)	Required	subset	Yes
baseline measurement	Measure baseline with ColdADC (4 gains x 4 peak times x 2 baselines x 4 leakage currents)	Required	subset	Yes
Noise measurement	Measure with ColdADC (4 gains x 4 peak times x 2 baselines x 4 leakage currents). A reference capacitive load of ~150 pF at the inputs.	Required	subset	Yes
Calibration with internal-DAC	Measure with ColdADC (4 gains x 4 peak times x 2 baselines x 4 leakage currents) for gain, linearity, range	Required	subset	Yes
Calibration with external precise source	Measure with ColdADC (4 gains x 4 peak times x 2 baselines x 4 leakage currents) for gain, linearity, range	Required	No	Yes
Crosstalk [1]	Measure with ColdADC (1 gains x 4 peak times)	No	No	no
Internal calibration capacitor measurement	Measure the capacitance of the calibration capacitor	Required	No	Yes

[1] crosstalk test should be done on FEMB only

Implemented LArASIC QC Test Items on DAT

```
(base) PS D:\Github\BNL_CE_WIB_SW_QC_main> python .\DAT_LArASIC_QC_quick_ana.py
Analyze all test items? (Y/N) : n
  QC task list
 0: Initilization checkout
 1: FE power consumption measurement
 2: FE response measurement checkout
 3: FE monitoring measurement
 4: FE power cycling measurement
 5: FE noise measurement
 61: FE calibration measurement (ASIC-DAC)
 62: FE calibration measurement (DAT-DAC)
 63: FE calibration measurement (Direct-Input)
 7: FE delay run
 8: FE cali-cap measurement
Please input a number (0, 1, 2, 3, 4, 5, 61, 62, 63, 8) for one test item: _
```

```
~/dune_ce/ce_ana/test nitish@nitish
(ce_venv) ❯ ll ../data/FE_001000001_001000002_001000003_001000004_00100
total 707M
-rw-rw-r-- 1 nitish  41M Nov  6 13:38 QC_CALI_ASICDAC.bin
-rw-rw-r-- 1 nitish 151M Nov  6 13:38 QC_CALI_DATDAC.bin
-rw-rw-r-- 1 nitish  51M Nov  6 13:38 QC_CALI_DIRECT.bin
-rw-rw-r-- 1 nitish 161M Nov  6 13:38 QC_Cap_Meas.bin
-rw-rw-r-- 1 nitish 8.6M Nov  6 13:38 QC_CHKRES.bin
-rw-rw-r-- 1 nitish  81M Nov  6 13:38 QC_DLY_RUN.bin
-rw-rw-r-- 1 nitish 1.1M Nov  6 13:38 QC_INIT_CHK.bin
-rw-rw-r-- 1 nitish  15K Nov  6 13:38 QC_MON.bin
-rw-rw-r-- 1 nitish 3.1M Nov  6 13:38 QC_PWR.bin
-rw-rw-r-- 1 nitish 4.1M Nov  6 13:38 QC_PWR_CYCLE.bin
-rw-rw-r-- 1 nitish 211M Nov  6 13:38 QC_RMS.bin
```

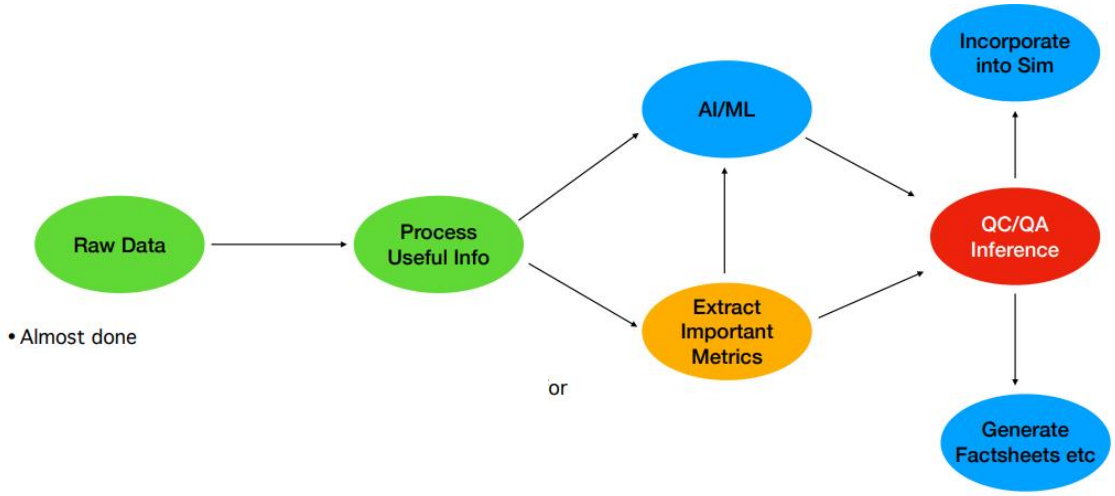
- 8 FE chips are tested simultaneously
  - It takes ~15 minutes to complete a full test
    - FE needs 3~5 seconds to work stably after per re-configuration
- QC test items were finalized, and QC test script was complete

AI/ML ASIC QC Analysis

- Some Identified AI/ML Opportunities

- **A work force at BNL has been summoned by Xin Qian**
- All ASIC chips are going to be tested in the warm condition, while 10% of the chips are going to be tested in the cold condition
  - Can we find a relation between the warm and cold AISC performance, so that we can reduce the likelihood of ASIC testing at cold.
  - Successful warm test does not guarantee a successful cold test
- Can we use AI/ML to find a way to predict cold performance based on warm performance?
  - This is to reduce iterations and increase efficiency

- Infer :
  - If various QC tests have passed/acceptable
  - Pole-zero cancellation etc
  - Insights from AI/ML
  - Store as flags
- Generate factsheets (database, pdfs if ne



ColdADC QC Items Recommendation

Item	Description	FEMB doable	DAT doable
Power consumption and power cycling	Voltage and current of each power rails should be recorded	No	Yes
I2C Write/Read	Check all default register values	Yes	Yes
Chip reset		Yes	Yes
Reference voltages measurement	VCMI, VCMO, VREFN, VREFN	Yes	Yes
Pulse 16 channels	Either at once or individually automatically. Needs external signal generator to get INL/DNL, ENOB, DC noise	No	Yes for INL/DNL Yes for ENOB [1] Yes for DC noise
Overflow checkout	Needs external signal generator	No	Yes
Coupled with LArASIC	Full-chain test. Needs automatically switch sources (LArASIC or signal generator) for ADC inputs	Yes	Yes
16-bit mode	COLDATA doesn't support 16-bit mode	No	No, 14-bit
Ring oscillator	Measure the frequency	No	Yes
UART	Not used in FEMB design	No	Yes

[1] It is doable with external ultra-low distortion function generator and extra coaxial cable connection

Note: QC test items are determined, and QC test script is being finalized

COLDATA QC Items Recommendation

Item	Description	FEMB doable	DAT doable
Power consumption and power cycling	Voltage and current of each power rails should be recorded	No	Yes
I2C Write/Read	Check all default register values	Yes	Yes
Fast commands	Verify all Fast Commands	Yes	Yes
PLL, 8b10b Encoder, Serializer, & Line Driver		Yes	Yes
Data Capture, Frame Formation, Switchyard		Yes	Yes
General Purpose I/O		Yes	Yes
Master/Slave operation	I2C LVDS, I2C CMOS and ADC I2C addressing	no	Yes
EFUSE	Add EFUSE programming into DAT revision	no	Yes

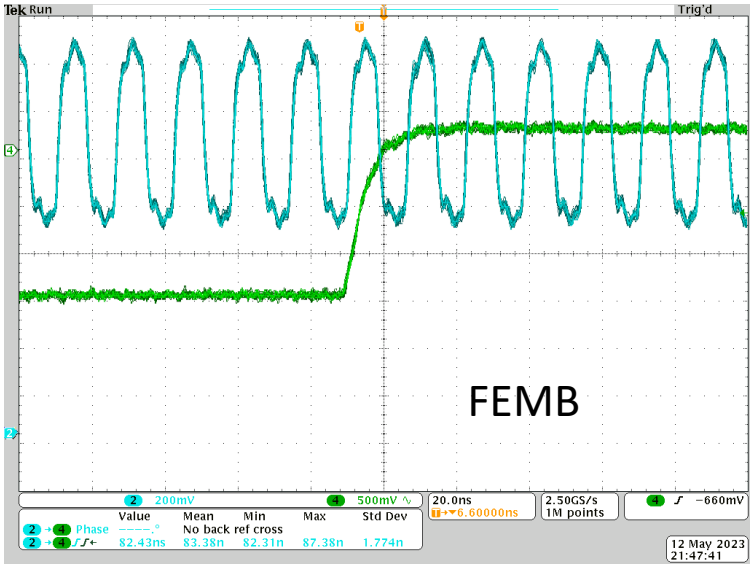
Note: QC test items are determined, and QC test script is being finalized

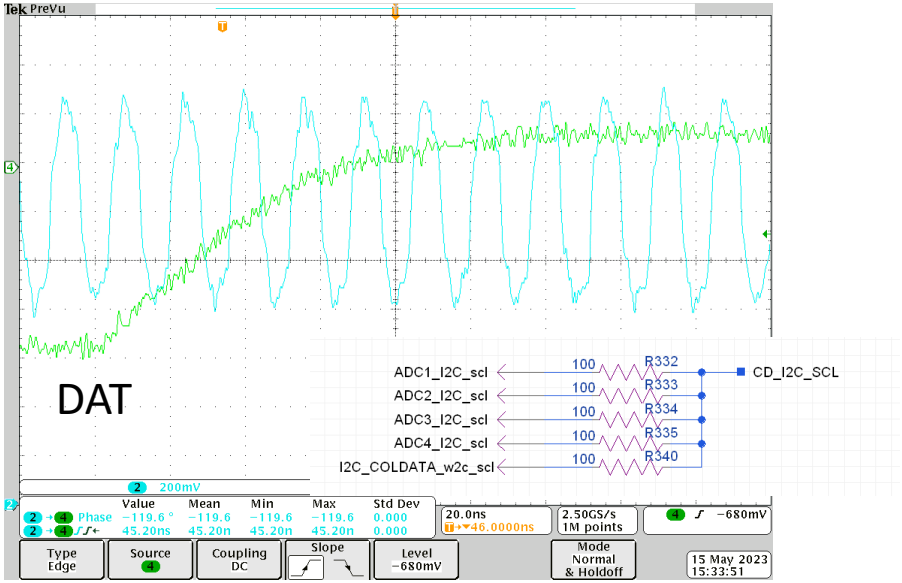
DAT Revision List

- BOM Update
  - Re-assign some resistors and capacitors with correct values
  - Add a 100 Ohm at each regulator output/input/bias to expedite the power cycling
  - Keep SMA footprint but DNI
- Schematics Issues
  - Some FPGA IOs were assigned with conflict
  - Some FPGA DIFF IOs missed external termination resistors
- Add clock fanout buffer for SCL/SDA between COLDATA and ColdADCs
- Connect COLDATA PLL lock signal to FPGA IO
- Remap FE calibration scheme
  - Calibrate one FE channel at a time per board if needed
- Remap ColdADC test scheme
  - Each ColdADC channel can be tested independently
- Add a SE-to-DIFF buffer on DAT for external signal from WIB
- Keep SFP cage inside the board outline
- Add circuit for COLDATA EFUSE programming

Add clock fanout buffer for SCL/SDA between COLDATA and ColdADCs

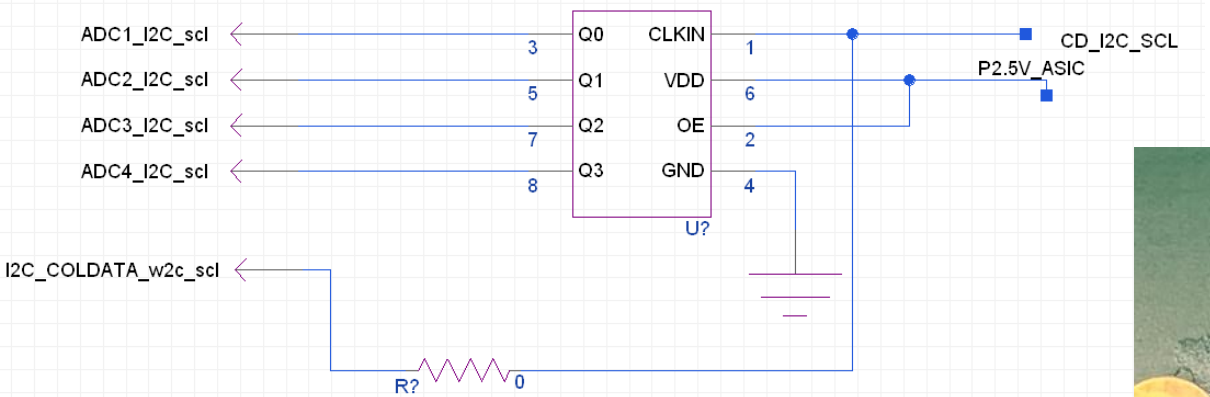
- Previous study indicates that SCL of ColdADC/COLDATA are sensitive to 62.5MHz system clock
  - Rising edge of SCL must be after rising edge of 62.5MHz
- DAT board
  - Each COLDATA SCL needs to drive 4 ColdADC chips and 1 COLDATA chip with long traces and connectors, which makes the load capacitance is large
    - It makes SCL too slow to guarantee the timing relation between SCL and 62.5MHz
    - The fine tuning that Alex implemented on WIB works for FEMB, but not for DAT board which rising and falling edge of SCL is much slower

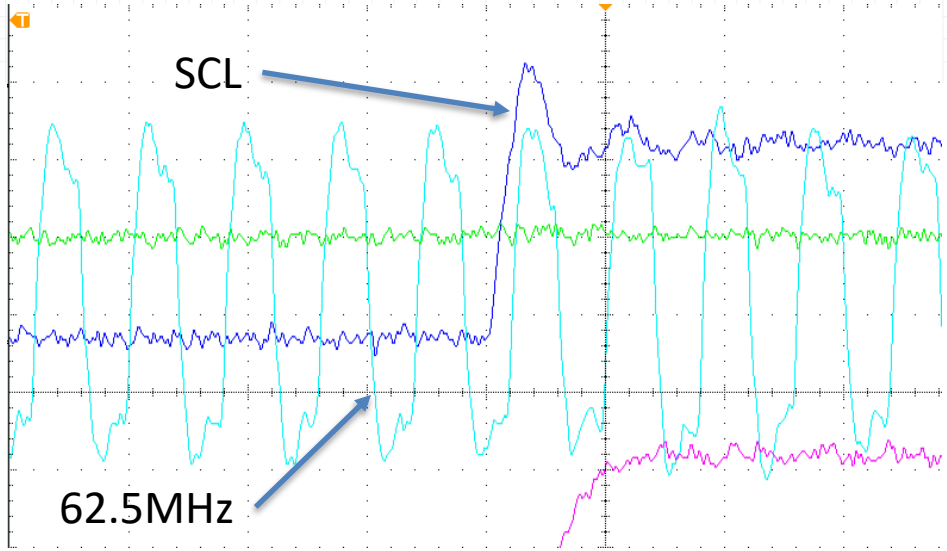




Add a Clock Fanout Buffer on Current DAT

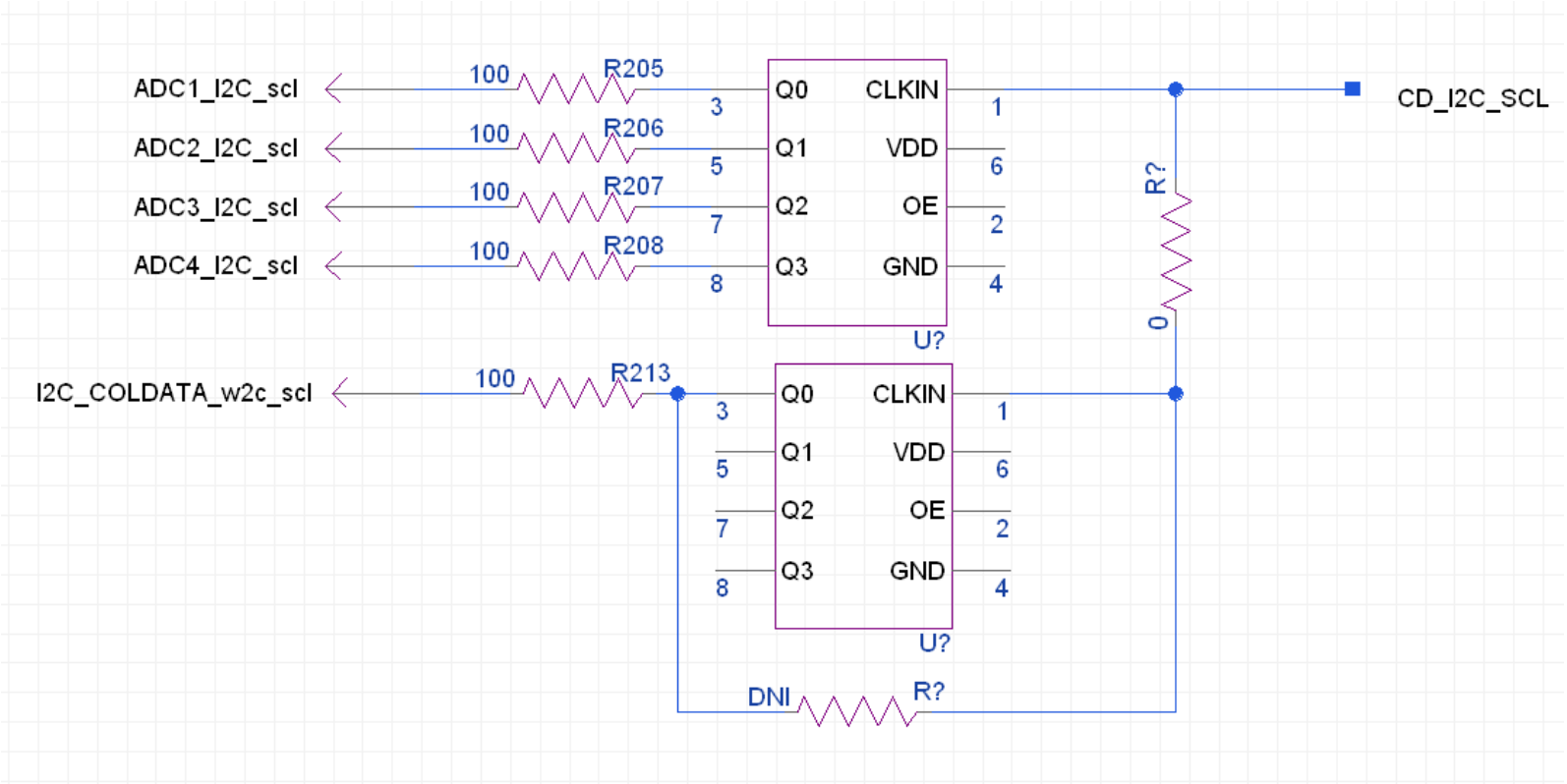
- Fly wires for the current DAT board
- Signals are much faster with clock fanout buffer





Implemented in Revision

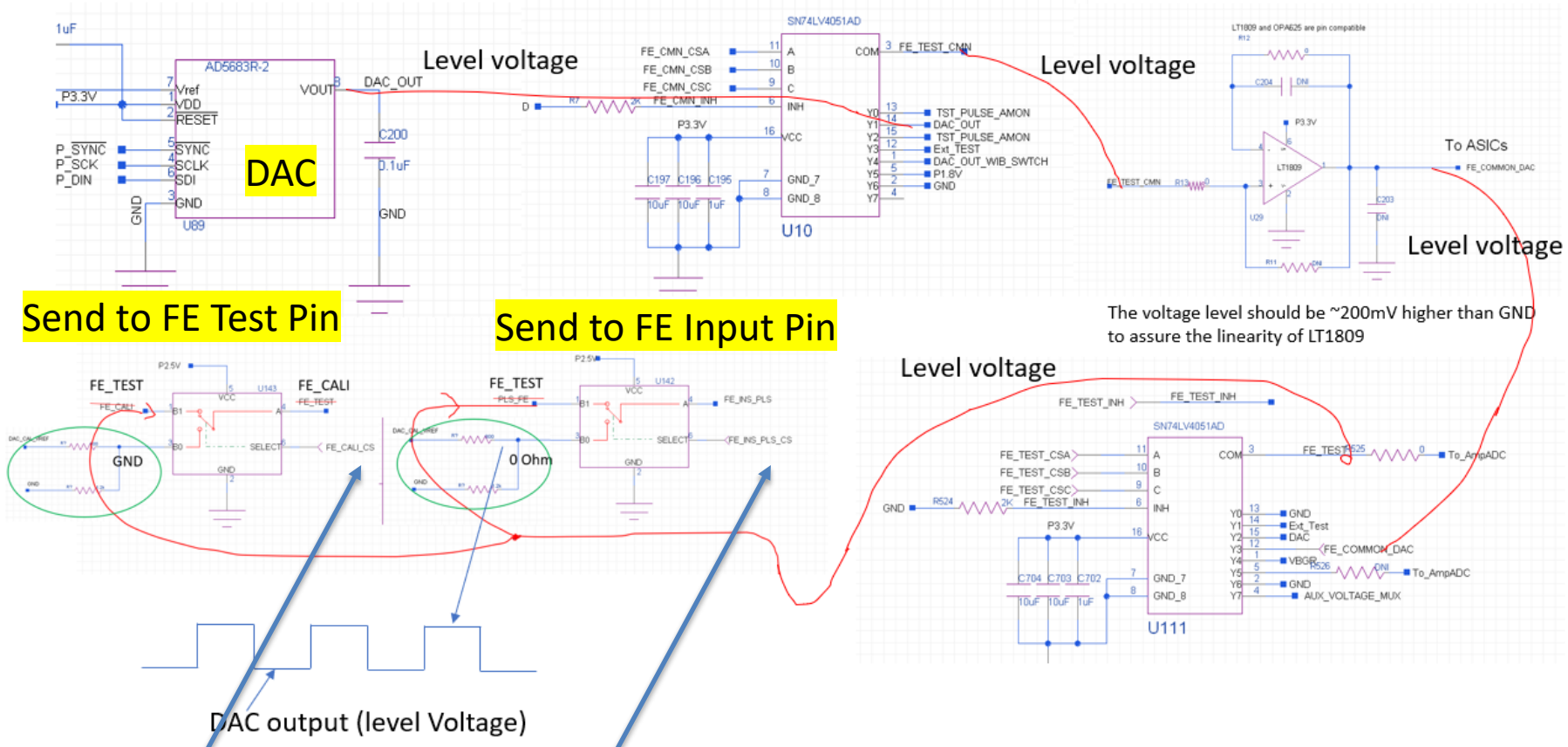
- Two CDCV304 for CD_I2C_**SCL**
- Two CDCV304 for CD_I2C_**SDA**_W2C



100Ohm serial resistors may mitigate the overshoot observed.

Revision: Remap FE calibration scheme

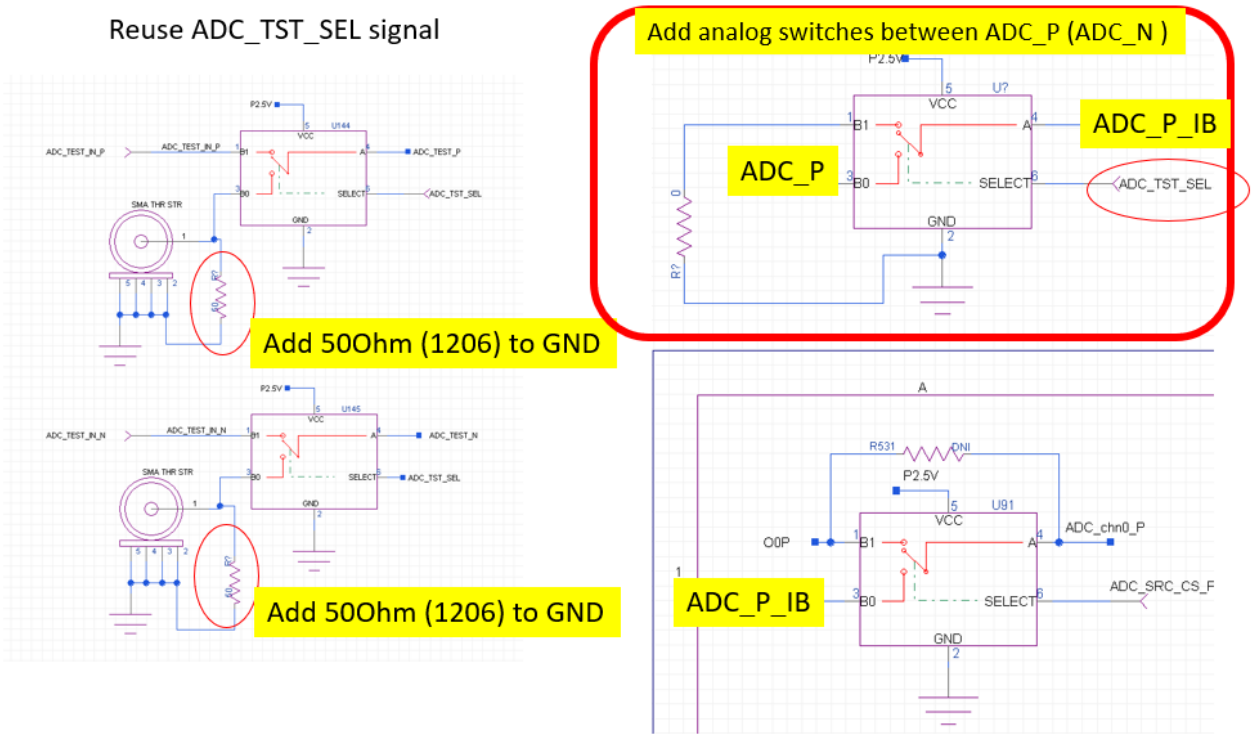
Proposed FE calibration scheme in use



Due to **FE?_CALI_CS** and **FE?_INS_PLS_CS** is directly controlled by FPGA IOs, we can **calibrate one FE channel at a time per board** if needed.

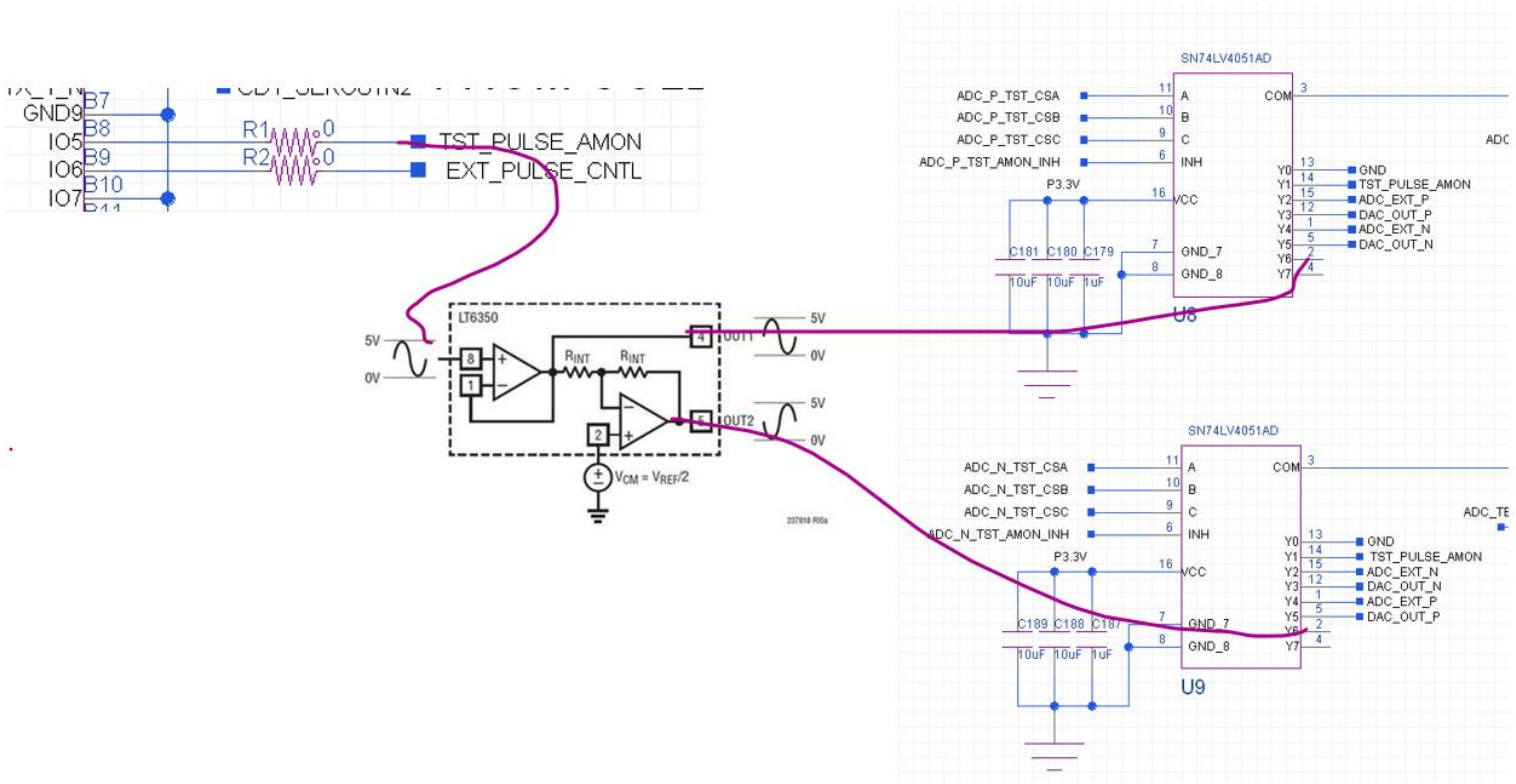
Revision: Remap ADC Test Scheme

- Calibrate one ADC channel at a time per board if needed
- There are 8 ADC_TST_SEL signals to control which ADC_Test pins connect to the SMA connectors. However, they are barely used.
- Add an analog switch controlled by ADC_TST_SEL, so that we can send external signal to each ColdADC channel independently.



Add a SE-to-DIFF Amplifier

- For analog input from WIB



Several SE-to-DIFF Amplifiers are under cold screening (THS4551, THS4531A, AD8137, LTC636, LTC1992)

COLDATA EFUSE Programming is Verified

- The programming procedure is determined
  - Step1: Send fast reset command to COLDATA
    - No other register operation on COLDATA after reset
      - Especially don't touch COLDATA page#0, reg#0x1f
  - Step 2: Start the EFUSE Programming following the timing sequence specified in datasheet
  - Step 3: Send fast reset command to COLDATA
  - Step 4: Check EFUSE programming status
    - If any bit should be programmed to '1' stays '0', go back to Step 1 and program EFUSE again
- Dave confirmed and updated P3 datasheet
  - Programming voltage is 2.5V
  - 32-bit for assigning unique chip ID
    - 16-bit for wafer batch number (0-65535)
    - 16-bit for chip ID under that batch (0-65535)

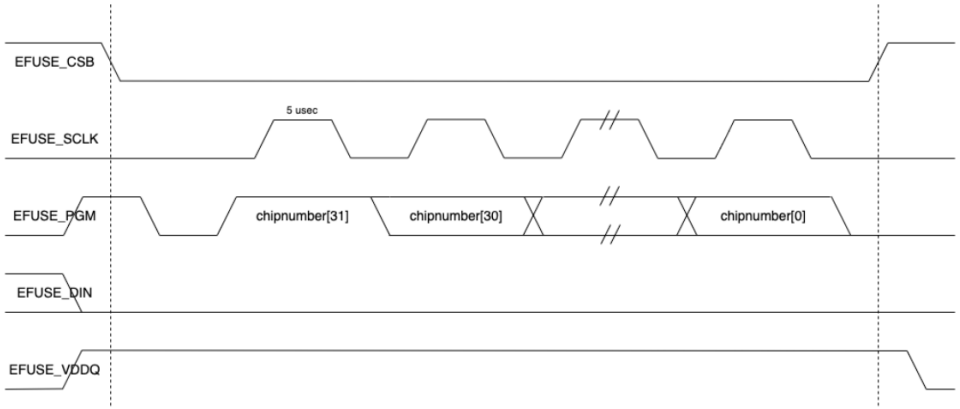
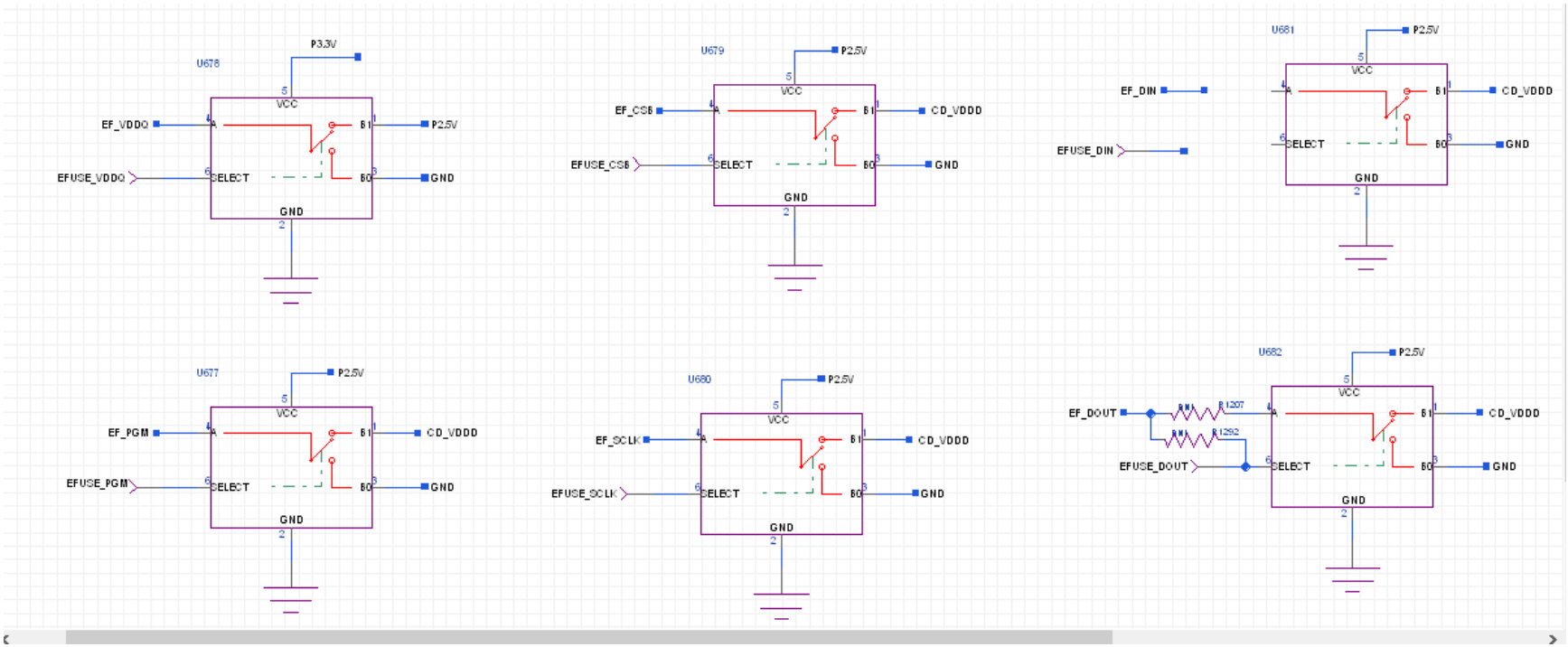


Figure 12: EFUSE Programming. EFUSE_VDDQ is the fuse-burning voltage and should be set to 2.5V (2.4-2.6V). The total time that EFUSE_VDDQ is on should be less than 1 second. The EFUSE control signals are 2.5V CMOS signals. EFUSE_SCLK should be held high for 5 microseconds for each bit to be programmed.

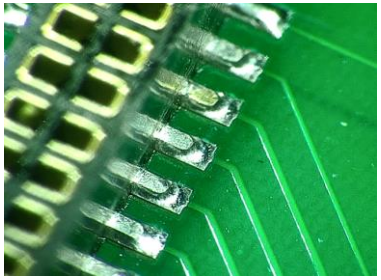
Add circuit for COLDATA EFUSE programming

- FPGA controls analog switches to drive EFUSE VDDQ and control signals instead of directly control EFUSE programming
  - FPGA IO has limited current strength
  - Control voltage level can be set by voltage divider

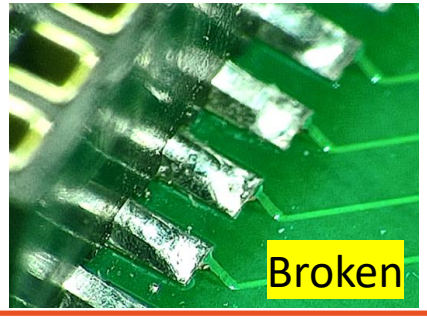


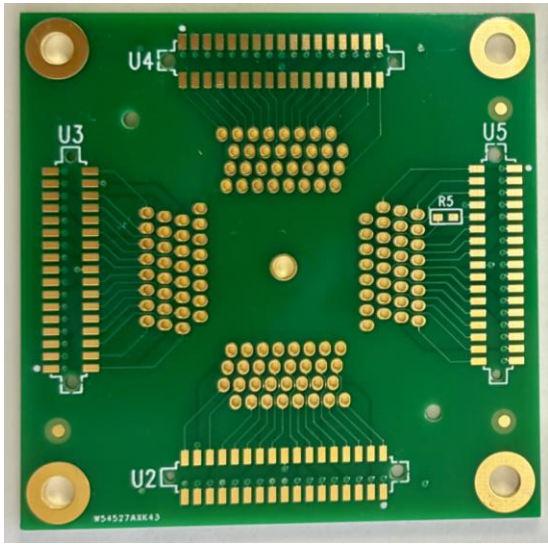
ASIC Socket Mezzanine Revision

- Surface footprint is fragile when replacing the ASIC socket mezzanine
- Layout update
  - Use via-in-pad for all mezzanine connector pad
  - Move all traces into inner layers, no routing on top/bottom layers
  - Add tear drop for vias on inner layers
  - Enlarge pad size as much as possible and keep the same solder mask opening, so called solder mask defined pad
- Similar layout request is applied on DAT as well

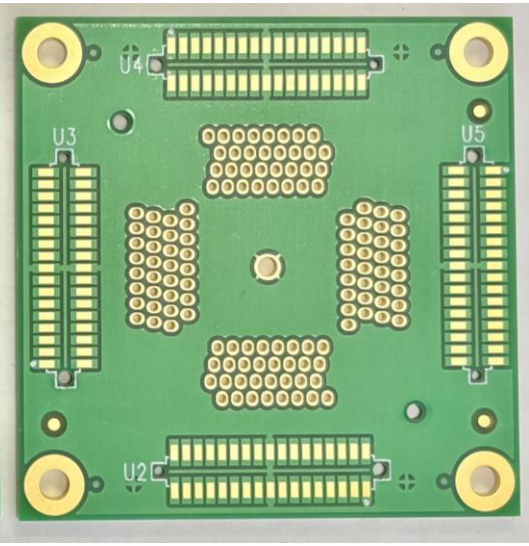


Good





Old layout



New layout

RTS arrived at BNL

- RTS arrived at BNL on 12/05
- Plan at BNL
  - Electrical inspection and safety for using 208V
  - Get familiar with Robot Programming

Summary

- Current DAT has been fully characterized to shows that it meets most ASIC QC requirement
  - With some flying wires, it can perform QC test for LArASIC, ColdADC and COLDATA
- A DAT revision is ongoing
  - Schematics is complete
  - Layout has started
    - A minor update will be made after Christmas when a cold SE-to-DIFF buffer is identified
  - New DAT is aimed to be ready for use in March 2024
    - Both WIB/DAT FPGA FW is available
  - Via-in-pad is applied in 128-pin socket mezzanine board
    - It will be applied on DAT and 208-pin socket mezzanine board