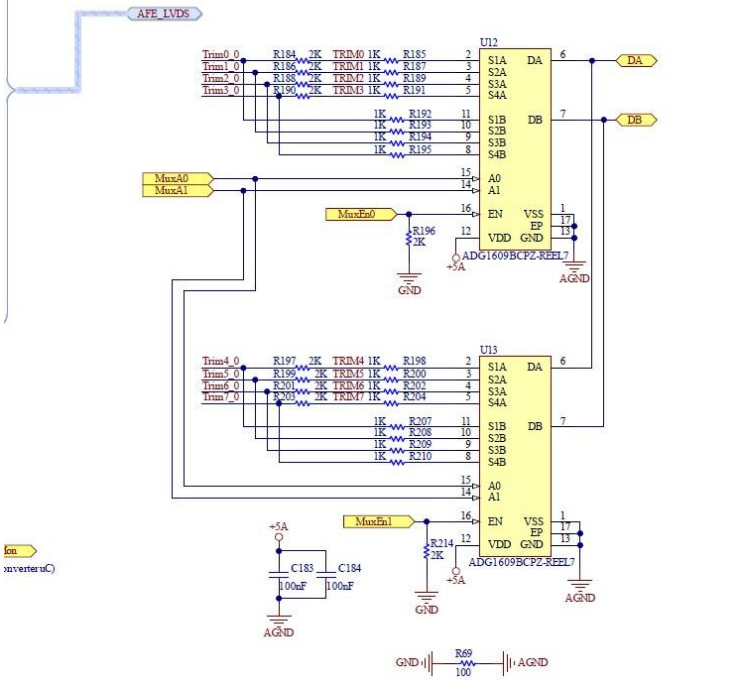
DAPHNE Status

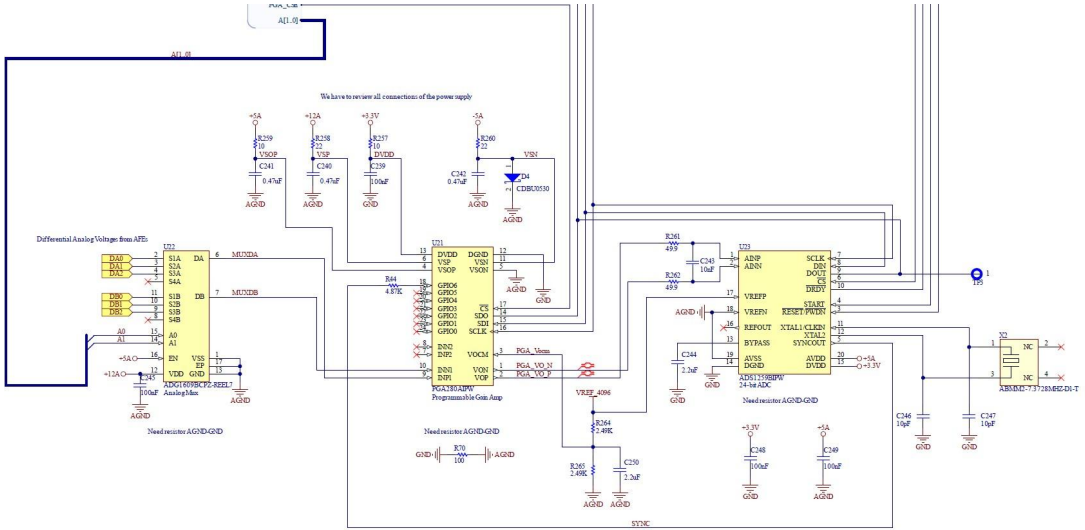
Deywis Moreno
Consortium Meeting
December 12, 2023

Outline

- DAPHNE_V2A firmware
- Self-trigger
- DAPHNE_V3 update

Current Monitoring



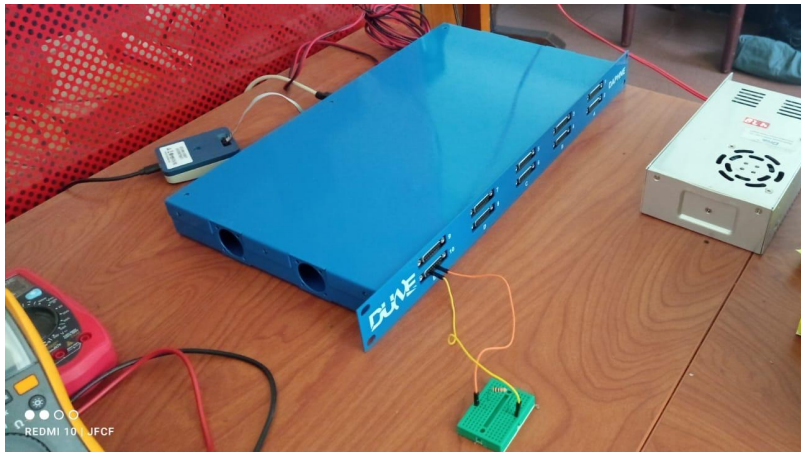


PGA280+ADS1259

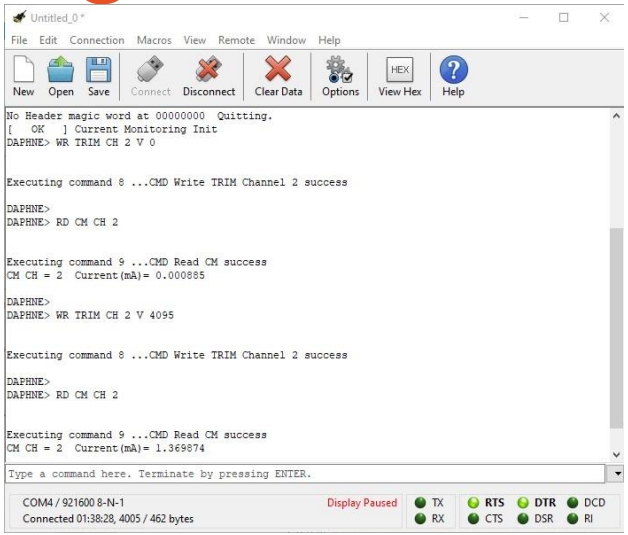
Analog mux to select the Trim current to be measured

Current on Load Resistor calculated from the Voltage measured by the 24-bit ADC

Current Monitoring Testing



Tests performed on DAPHNE V1 at UAN and Fermilab

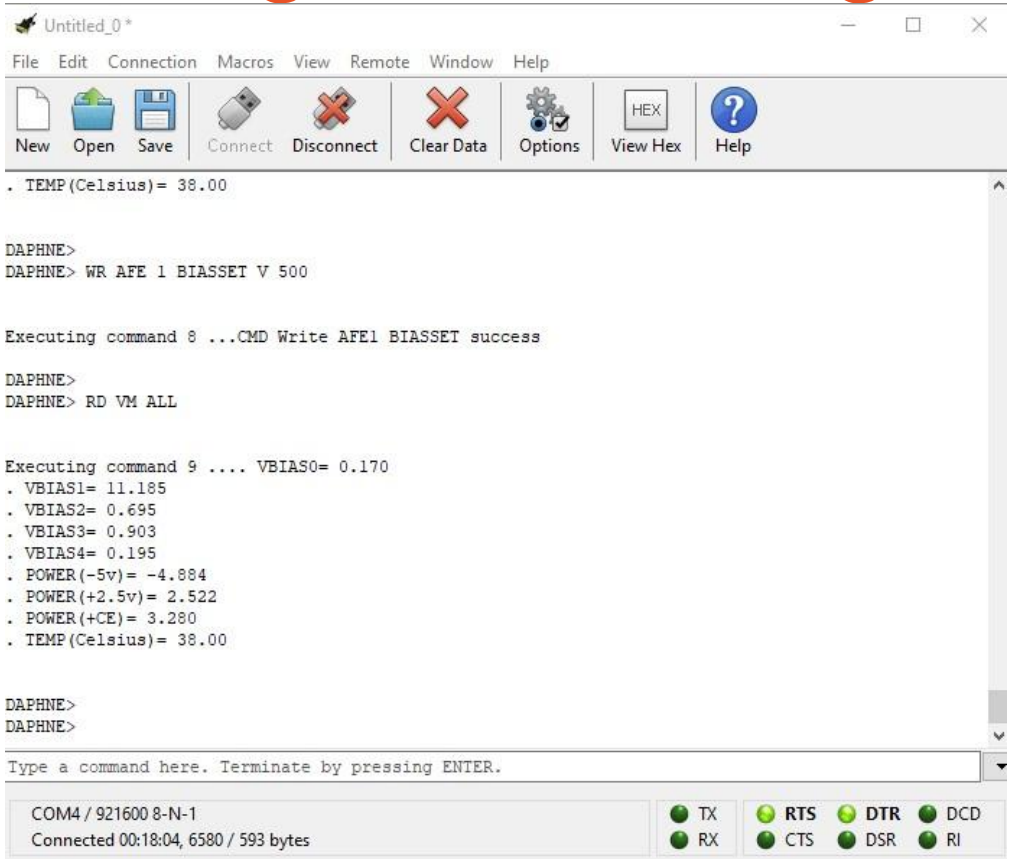


1K resistor connected between Trim 2 (pin 11) and AGND (using the Cold Electronics VR pin 14), E connector

WR TRIM CH xx V yy: set Trim Voltage on channel xx to yy value (from 0 to 4095 referred to DAC output). We will implement a command that take this value in Volts

RD CM CH X: measurement of the SiPM current of channel X (in mA)

Voltage Monitoring Test



WR VBIASCTRL V xx: set the General Bias to XX (from 0 to 1000), referred to DAC output from 0 to 1 V (DC-DC converter)

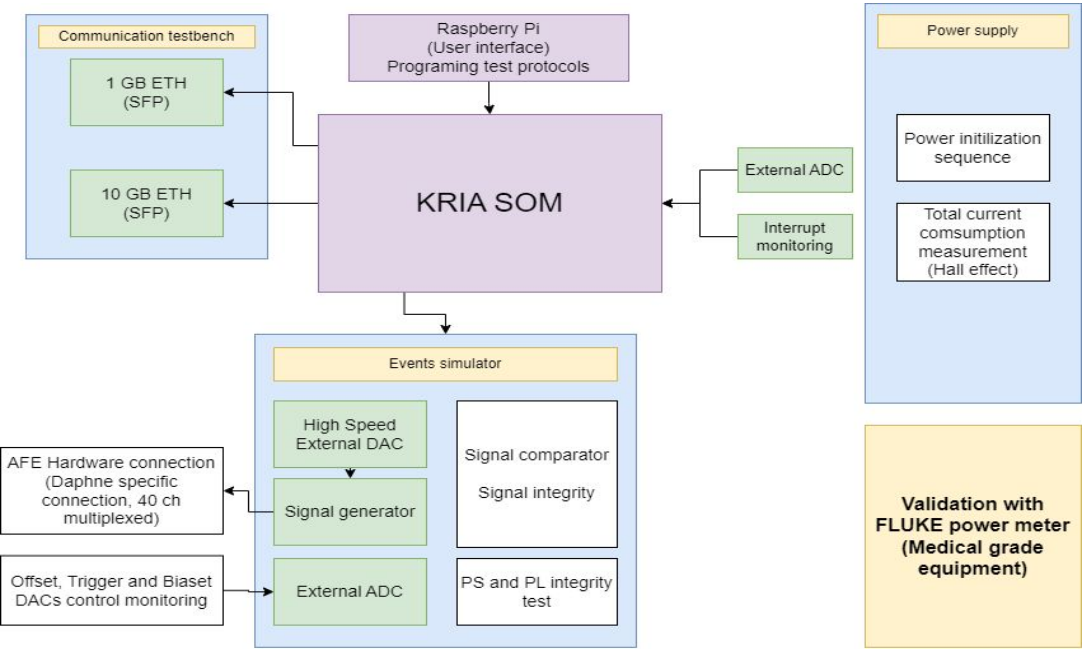
WR AFE X BIASSET V YY: set voltage on AFE X (from 0 to 4) to YY (from 0 to 4095 referred to DAC output), we will implement an update to enter the direct value in volts

RD VM ALL: measurement of the VBias (from 0 to 4) in volts, power supplies (-5V, 2,5 V, Cold electronics) and microcontroller temperature

Monitoring Work Ongoing

- Calibration of the Voltage monitoring
- Improvement of the uC temperature measurement (calibration, mathematical model, etc) according to the datasheet
- Verification and calibration of the CM analog multiplexing circuit (originally designed by Sten H. for Mu2E FEB)
- Experimental test performed on DAPHNE V2 at Milano-Bicocca in with the help of Esteban C. (Scheduled for December 12th 2023)

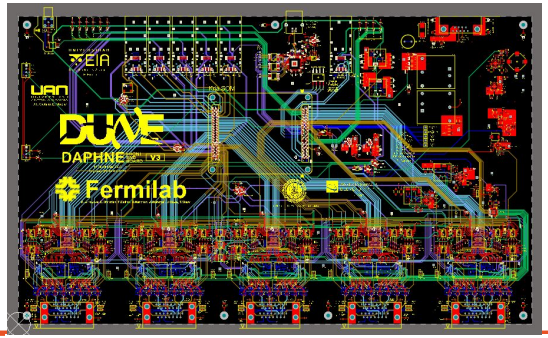
High-performance test bench for the automation of DAPHNE board minimum performance tests



Test bench Architecture

Timming signals	Voltage signals	Clock signals	Power signals	Columna1
AFE_CLK_P	TRIM[7..0]	CLK625_P	VREF_4096	PG3V3A
AFE_CLK_N	OFFSET[7..0]	CLK625_N		PG1V8A
	VBIAS_CTRL	CLK100_P	+3.3VDPS	+3.3VA
GTH_REFCLK_P	BIAS_SET[4..0]	CLK100_N	+5VD	PG1V8A
GTH_REFCLK_N	VGAIN[4..0]		+1.8VDPS	+5.5V
		25MHZ_CLK	+3.3VD	+3.6V
	VBiasRaw		+1.8VD	-5VA
	BiasSet			+5VA
	BiasMon			
	DA			
	DB			

- Signal's definition and test point validation

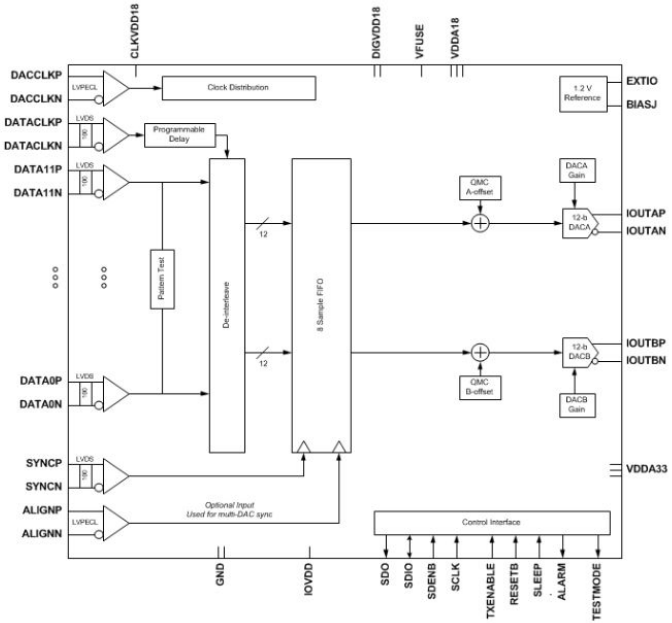


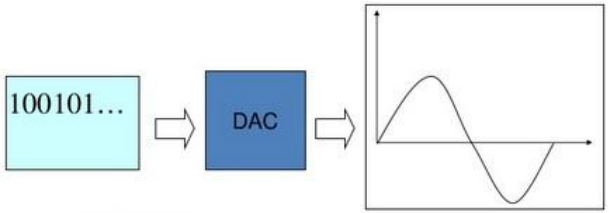
Test bench as event signal simulator

Part selection

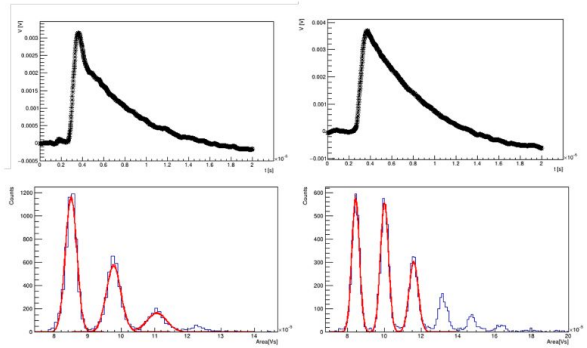
DAC31154 ACTIVE

Dual-channel, 10-bit, 500-MSPS digital-to-analog converter (DAC) with input FIFO and current sour

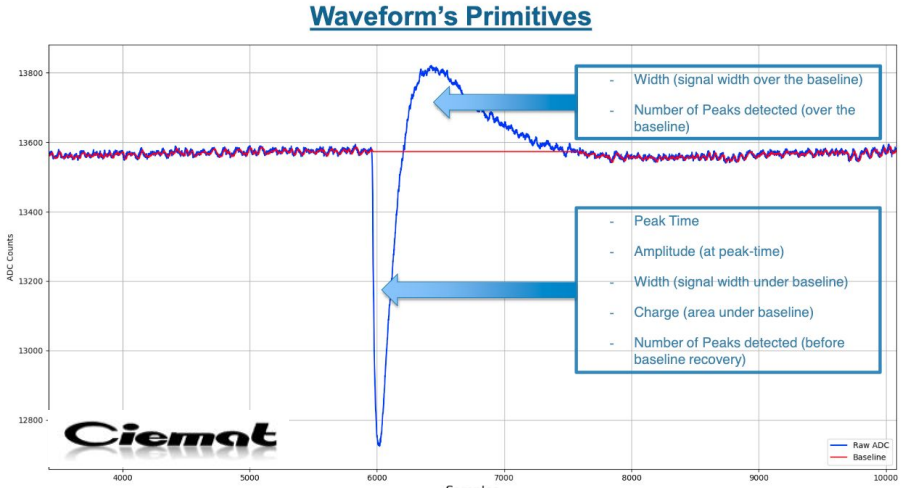


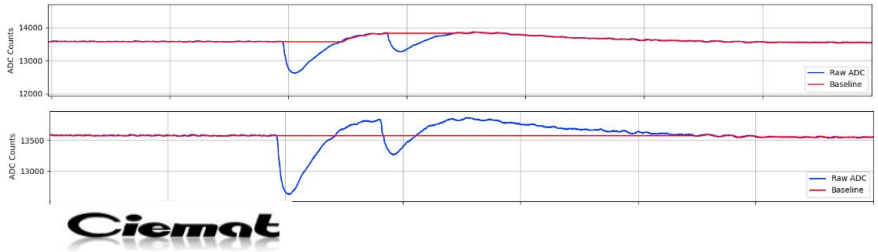


LoopBack with AFE5808A



Self-Triggering





- Different algorithms are under testing at Ciemat
- University EIA is also working in a match filter for triggering
- In previous WG meetings discussions for a join work is planned

Self-trigger algorithm for the Photon Detection System(PDS) in DUNE

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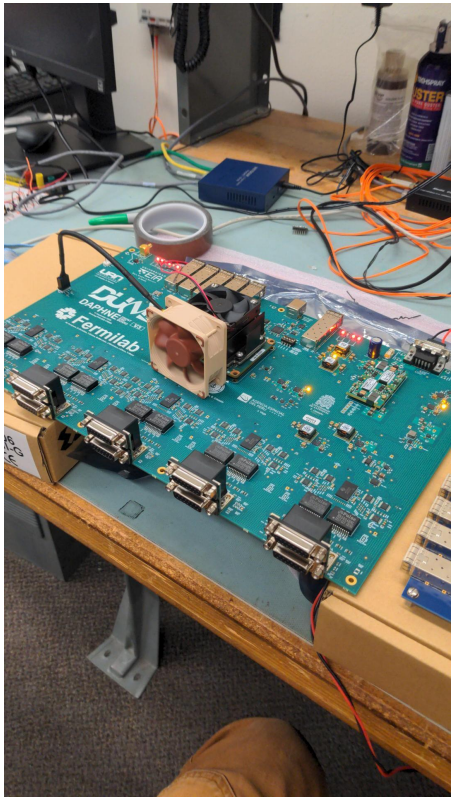
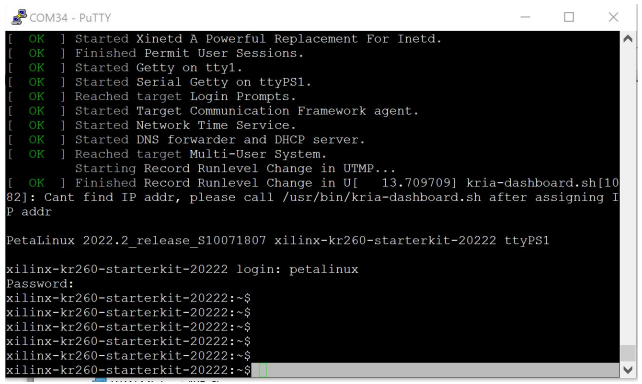
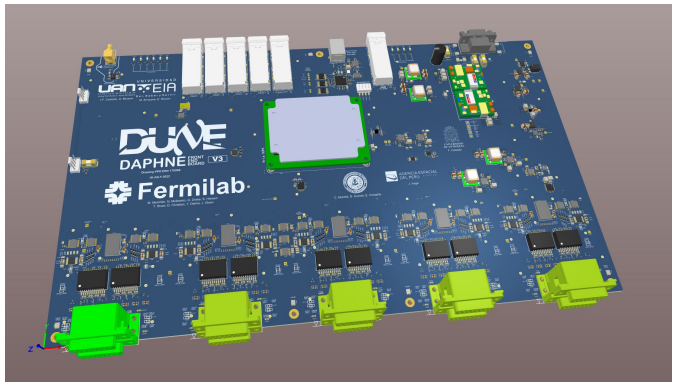
DAPHNE_V3



- 12 PCBs produced; 10 DAPHNE_V3 assembled
- 2 DAPHNE_V3 were delivered (vendor was unsure of ball grid array quality)
  - Many bad ball grid array connections found
  - Boards were reworked (all BGA connections reflowed individually). 1 board now looks good & is being tested, the other has no obvious BGA problems, but the Kria SOM doesn't boot properly.
  - Decision to rework the remaining 8 boards will be made this week.





Work ongoing

- DAPHNE V2A installation and integration at CERN is progressing
- Design of a DAPHNE test bench ongoing
- Self-Trigger algorithms under development in many labs. Performance Comparison needs to be done
- DAPHNE_V3 testing is ongoing; decision on rework of remaining 8 boards will be made late this week.