Triggers for hadron colliders at the energy frontier

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Outline:

- LHC Luminosity Upgrade & Challenges
- Upgrade Tools: FPGAs, ATCA, Transceivers, GPU, PCIe
- Upgrade Trigger Strategies for ATLAS & CMS

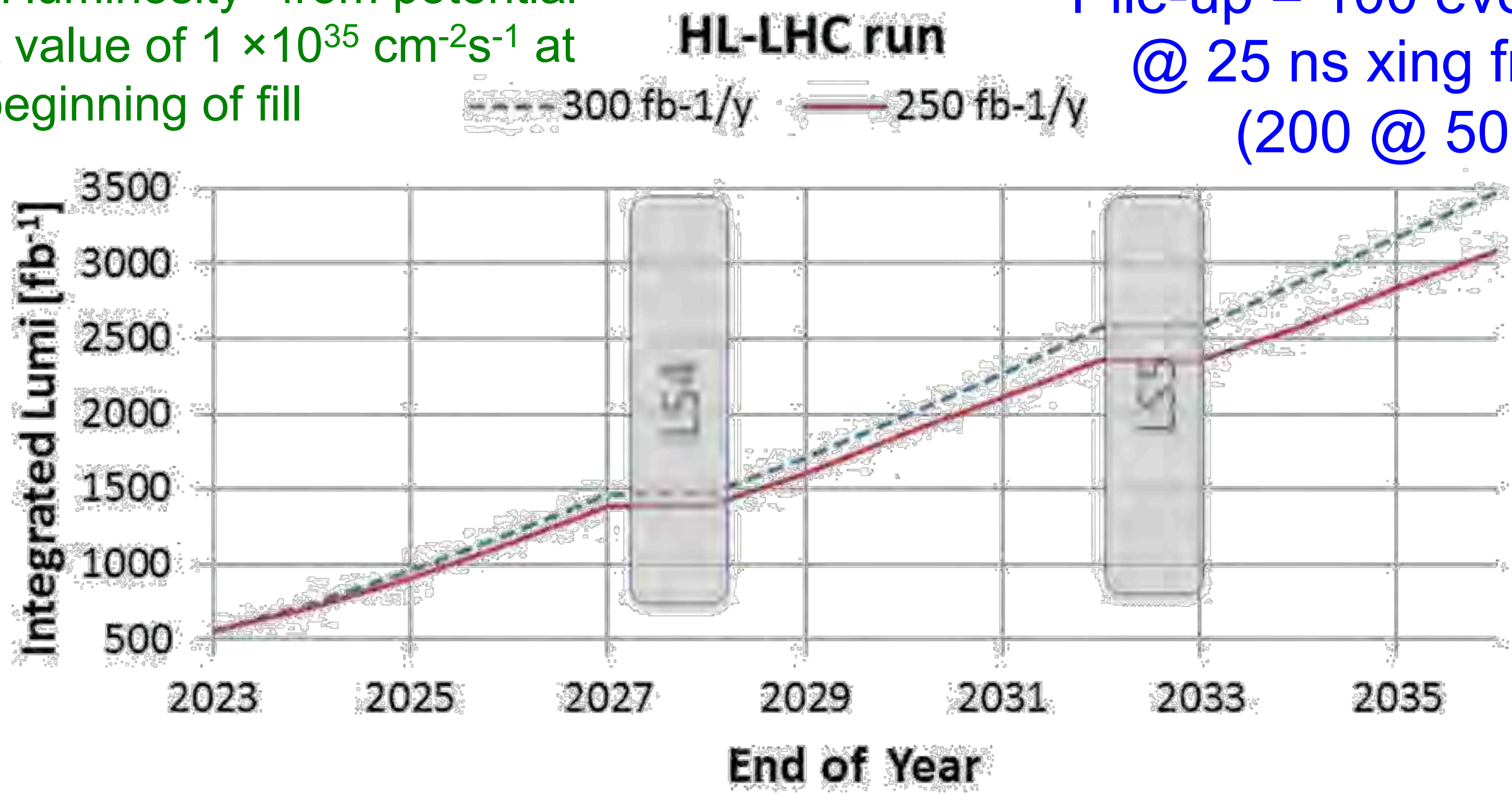
HL-LHC: 2023 onward: Phase 2

3000 fb^{-1} in a 10-12 year run

Peak Luminosity: 5×10^{34}*

Level luminosity^{-1} from potential peak value of 1×10^{35} cm^{-2}s^{-1} at the beginning of fill

Pile-up = 100 events @ 25 ns xing freq. (200 @ 50 ns)



ATLAS & CMS High Luminosity Motivation

Establish nature of Higgs boson and of EWSB:

- fundamental or composite?
- how many doublets? singlets? charged H's?

Need to measure, as accurately as possible:

- Higgs couplings to fermions, gauge bosons & self-couplings
- Rare decay modes, possible Flavor Changing Neutral Current
- WW scattering at high E
- Gauge boson self-couplings

Example:

- Higgs: $H \rightarrow Z\gamma$ @ 3.5/11 σ with 600/6000 fb^{-1}
  or $H \rightarrow \mu+\mu-$ < 3.5σ for 600 fb^{-1} and ~ 7σ for 6000 fb^{-1}

Requirements for LHC phases of the upgrades: ~2010-2030

Phase 1: (until 2021)

- Goal of extended running in second half of decade to collect ~100s/fb
- 80% of this luminosity in last three years of this decade
- About half the luminosity would be delivered at luminosities above the original LHC design luminosity
- Trigger & DAQ systems should be able to operate with a peak luminosity of up to 2 x 10^{34}

Phase 2: High Lumi LHC (2023+)

- Continued operation of the LHC beyond a few 100/fb will require substantial modification of detector elements
- Goal is to achieve 3000/fb in phase 2
- Need to be able to integrate ~300/fb-yr
- Will require new tracking detectors for ATLAS & CMS
- Trigger & DAQ systems should be able to operate with a peak luminosity of up to 5 x 10^{34}

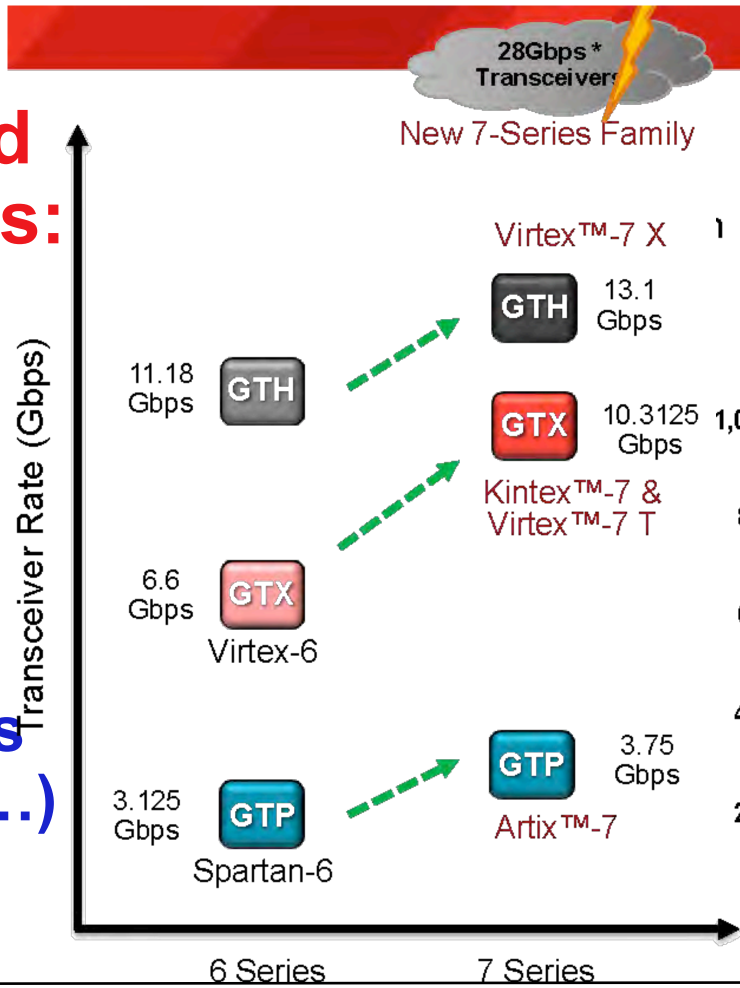
Tools for Upgrades: FPGAs

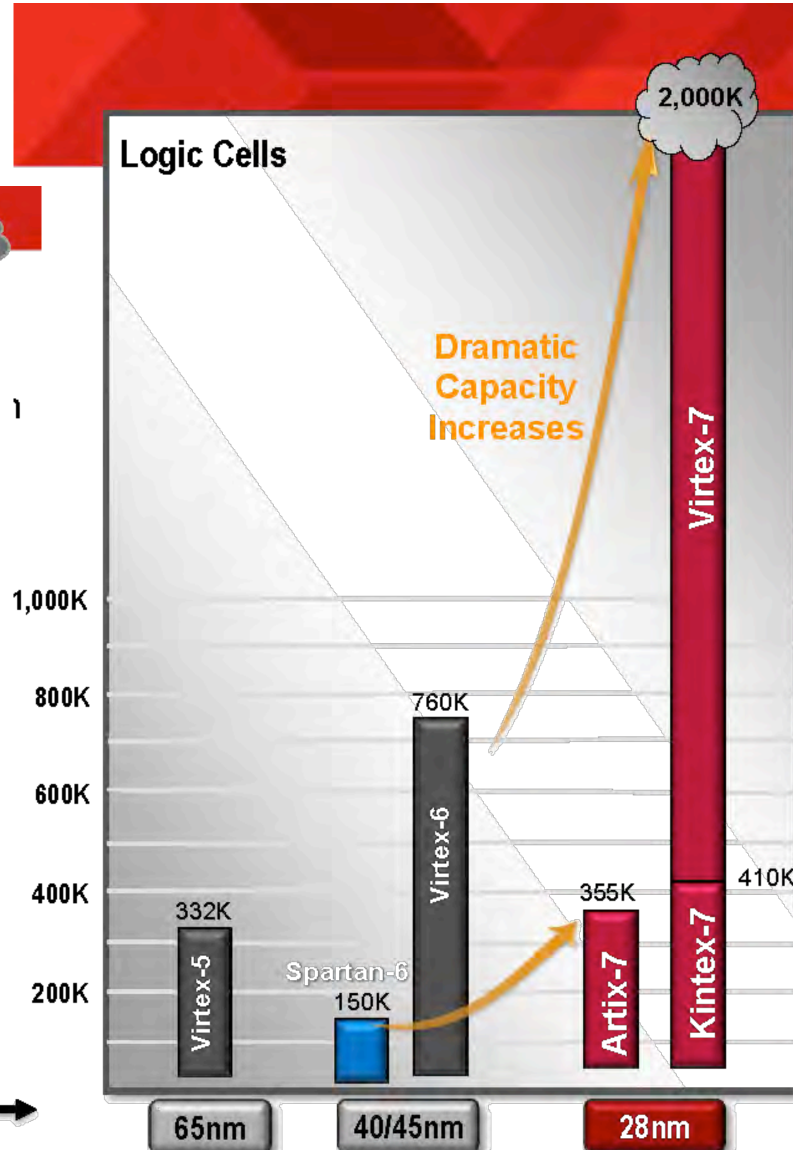
Logic Cells

- 28 nm: > 2X gains over 40 nm→

On-Chip High Speed Serial Links:

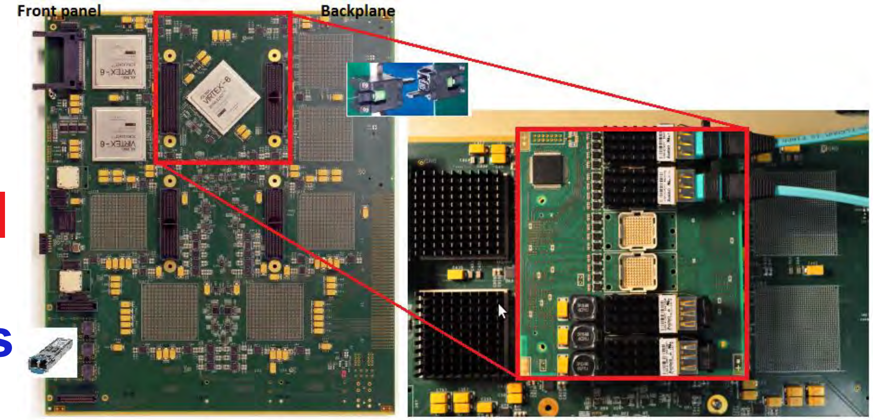
- Connect to new compact high density optical connectors (SNAP-12…)





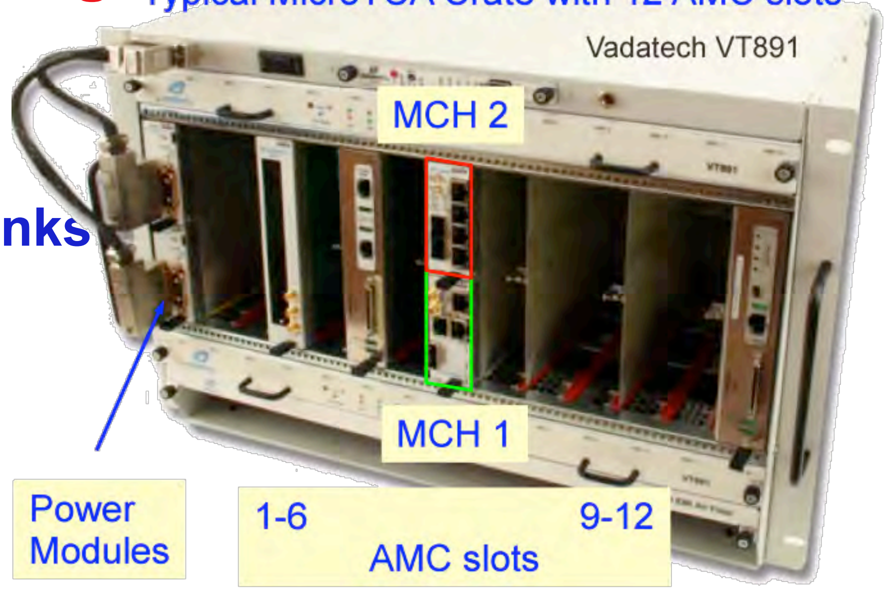
Tools for upgrades: ATCA

- **Advanced Telecommunications Computing Architecture ATCA**
- **Example: ATLAS Upgrade Calorimeter Trigger Topological Processor Card**
  - **12-chan. ribbon fiber optic modules**
  - **Backpl. opt. ribbon fiber connector**



- **Example: µTCA derived from AMC std. used by CMS HCAL, Trig.**
  - **Advanced Mezzanine Card**
  - **Up to 12 AMC slots**
    - *Processing modules*
  - **6 standard 10Gb/s point-to -point links slot to hub slots (more available)**
  - **Redundant power, controls,clocks**
  - **Each AMC can have in principle (20) 10 Gb/sec ports**
  - **Backplane customization is routine & inexpensive**

Typical MicroTCA Crate with 12 AMC slots



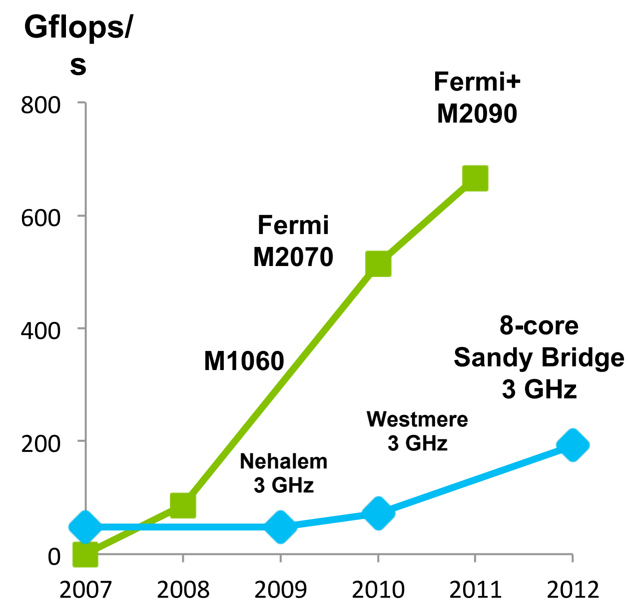
Tools cont'd: CPU, GPU, PCIe

CPU Gains for High Level Triggers: Moore's Law

GPU Enhancement of HLT →

- GPU performance tracks Moore's Law, since GPU architecture is scalable:
  - Large Increase in memory bandwidth x10 in Gbytes/s
  - Power efficient x3 with latest GPU card
  - Well suited to tracking, fitting algorithms

Peak Double Precision FP



Enhancement of detector to DAQ readout:

- **PCI Express Gen3 Cards now available**
- **Up to 56Gb/s InfiniBand or 40 Gigabit Ethernet per port**

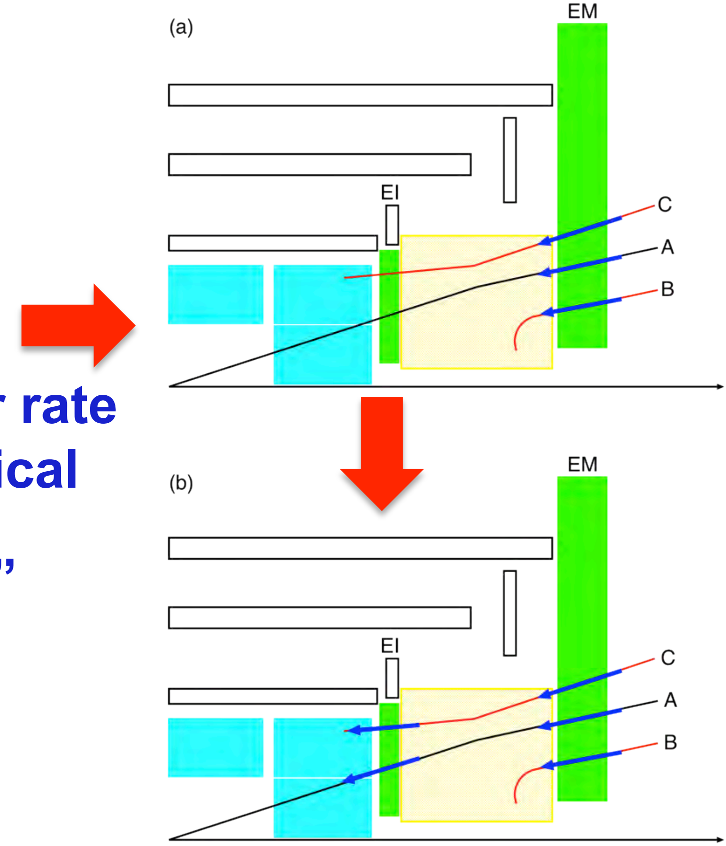
ATLAS Upgrade Trigger Strategy

Near Future (2014)

- New calorimeter trigger & central trigger processor modules provide topological triggers, more triggers

Phase 1:

- “New Small Wheel” provides inner track segments to reduce endcap muon trigger rate
- Muon trigger upgrade to provide topological triggers
- Calorimeter trigger digital “preprocessor” & feature extractors allow use of finer granularity information
- Latency & L1 Trigger Rate stay same through phase 1



Phase 2 Options:

- Divide L1 trigger into L0, L1 of latency 5, 20 μsec, rate < 500, 200 kHz
- L0 uses Calo & Muon Triggers, generates track trigger seeds
- L1 uses track trigger & more muon detectors & more fine-grained calorimeter trigger information.

CMS Upgrade Trigger Strategy

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Constraints

- Output rate at 100 kHz
- Input rate increases x2/x10 (Phase 1/Phase 2) over LHC design (10^{34})
  - Same x2 if crossing freq/2, e.g. 25 ns spacing → 50 ns at 10^{34}
- Number of interactions in a crossing (Pileup) goes up by x4/x20
- Thresholds remain ~ same as physics interest does

Example: strategy for Phase 1 Calorimeter Trigger

- Present L1 algorithms inadequate above 10^{34}
  - Pileup degrades object isolation
- More sophisticated clustering & isolation deal w/more busy events
  - Process with full granularity of calorimeter trigger information
- Should suffice for x2 reduction in rate as shown with initial L1 Trigger studies & CMS HLT studies with L2 algorithms

Potential new handles at L1 needed for x10 (Phase 2: 2023+)

- Tracking to eliminate fakes, use track isolation.
- Vertexing to ensure that multiple trigger objects come from same interaction
- Requires finer position resolution for calorimeter trigger objects for matching (provided by use of full granularity cal. trig. info.)

CMS Phase 2: Tracker input to L1 Trigger

Use of Tracker input to Level-1 trigger

- **μ, e and jet rates would exceed 100 kHz at high luminosity**
  - Even considering "phase-1" trigger upgrades
- **Increasing thresholds would affect physics performance**
  - Performance of algorithms degrades with increasing pile-up
    - **Muons: increased background rates from accidental coincidences**
    - **Electrons/photons: reduced QCD rejection at fixed efficiency from isolation**
- **Add tracking information at Level-1**
  - Move part of HLT reconstruction into Level-1!

Full-scope objectives:

- **Reconstruct "all" tracks above 2 - 2.5 GeV**
- **Identify the origin along the beam axis with ~ 1 mm precision**

CMS Track Trigger Architectures: Phase 2

"Push" path:

- L1 tracking trigger data combined with calorimeter & muon trigger data regionally with finer granularity than presently employed.
- After regional correlation stage, physics objects made from tracking, calorimeter & muon regional trigger data transmitted to Global Trigger.

"Pull" path:

- L1 calorimeter & muon triggers produce a "Level-0" or L0 "pre-trigger" after latency of present L1 trigger, with request for tracking info at ~1 MHz. Request only goes to regions of tracker where candidate was found. Reduces data transmitted from tracker to L1 trigger logic by 40 (40 MHz to 1 MHz) times probability of a tracker region to be found with candidates, which could be less than 10%.
- Tracker sends out info. for these regions only & this data is combined in L1 correlation logic, resulting in L1A combining track, muon & cal. info..
- Only on-detector tracking trigger logic in specific region would see L0

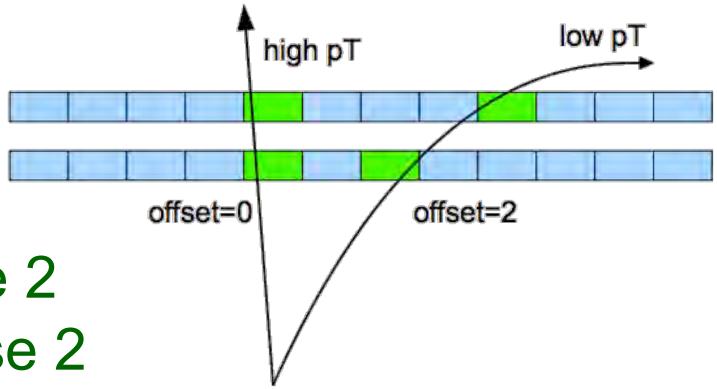
"Afterburner" path:

- L1 Track trigger info, along with rest of information provided to L1 is used at very first stage of HLT processing. Provides track information to HLT algorithms very quickly without having to unpack & process large volume of tracker information through CPU-intensive algorithms. Helps limit the need for significant additional processor power in HLT computer farm.

ATLAS Trigger Upgrades

Various projects being pursued:

- **Track trigger**
  - Fast Track Finder (FTK), hardware track finder for ATLAS (at L1.5)
    - **Phase 1**
  - ROI based track trigger at L1 – Phase 2
  - Self seeded track trigger at L1 – Phase 2



- **Combining trigger objects at L1 & topological "analysis"**
  - Phase 1 & 2
- **Full granularity readout of calorimeter**
  - requires new electronics – Phase 2
- **Changes in muon systems (small wheels), studies of an MDT based trigger & changes in electronics – Phase 1**
- **Upgrades of HLT farms**

Some of the changes are linked to possibilities that open when electronics changes are made (increased granularity, improved resolution & increased latency)

ATLAS L1 Track Trigger Design Options for Phase 2

Region Of Interest based Track Trigger at L1

- **uses ROIs from L1Calo & L1Muon to seed track finding**
- **has a large impact on the Trigger architecture**
  - requires significantly lengthened L1 pipelines and fast access to L1Calo and L1Muon ROI information
  - could also consider seeding this with an early ("Level-0") trigger, or sending a late ("Level-1.5") track trigger
- **smaller impact on Silicon readout electronics**

Self-Seeded Track Trigger at L1

- **independent of other trigger information**
- **has a large impact on Silicon readout electronics**
  - requires fast access to Silicon detector data at 40 MHz
- **smaller impact on the Trigger architecture**

Summary

- Very significant challenges to operate trigger & DAQ systems for high rate hadron collider detectors
- Very substantial assets to bring to bear on these challenges from commercial world: ATCA, FPGAs, high speed links (transceivers), optical connectors …
- Exploiting these assets enables physics input to drive much more precise selection of events and processing of a much higher volume of data.
  - e.g. a level-1 tracking trigger for ATLAS & CMS
- There is considerable technical difficulty involved in successfully exploiting these advances in technology and implementing them in running experiments in a controlled and adiabatic manner.