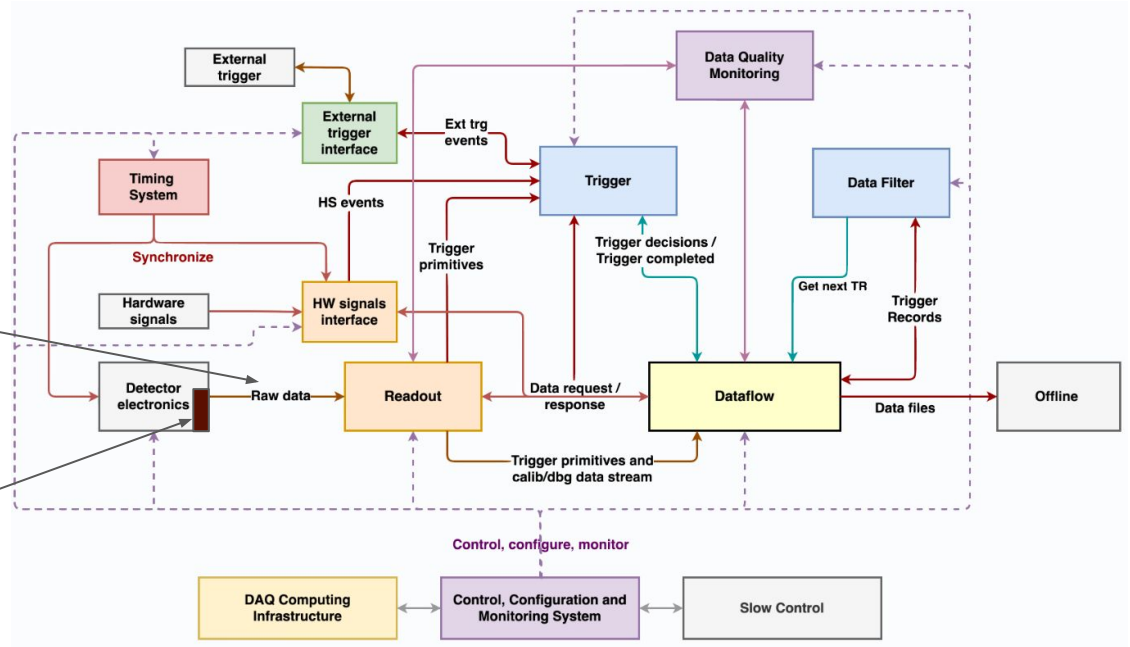# DAQ WG Status Report

Nicolò Tosi for the DAQ WG

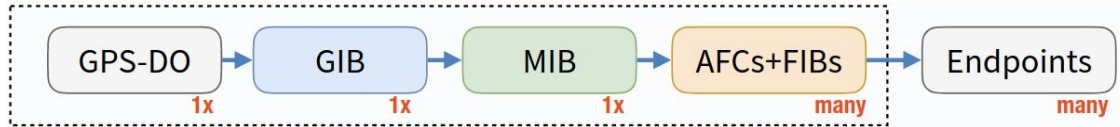# Quick recap of central DAQ and Timing architecture

- DAQ is based on Ethernet, timing is based on a custom protocol over Fiber

- Central DAQ expects 10G fibers from endpoints

- Central DAQ maintains a firmware block to be integrated in the endpoints
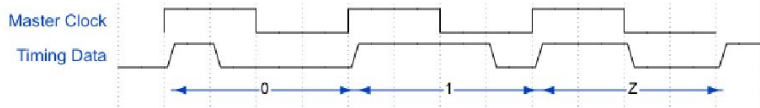
DAQ is optimized for FD, ND is somewhat simpler

Quick recap of central DAQ and Timing architecture

uTCA Crate (1 for all NDs)

GPS-DO → GIB → MIB → AFCs+FIBs → Endpoints
1x   1x   1x   many   many

Fiber transmits encoded clock (62.5 MHz and data (timestamps, sync command, spill, …)

Master Clock
Timing Data
0   1   Z

Endpoints transmit back for delay compensation

GIB v1

MIB v2

FIB v1+ AFC v4

8 Fibers per FIB, 8 Endpoints per fiber

Quick recap of central DAQ and Timing architecture

- We asked for O(10)-O(100) ps rms depending on subdetector
  - Both **between** and **within** subdetectors
  - Our strongest requirement applies only within a spill
  - DTS only "promised" O(100) ps
  - But they meant long term (i.e. drift), short term is better

- **The requirement can be met**
  - Within a spill, and a group of endpoints

PLL BW	Skew stdev.
100Hz	31 ps
400Hz	6.9 ps
1kHz	2.8 ps
4kHz	1.8 ps

From https://indico.fnal.gov/event/61796/

Open Questions

- More detailed measurements of variance per endpoint group
  - So far only hard numbers for groups of 8 (same fiber)
  - Requires full uTCA crate with GIB, MIB, FIB(s)
  - System will be available at CERN for ProtoDUNE operation

- Beam timing measurement from accelerator seems lacking
  - Certainly does not reach O(100) ps
  - From our meetings with ND, Timing, TMS, there is consensus on having dedicated hardware

Plans for SAND subdetectors: GRAIN

GRAIN most closely mirrors the architecture of
the FD for which DUNE DAQ was designed:

- **Cold** *camera board* inside cryostat, with
  the SiPMs and ASIC
- Cryo-vacuum feedthrough
- **Warm** *interface board*, connected to ~8
  camera boards
- The *interface board* will be an endpoint for
  the DAQ, timing and slow control
  - Implemented using the same type of
    hardware of the FD, i.e. an AMD Zynq or
    similar (FPGA + ARM CPU)
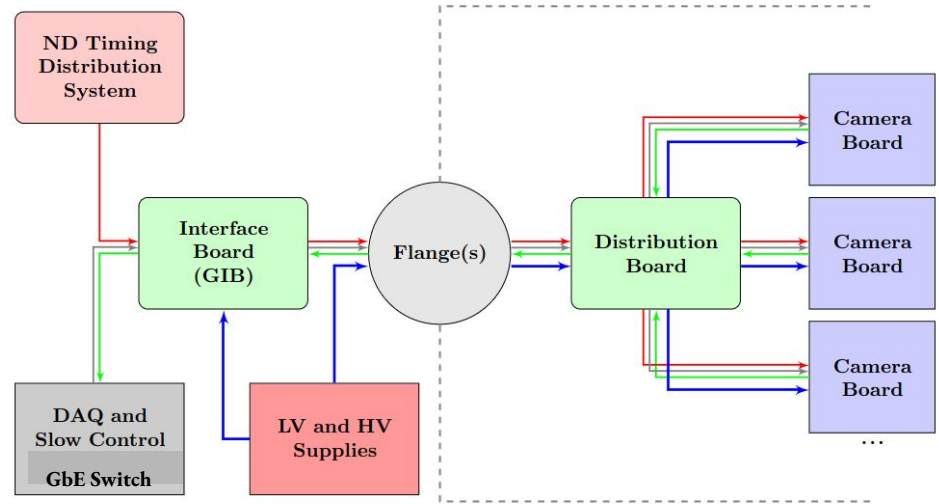
From the future GRAIN ASIC requirement document
https://www.overleaf.com/read/fzqtfwdqkpyn#9f1f56

Groups involved: BO, GE, TO   DAQ WG contact: Sergio and Nicolò

Plans for SAND subdetectors: ECAL

Meeting with CAEN during Jan CM:

- Readout based on current Preamp + Discriminator + picoTDC explored
  - There is potential but not all physics requirements demonstrated
- Integration with DAQ non trivial
  - CAEN solution based on FERS boards
  - FERS concentrator would be modified to serve as DAQ/Timing/SC endpoint
  - Technical challenges and IP/maintenance/support concerns
  - Degradation and additional complexity of timing distribution (two systems in sequence)

- Alternative in-house solution could be pursued, but there is no one working on it

Groups involved: CAEN, ROMA1   DAQ WG contact: **<open position>**

Plans for SAND subdetectors: STT

Deferred item: will be discussed later

Groups involved: SC (Roberto), **??**   DAQ WG contact: **<open position>**

Activities in progress (Q1 2024)

- Planning of extended tests of the Timing system
  - Primary contact: Dave Cussans, Bristol
  - Aim is to prepare a test to confirm timing variance over endpoints from different fibers

- Initial discussion on a Beam Synchronization Device
  - Coordinate with FNAL, LBNF Project, other ND (especially TMS), etc …
  - Desire to specify a *fast* beam pickup upstream of target (coil, RW, …), to get better beam synchronization than baseline proposal

- Identifying a reasonable TDR-level design for STT and ECAL
  - Including potential alternate solutions

Future activities planned for 2024

- Timing tests (Q2-Q3 depending on Protodune exact schedule)

- TDR writing, including items that have not been addressed so far:
  - Slow control (hardware and software side)
  - Software side of DAQ (including online software "trigger", e.g. for cosmics/calibration)

- …

Draft contents of DAQ chapter of the TDR

- DAQ Architecture

- Detector Control (DCS) and Detector Safety system (DSS)

- Timing System

  - Trigger System

  - Calibration

- DAQ/DCS Interface description:

  - GRAIN (starting from the ASIC doc https://www.overleaf.com/read/fzqtfwdqkpyn#9f1f56)

  - STT

  - Calorimeter