

Introduction

Cheng-Ju Lin

Lawrence Berkeley National Laboratory

Power & Timing Card Procurement Readiness Review

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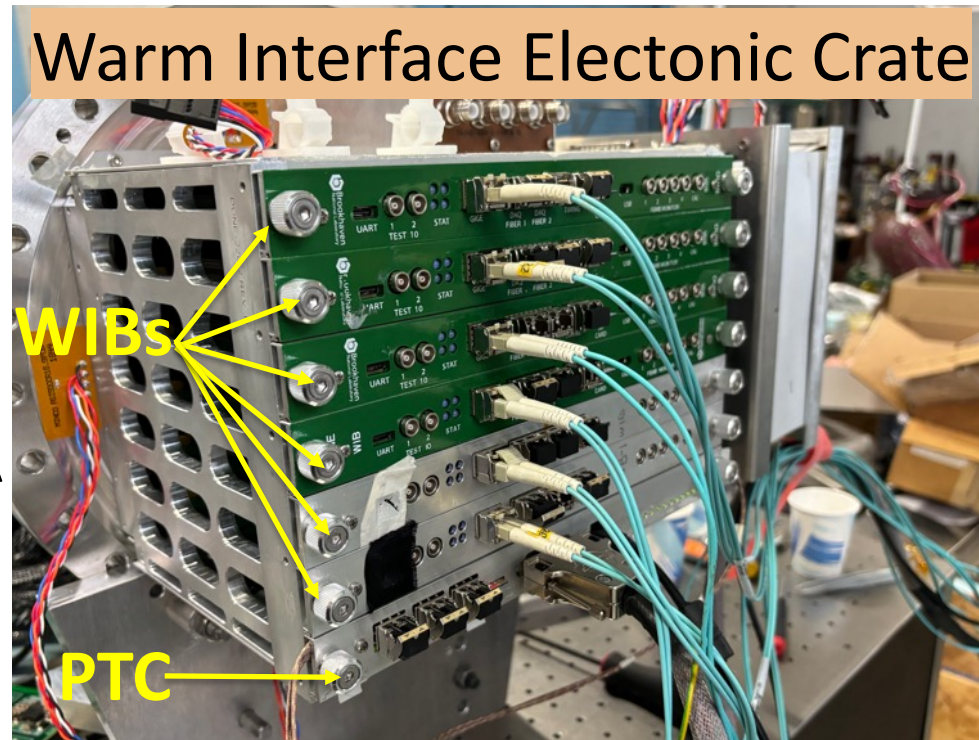
**Thank you for taking time to serve on the PTC
Procurement Readiness Review**

**Your assessments and recommendations are
important to us**



Introduction

- Power & Timing Card (PTC) distributes power and timing information to the Warm Interface Boards and Frontend Motherboards
- PTC was upgraded to add monitoring functionality. Also added interfaces for Slow Control and CE Safety Interlock system (see Adrian's talk for details)
- One PTC per Warm Interface Electronic crate (WIEC): 150 PTCs for FD1 and 80 PTCs for FD2
- FD1 WIEC houses 5 WIBs for 20 FEMBs. One WIEC per APA
- FD2 WIEC houses 6 WIBs for 24 FEMBs. One WIEC per CRP

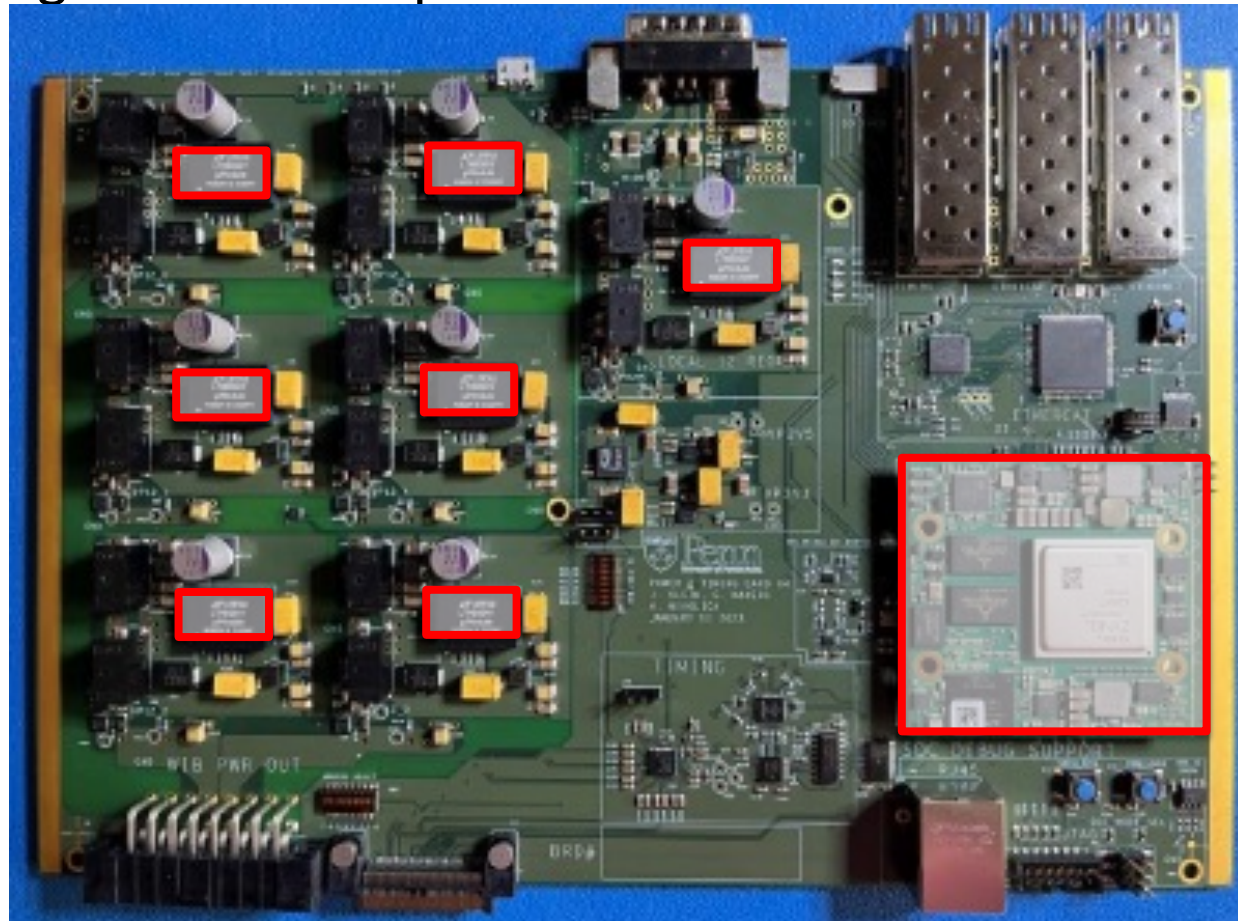


PTC Reviews

- FD1 TPC Electronics FDR ([Nov 2022](#)) and FD2 Bottom Drift Electronics FDR ([May 2023](#))
- PTC Procurement Readiness Review for PTC FPGA, DC-to-DC Converters, and voltage monitor chips also included in the FD2 FDR

For this PRR (stage-1), we are requesting to procure the rest of the PTC discrete components outside the red boxes (also 9 voltage monitor chips)

Procurement request is for FD1 and FD2



Presentations for Today

- Brief Introduction – This talk
- Adrian will cover the PTC design/validation and procurement plan
- We have done extensive PTC testing on the benchtop, system-level at CERN, CE Safety Interlock integration at ICEBERG, cooling study at elevated temperatures to simulate SURF environment, etc.
- Shekhar and Roger will cover tests at CERN and Fermilab. Adrian will summarize the BNL temperature studies in his talk

Past Review Recommendations

- Two recommendations related to PTC have already been closed
- One “for the future” is related to defining the requirement between PTC and DUNE Detector Safety System (DDSS). Waiting for the DDSS group to be formalized
- Remaining outstanding one is from FD2-VD BDE Final Design Review:
“When the CRP test is validated, order the PTC long lead time components”