DEEP UNDERGROUND NEUTRINO EXPERIMENT

Penn
University of Pennsylvania

PTCv4A Design, Validation, and Component Procurement

PTC Procurement Readiness Review, 25 March 2024

Josh Klein, Godwin Mayers, **Adrian Nikolica**

Intro and charge questions

- See Cheng-Ju's slides for intro
- Charge questions [1]:
  - **1) Has the consortium responded appropriately to the relevant recommendations from past design reviews and are they closed?**
  - **2) Are there any further relevant reviewer comments and recommendations based on design changes implemented since the FDR?**
  - **3) Has the current design been validated sufficiently to give confidence that the components to be procured are the correct ones?**
  - **4) Is there a credible plan in place for how the components will be procured? Are the required quantities including spares well understood?**
  - **5) Is there a credible plan for how the components will be shipped, handled and stored before assembly on the PTC boards?**
  - **6) Is an effective QC plan for acceptance testing in place in order to ensure the parts received meet specifications?**

[1] https://edms.cern.ch/document/3055270/1

Intro and charge questions

- **1) Has the consortium responded appropriately to the relevant recommendations from past design reviews and are they closed?**
  - R5 [28 Nov 2022] : Update the requirements documents (WIB and PTC) and to justify all the added functionalities [2]
    - Documentation is here: https://edms.cern.ch/document/2731292/3
  - R6 [28 Nov 2022]: The firmware and software development process and timeline for both the WIB and the PTC are be documented [2]
    - Documentation is here: https://edms.cern.ch/document/2893862/1
  - R4 [18 Jun 2023]: Finalize the PTC firmware in view of a test with a CRP at CERN [3]
    - Will be addressed in this presentation
  - R5 [18 Jun 2023]: When the CRP test is validated, order the PTC long lead time components [3]
    - Will be addressed in this presentation
- **2) Are there any further relevant reviewer comments and recommendations based on design changes implemented since the FDR?**
  - Layout change based on cooling study – will be addressed in this presentation

[2] https://edms.cern.ch/document/2796062/1

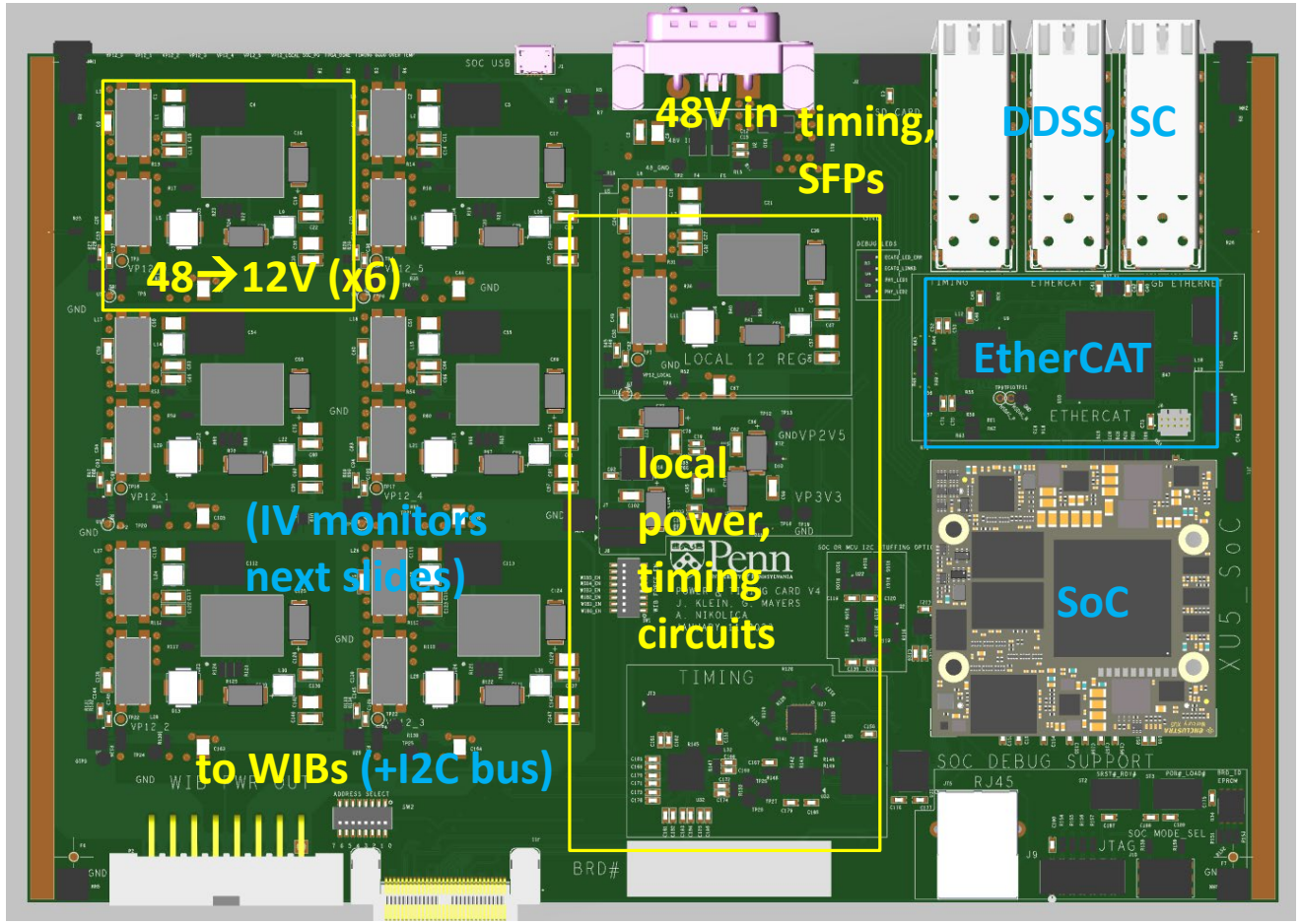
[3] https://edms.cern.ch/document/2861206/2

Design and Validation

[Charge question #3: Has the current design been validated sufficiently to give confidence that the components to be procured are the correct ones?]

PTCv4: external interfaces

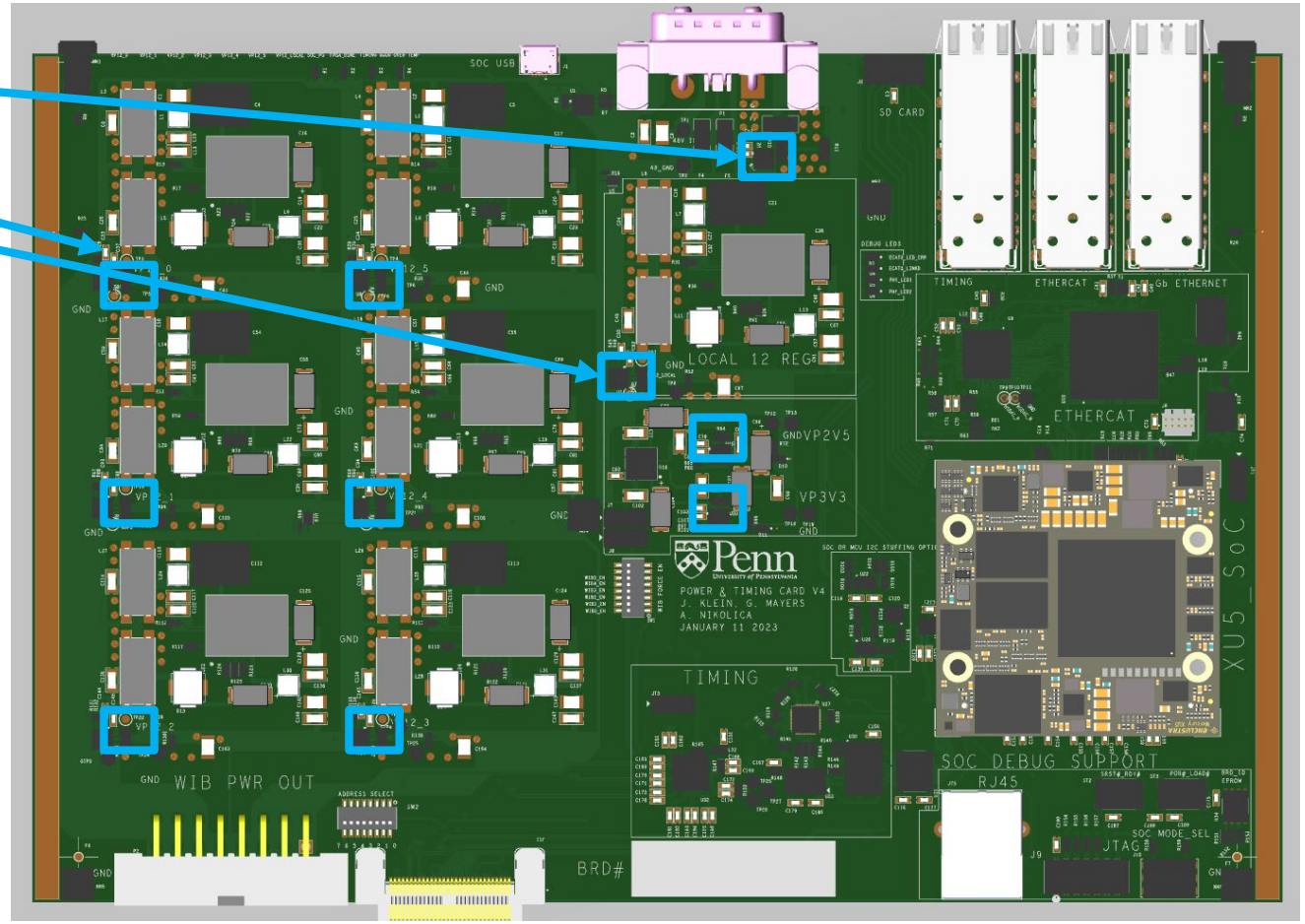
- 48V in
- Bristol timing system via 1000Base-BX SFP
- Slow Control via Ethernet over 1000Base-LX SFP
- DDSS via EtherCAT over 100Base-FX SFP
- WIB Interfaces
  - 12V out to WIB
  - Timing clock and data out to WIB
  - Timing transmit from WIB
  - I2C to/from WIB



PCB image exported from Cadence (populated)
NOTE: **BLUE** = new feature

Monitored quantities

- Voltages and currents (using LTC2945):
  - 48V input
  - All 6x WIB 12V rails
  - Local 12V (3.3V and 2.5V optional)



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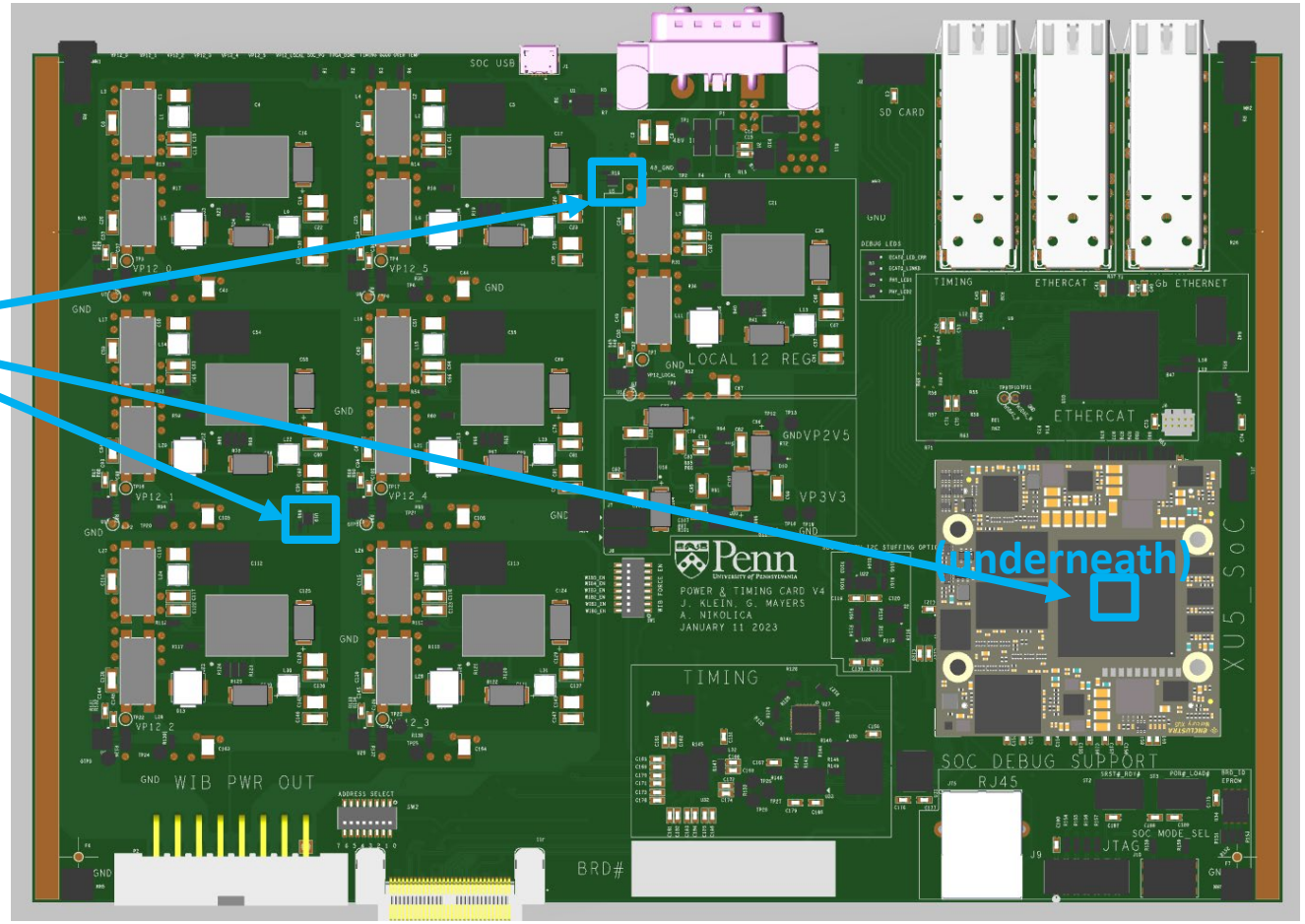
- Temperatures (using TMP117)
  - 3x locations on board
  - SoC can monitor its own FPGA internal temperature



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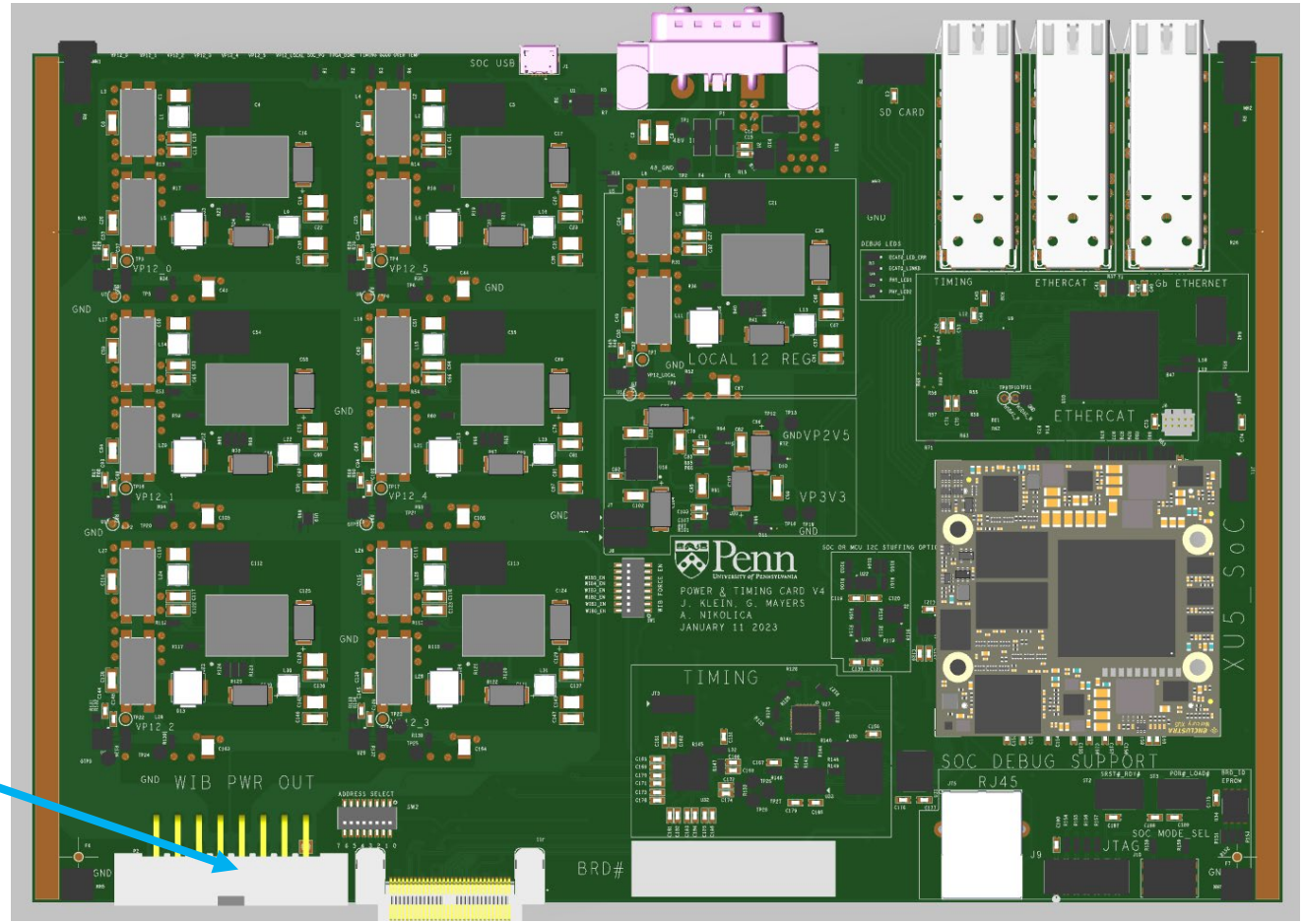
- WIB I2C



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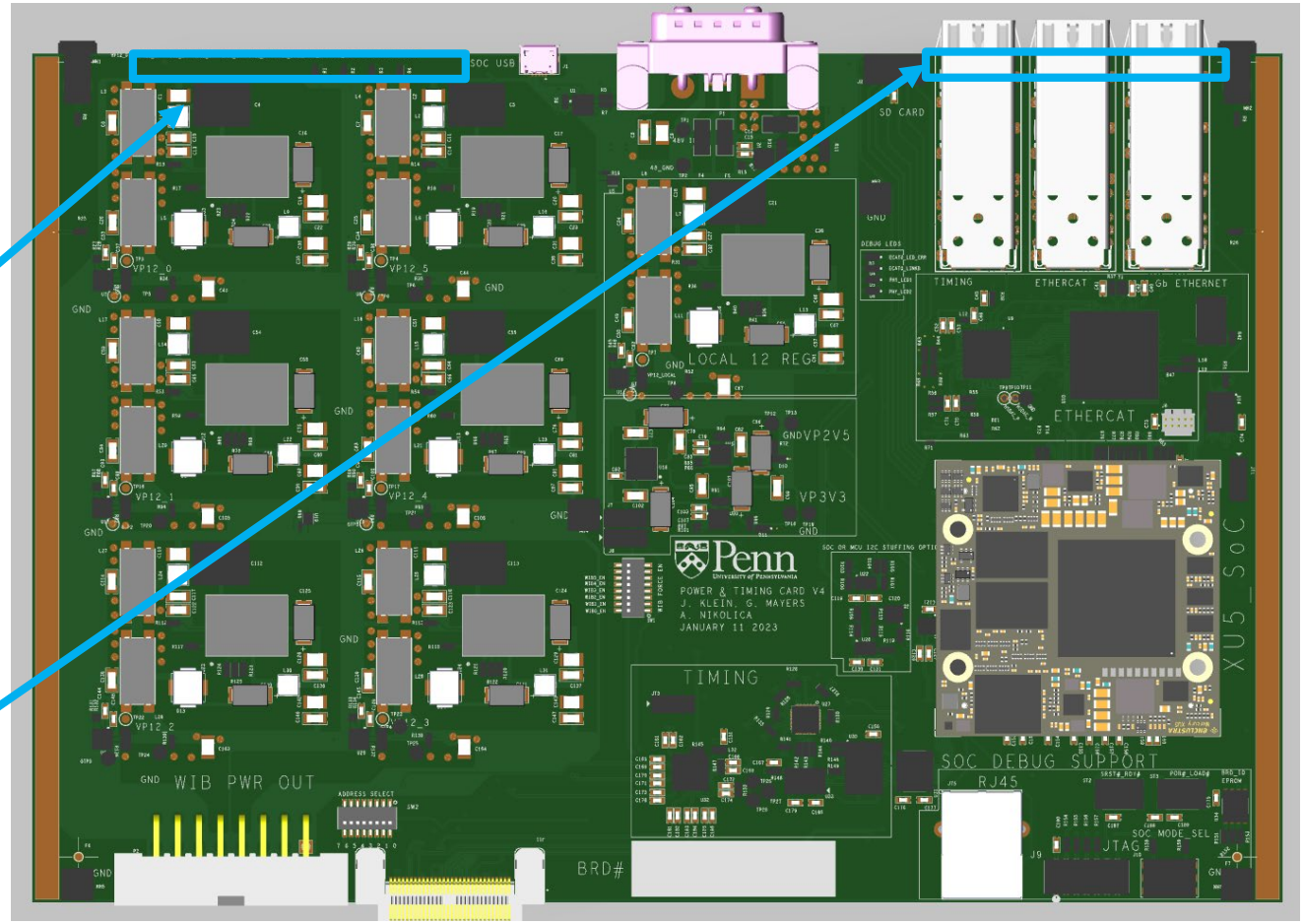
  - SoC can monitor its own FPGA internal temperature
- WIB I2C
- LEDs
  - 6x WIB power indicators
  - Over temperature (FPGA programmable)
  - SoC: power good, and FPGA done
  - Timing signal okay (decoded by FPGA)
  - SFP LEDs:
    - 3x loss of signal (LOS)
    - Timing: WIB transmit back indicator
    - DDSS: EtherCAT link active
  - (Other debug LEDs for bench only)



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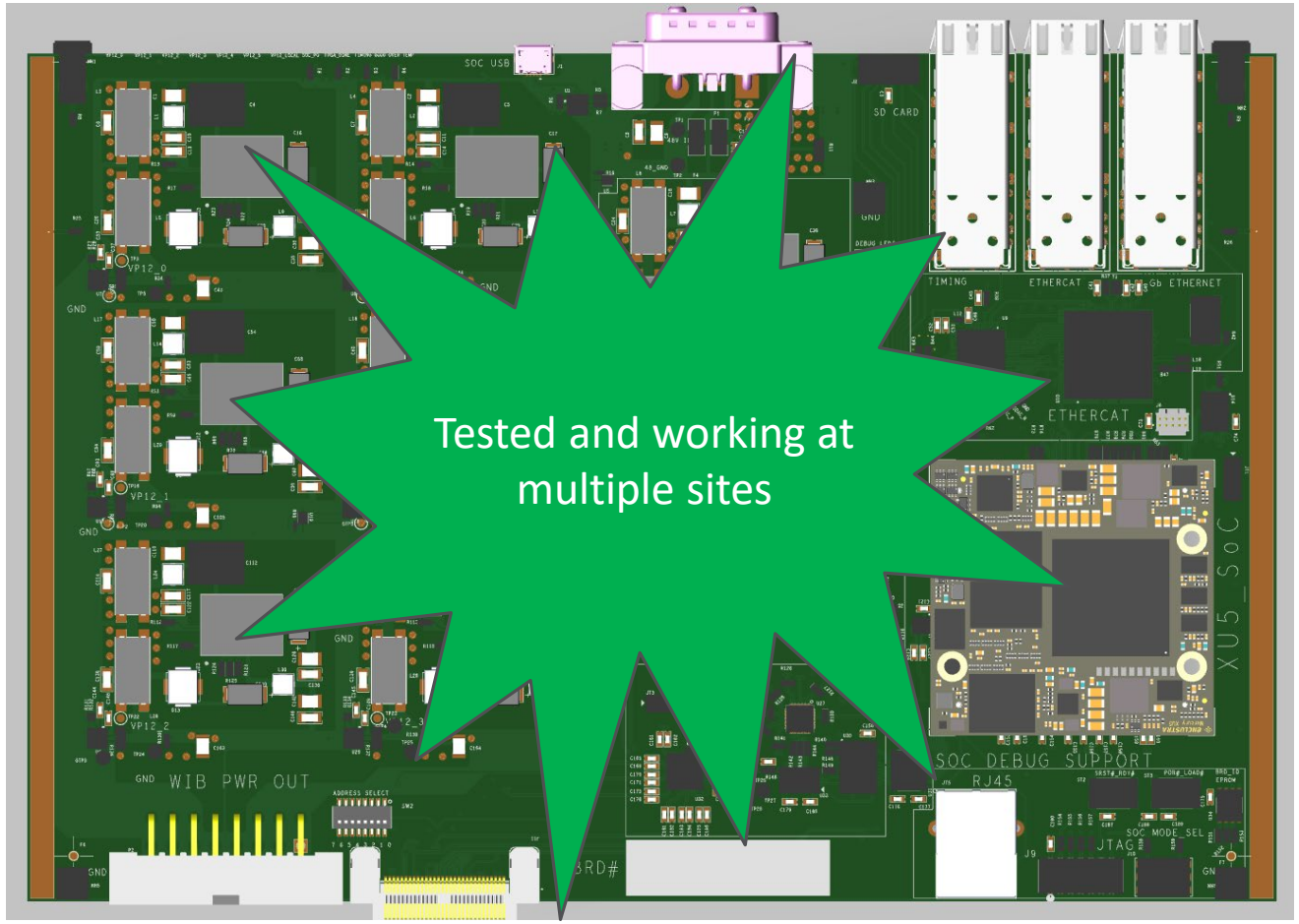
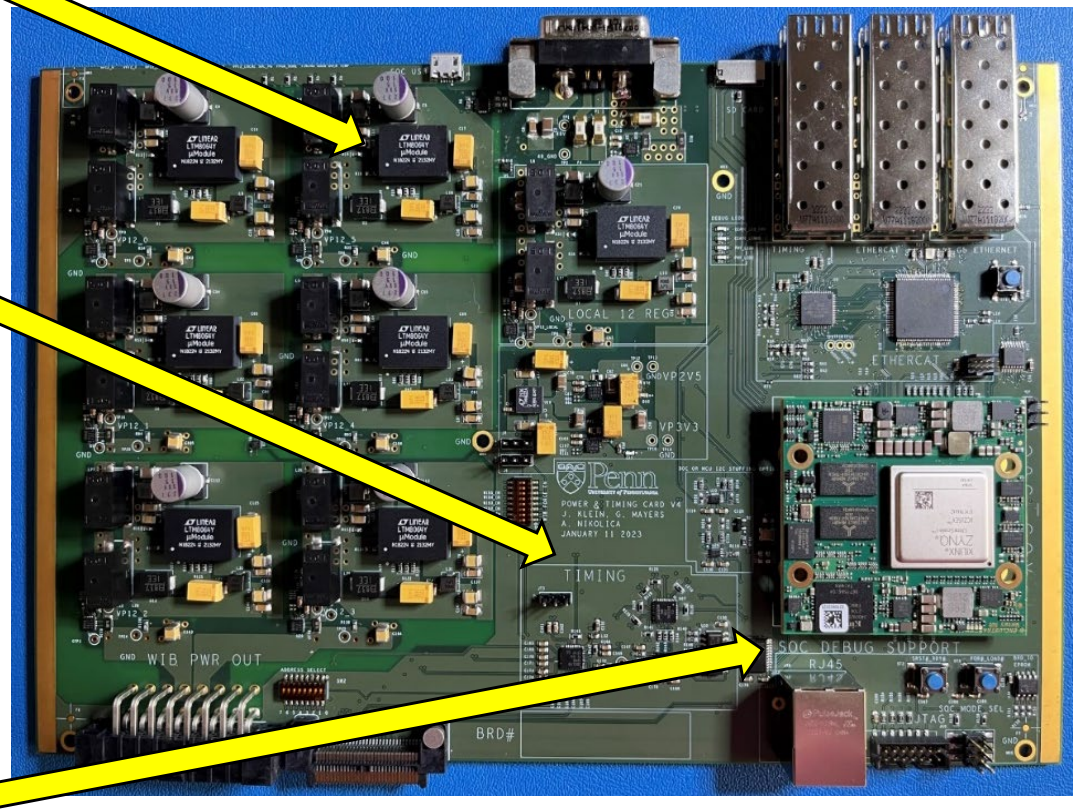


Design notes

- Power regulators
  - Use same LTCM8064 48V -> 12V DC-DC converters as PTCv3B
  - Set to 970kHz switching frequency, but have option to use SYNC to drive out of phase (not used)
  - LTM4622 DC-DC for 3.3V and 2.5V local electronics
- Timing system:
  - Timing information is only passed through in hardware (PTCv3B functionality)
  - Option to control priority encoder with FPGA to guard against hang-up on WIB
- SoC mezzanine
  - Enclustra ME-XU5-5EV-2I-D12E (prototypes)
  - Same Xilinx Zynq UltraScale+ FPGA family as WIB
  - Simple to design with, upgradeable during detector life
  - Power sequencing and control
  - GbE to SC
  - UART communications to EtherCAT microcontroller
  - I2C power monitoring (local, and WIB)
  - Minimal timing endpoint interface



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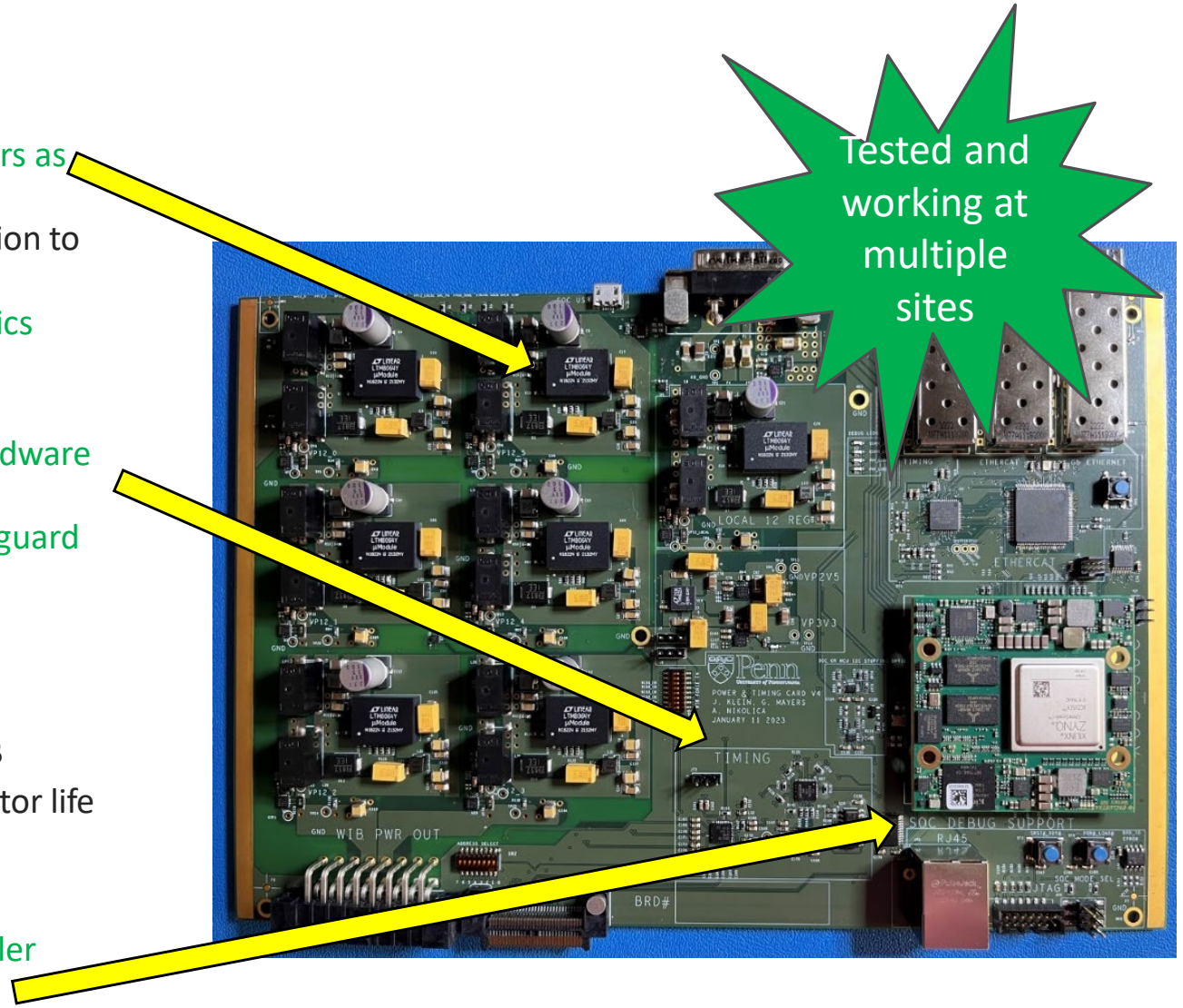
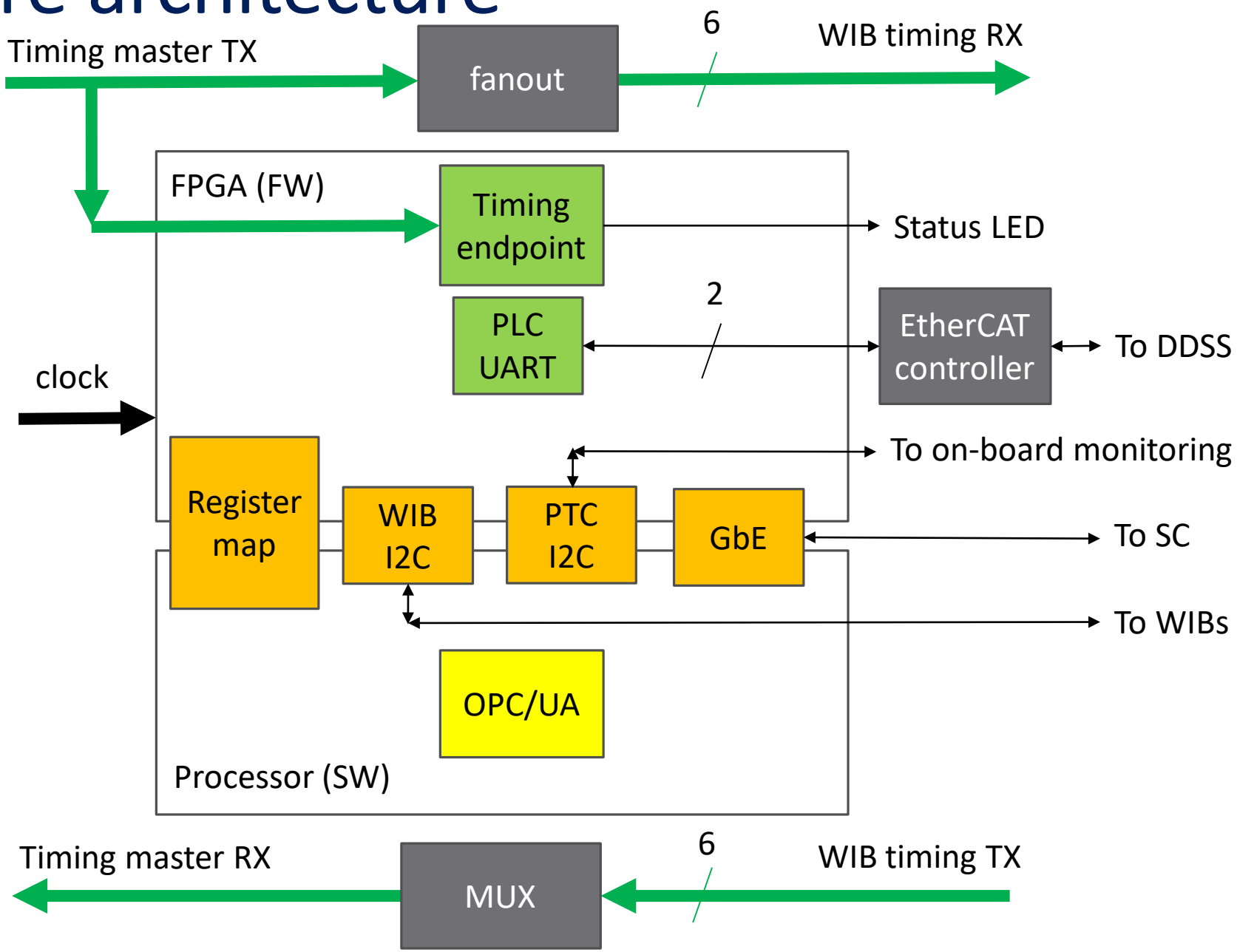
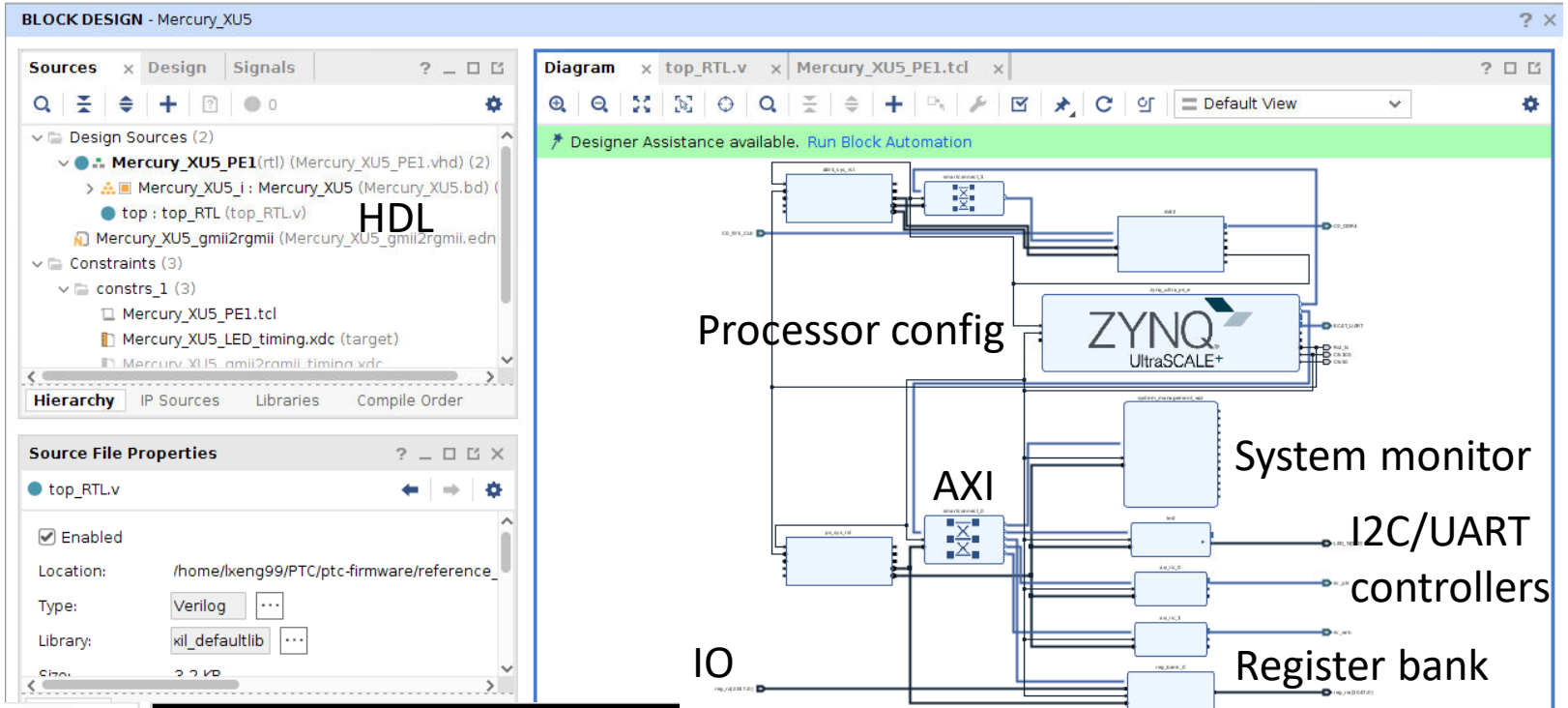


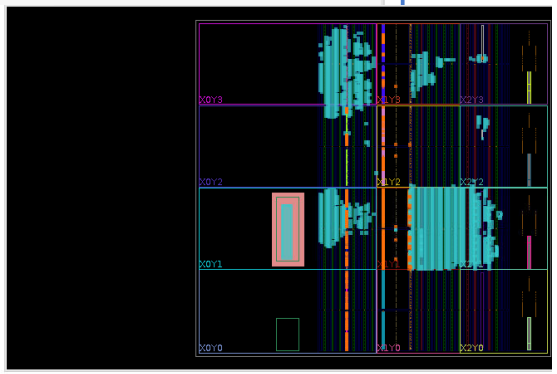
Firmware architecture

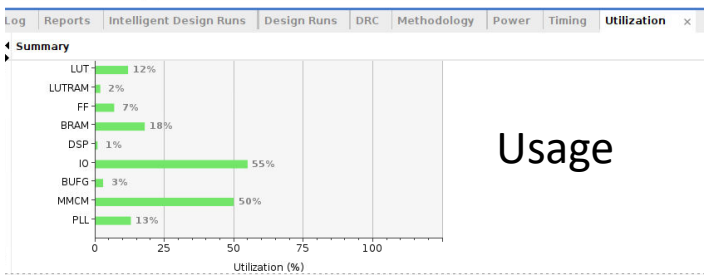


Firmware

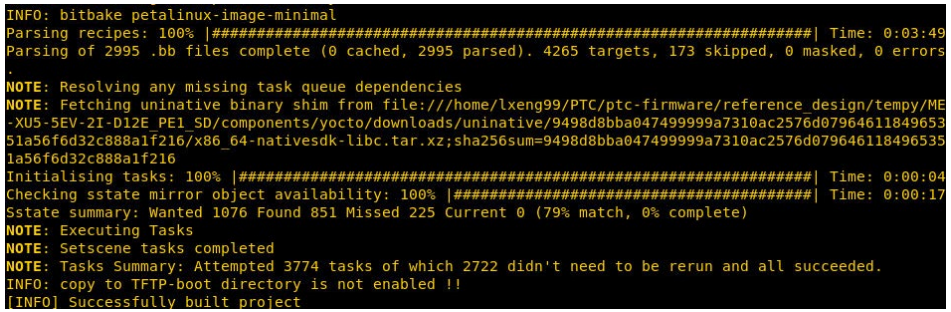
- Snapshot of Vivado project
  - Much work done in software
  - Additional custom firmware can be added in HDL files
- Firmware has been in use at all four test facilities for some time
- Expected optimizations and improvements to FW and SW will be done over time, but core functionality has been proven
- Enclustra SoM has plenty of room for expansion







Usage

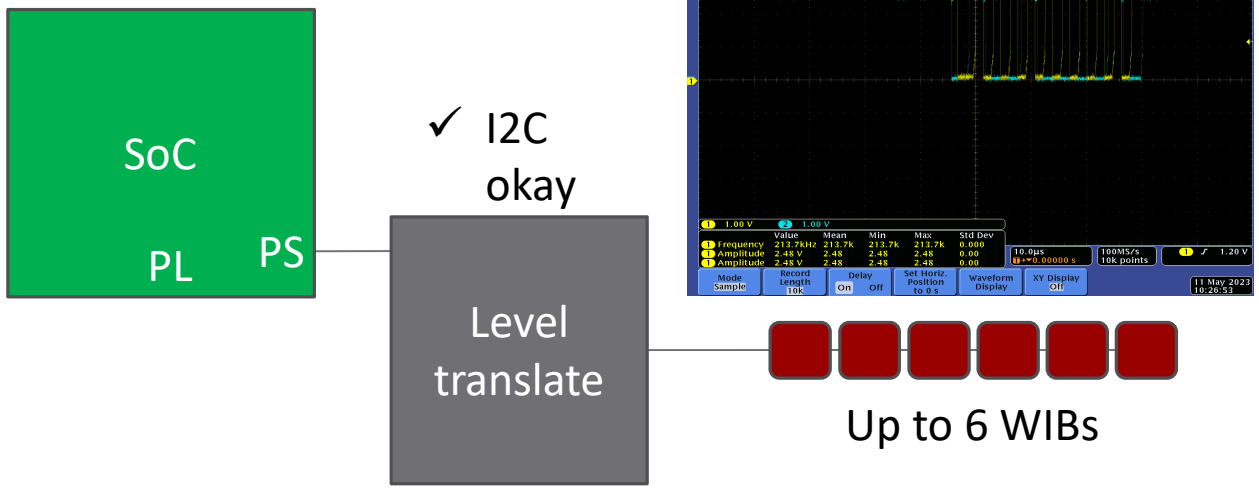


PetaLinux build environment

Tests since FDR

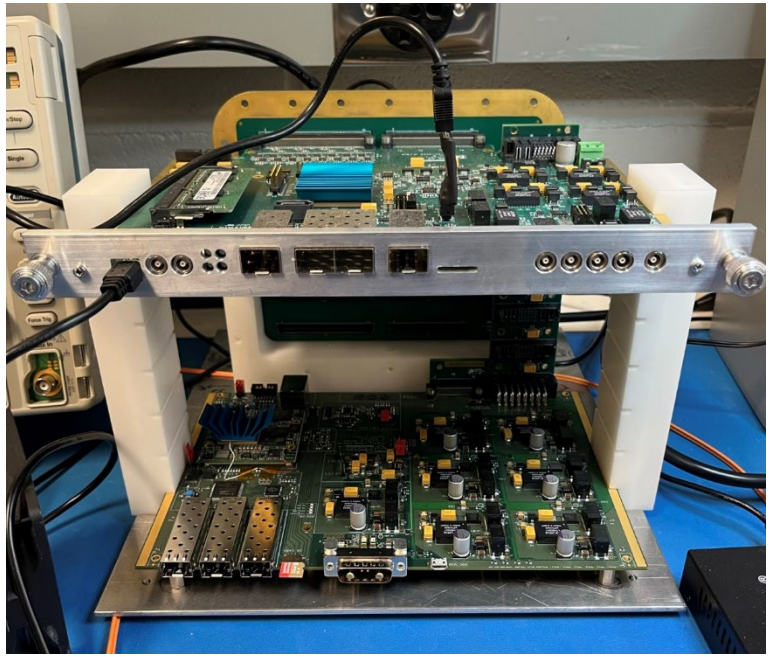
I2C tests to WIB

- I2C from Zynq PS through level translator to WIB has been tested on both WIBv3 and WIBv3A
  - WIBv3A added buffers to protect against fault conditions both on the WIB itself, and if a WIB is powered down in a WEIC. See details here:
  - https://indico.fnal.gov/event/61871/




```
root@ptc:~# i2cdetect -y -r 2
     0  1  2  3  4  5  6  7  8  9  a  b  c  d  e  f
00:                         -- -- -- -- -- -- -- --
10: -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
20: -- -- 22 23 -- -- -- -- -- -- -- -- -- -- -- --
30: -- -- -- -- -- -- -- -- -- -- -- -- -- 3d -- --
40: -- -- -- -- -- -- -- -- 48 49 4a 4b -- -- 4e --
50: -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
60: -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
70: -- -- -- -- -- -- -- --
```

Example of WIB sensor addresses being detected from the PTC Petalinux environment. Readout is via simple `i2cread` command



WIB monitored quantities

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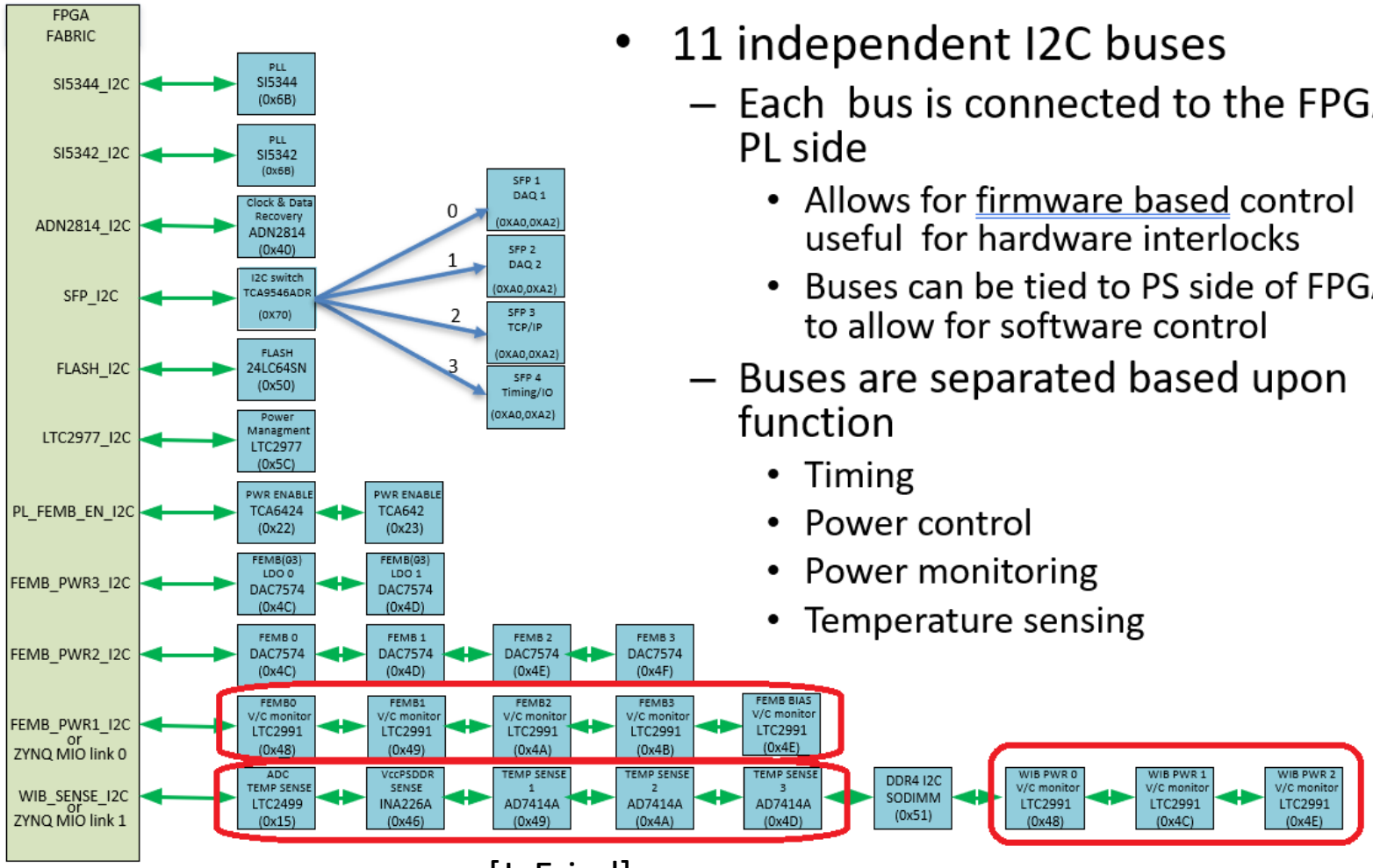
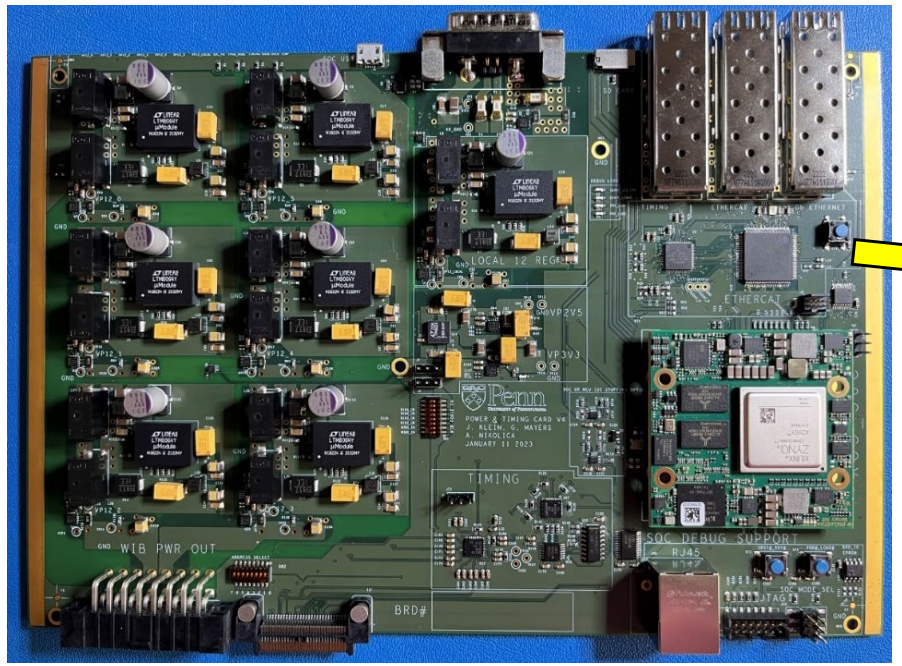
WIB I2C MAP

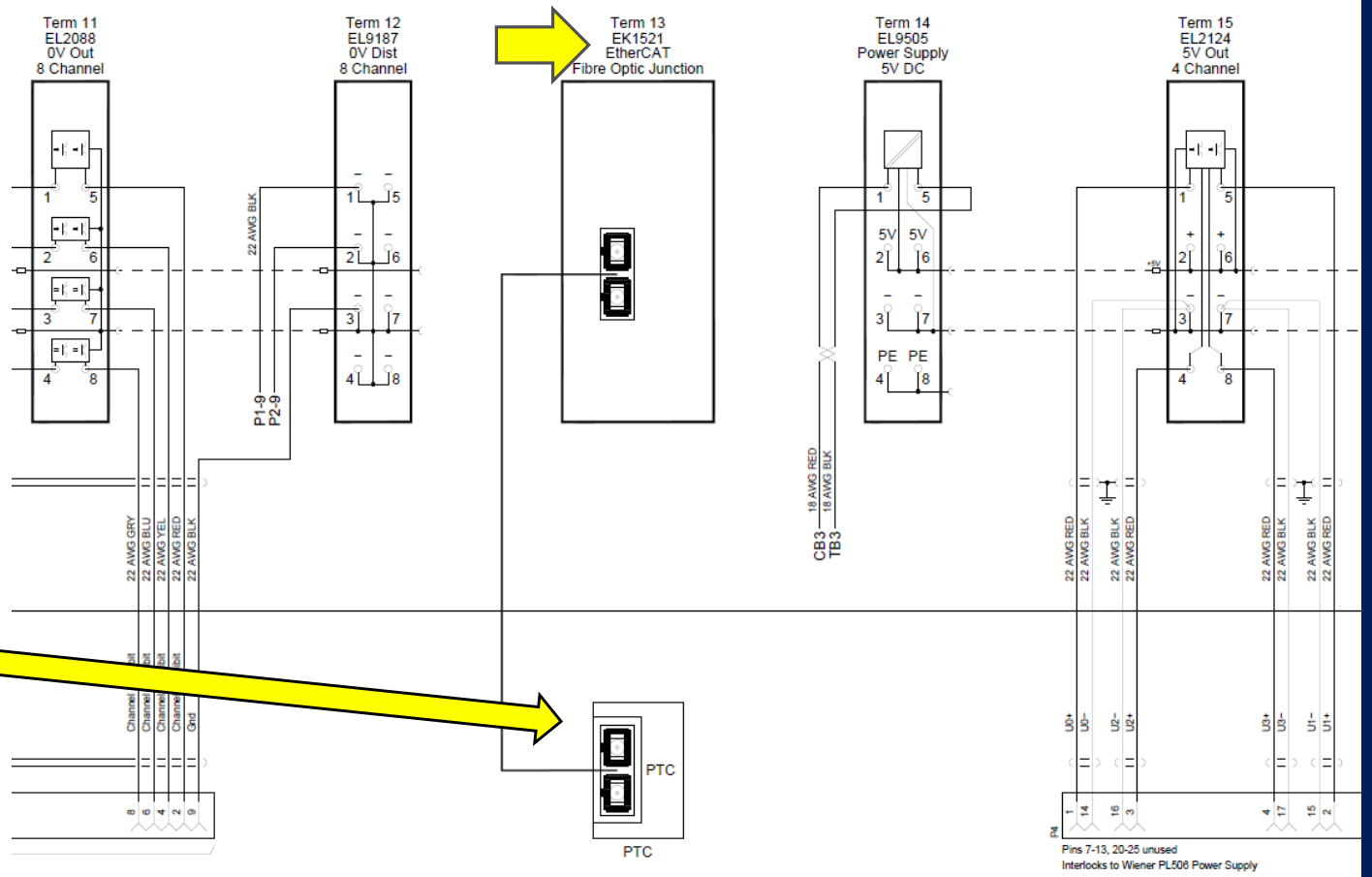


- 11 independent I2C buses
  - Each bus is connected to the FPGA PL side
    - Allows for firmware based control useful for hardware interlocks
    - Buses can be tied to PS side of FPGA to allow for software control
  - Buses are separated based upon function
    - Timing
    - Power control
    - Power monitoring
    - Temperature sensing

Design: EtherCAT

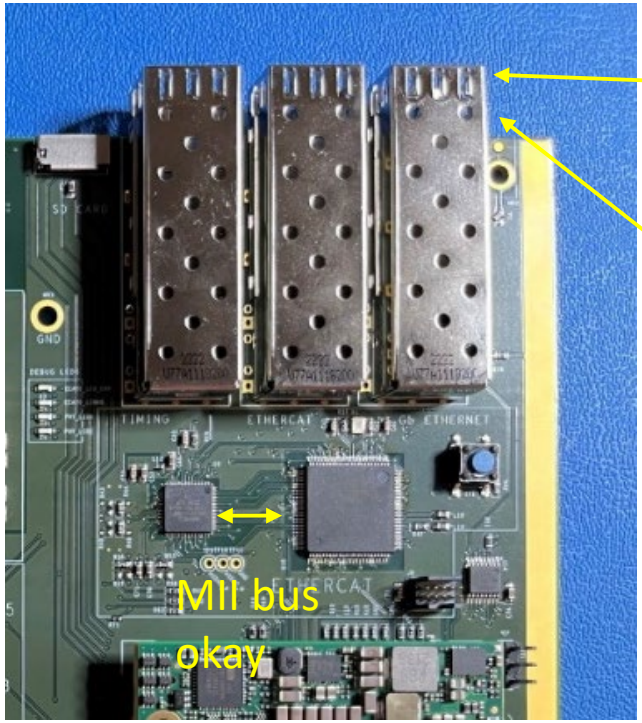
- EtherCAT interface is required for DDSS connection (already designed)
- Implemented with an Infineon XMC4300 EtherCAT-capable microcontroller
  - Beckhoff firmware solution was prohibitively expensive

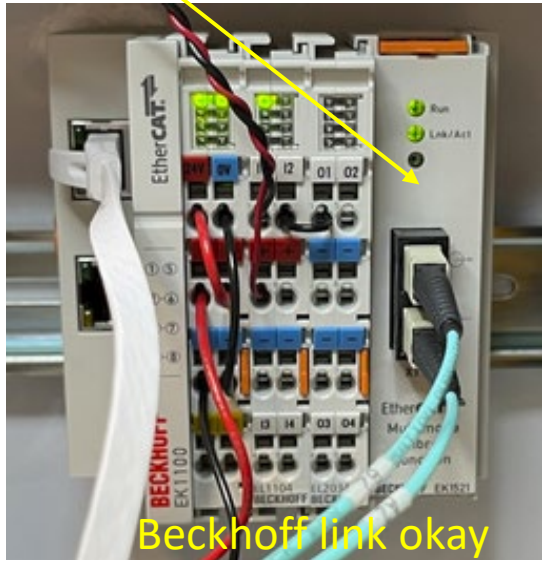




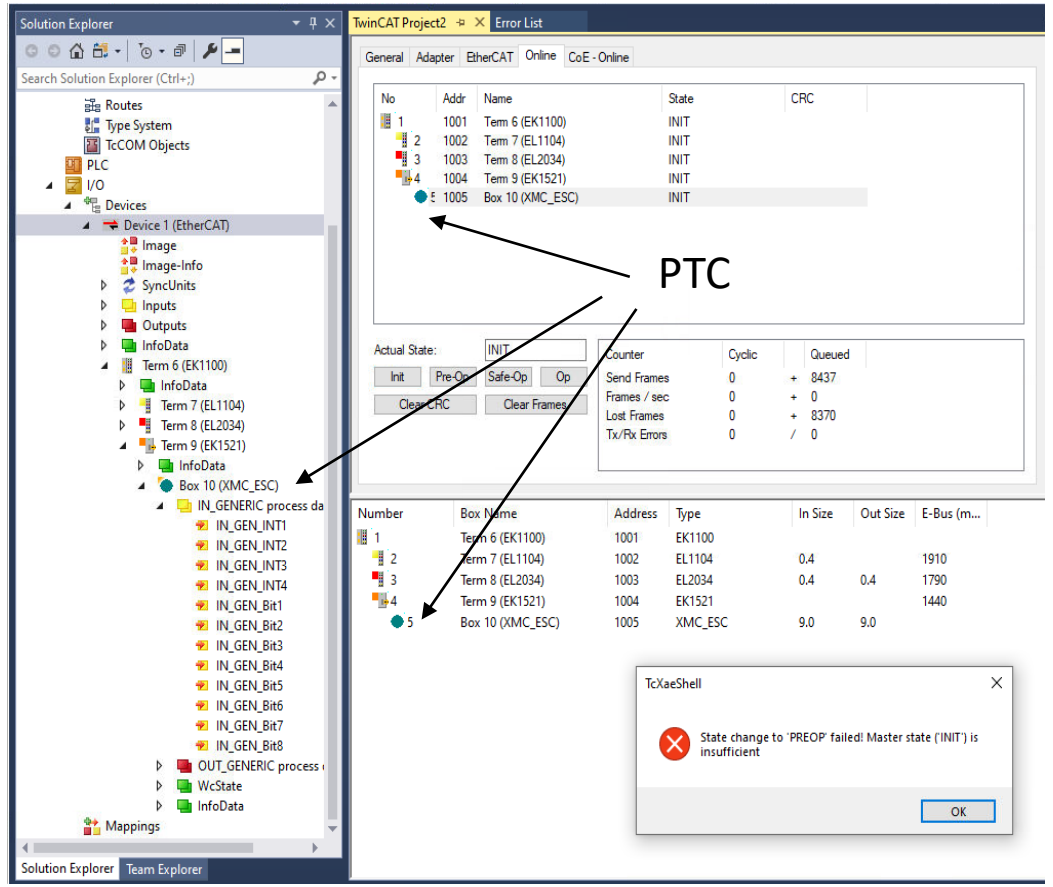
(Section of DDSS design -- link in backup slides)

EtherCAT tests

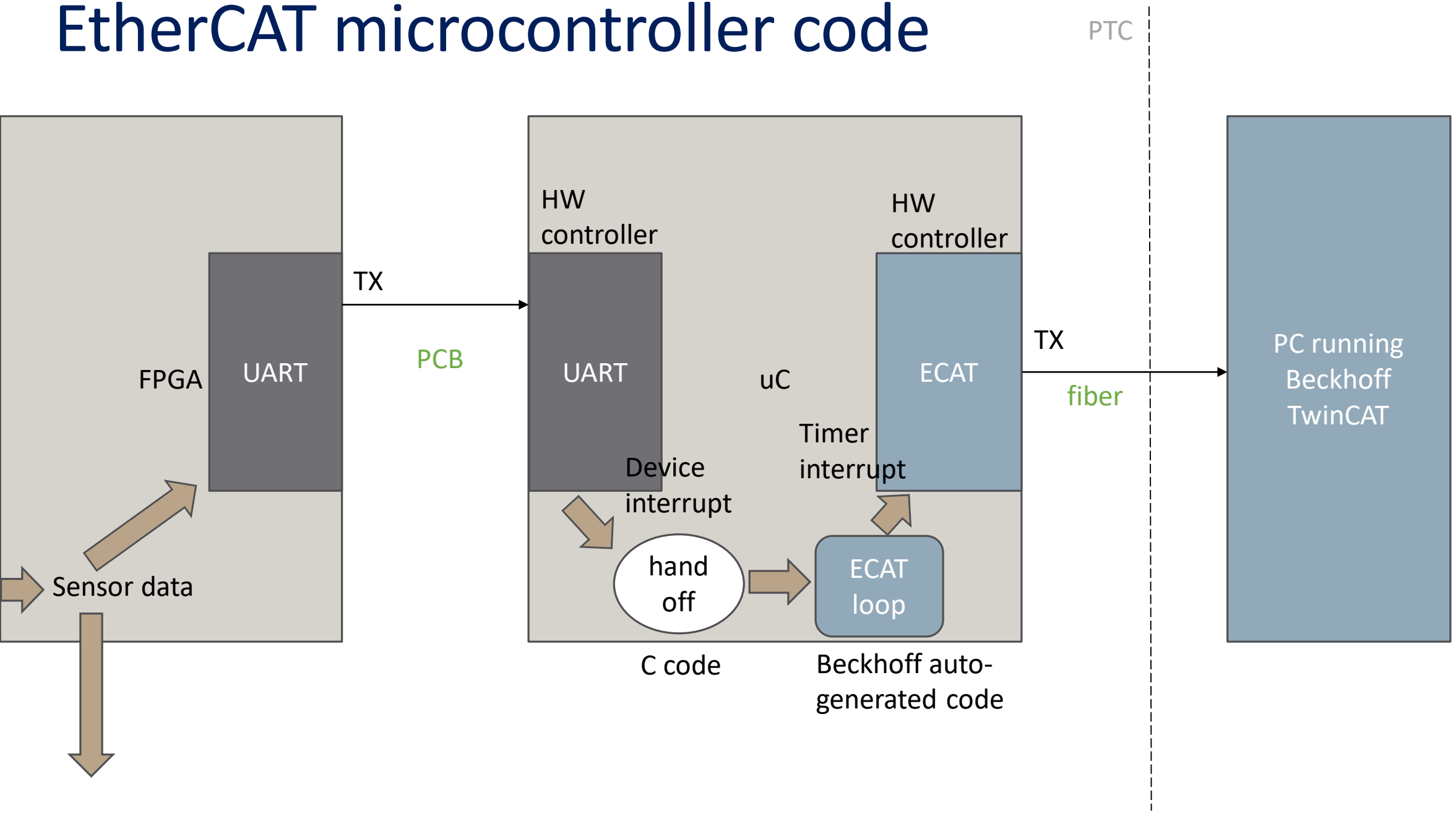


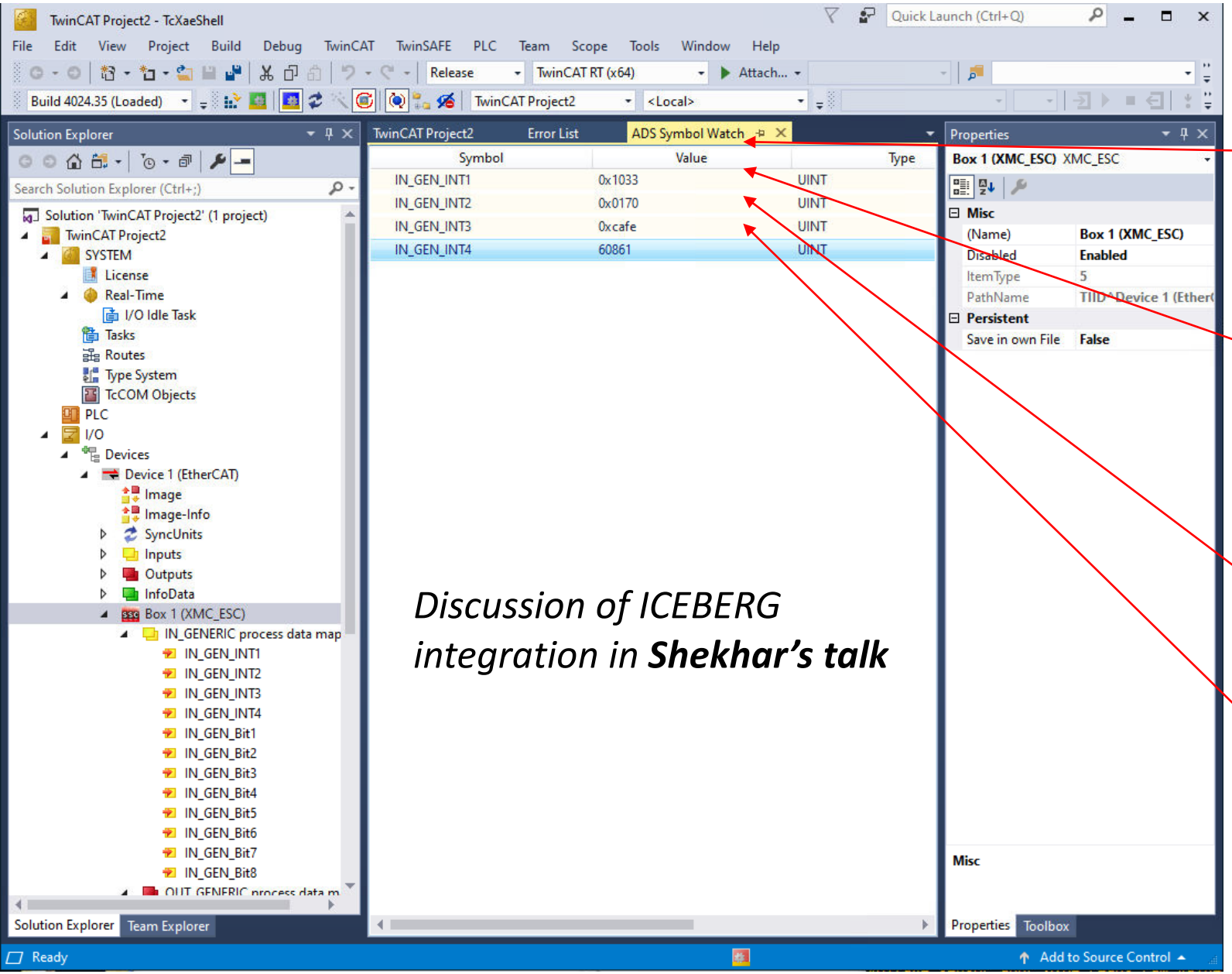


PTC being recognized in TwinCAT



EtherCAT microcontroller code





*Discussion of ICEBERG integration in **Shekhar's talk***

0x1033 raw ADC value from TMP117 temp sensor
0x1033 = 4147
4147 * 7.285 mC =
30.2C

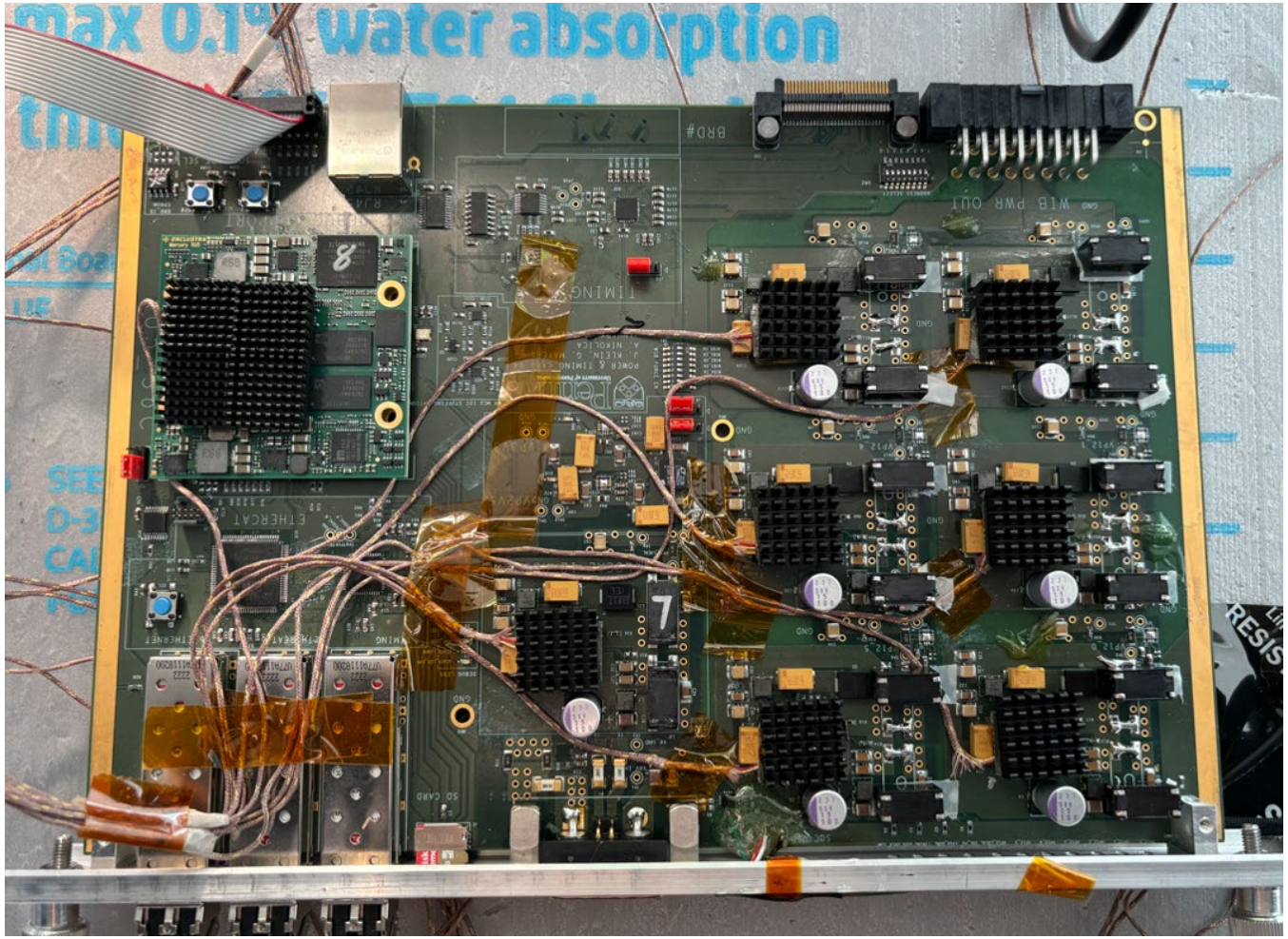
0x0170 raw ADC value from LTC2945 power monitor
((0x170)>>4) = 23
(23 * 25uV)/2.5mOhm =
230mA

0xcafe is an alignment word

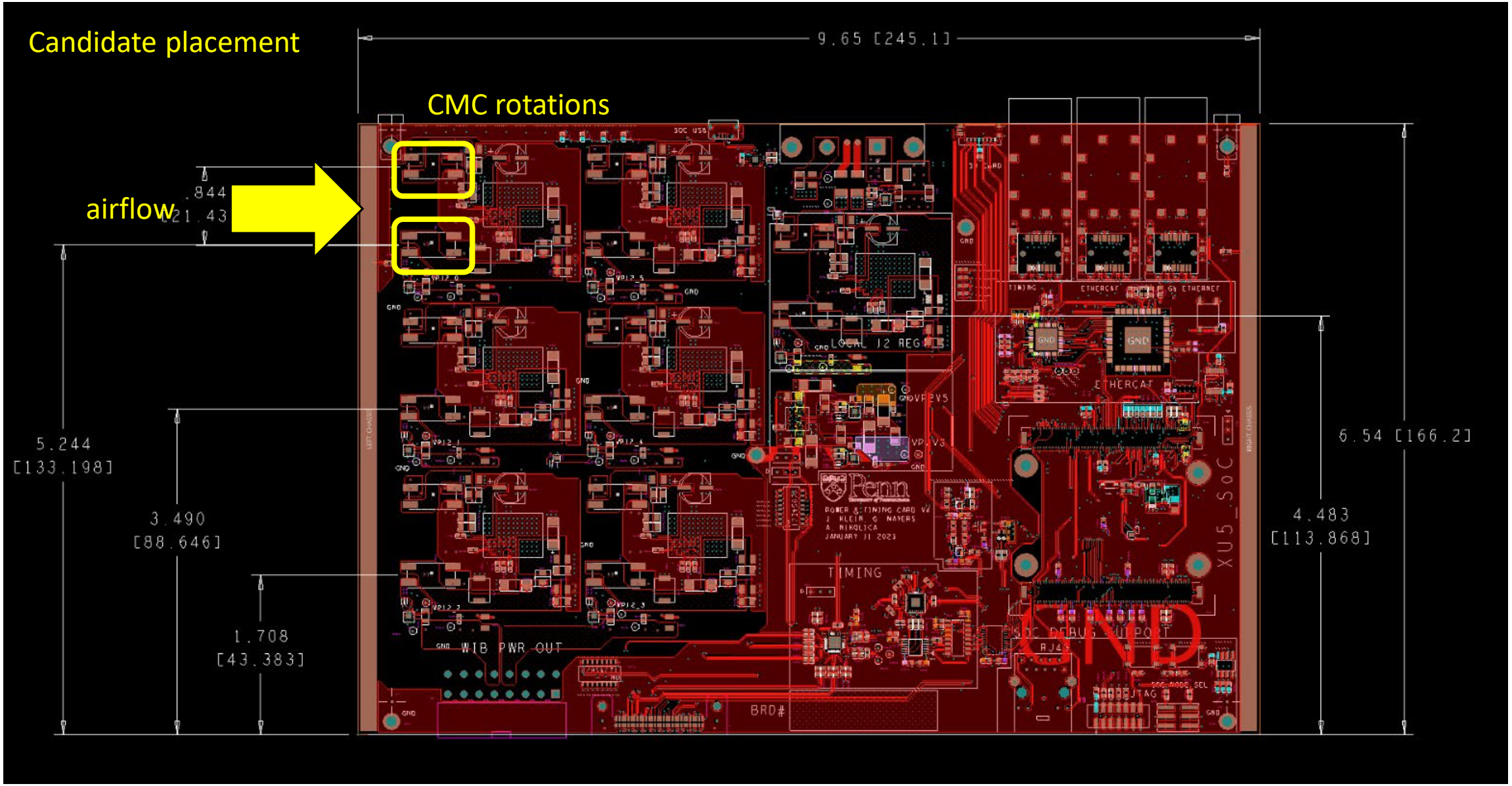
This is a sequence number that goes 0-65535, one increment per group of sensor reads, and then rolls over

Cooling

- Key concern:
  - LTM8064 should be temperature derated. At 5A max WIB current, we should keep device below 60C even though max die temp is 125C (info from datasheet and AD FAE)
- Many configurations tested at BNL (thanks Shanshan and Manhong)
  - 4 v. 6 fans
  - With or w/o air guides
  - With various air grates before fans
  - See details here:
  - https://indico.fnal.gov/event/62258/
  - https://indico.fnal.gov/event/60987/sessions/23926/#20240125
- Key takeaways:
  - Larger slots in WEIC for airflow + 6 fans
  - Heatsinks on DC-DC converter and FPGA
  - Rotate common mode chokes (CMC) in final layout to increase airflow to DC-DC converters

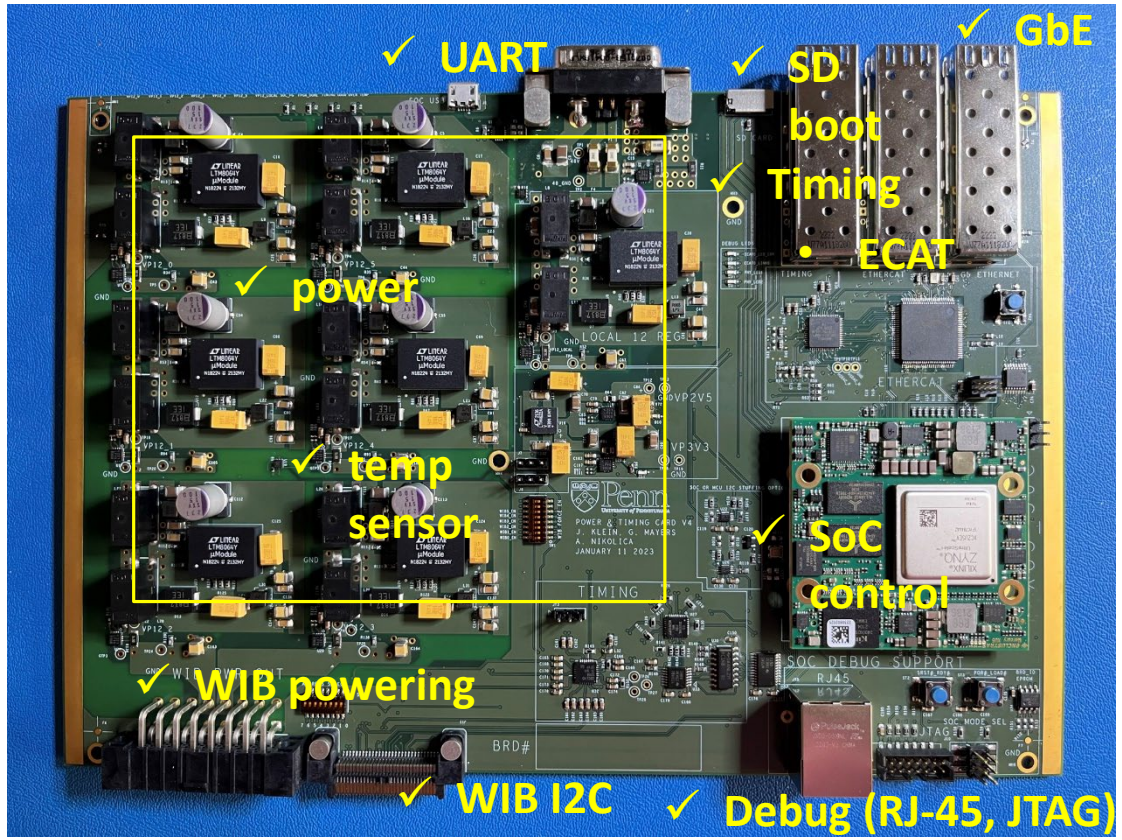


Layout change on PTC (in progress)



Testing summary

- ✓ All six 12V regulators power up, can be enabled via FPGA register bit
  - ✓ Can power multiple WIBs
- ✓ Local 12V, 3.3V, 2.5V power all ICs with no excessive current
- ✓ Enclustra Mercury XU5 mezznanine (Zynq 5EV Ultrascale+):
  - ✓ Boots via SD card
  - ✓ Front panel UART, debug RJ-45, and JTAG work
  - ✓ SFP status signals can be read in via FPGA register bits
  - ✓ Can talk to temperature sensors and power monitors
- ✓ Timing distribution test (TX and RX) work
- ✓ GbE can talk over front panel
- ✓ WIB I2C sensor reads demonstrated at BNL and Penn with WIBv3 and WIBv3A
  - ✓ Including new buffering scheme
- ✓ EtherCAT – two representative sensor reads demonstrated at FNAL and Penn
  - Remainder of sensor read implementation is largely microcontroller code



*Discussion of noise in CERN setup in **Roger's talk***

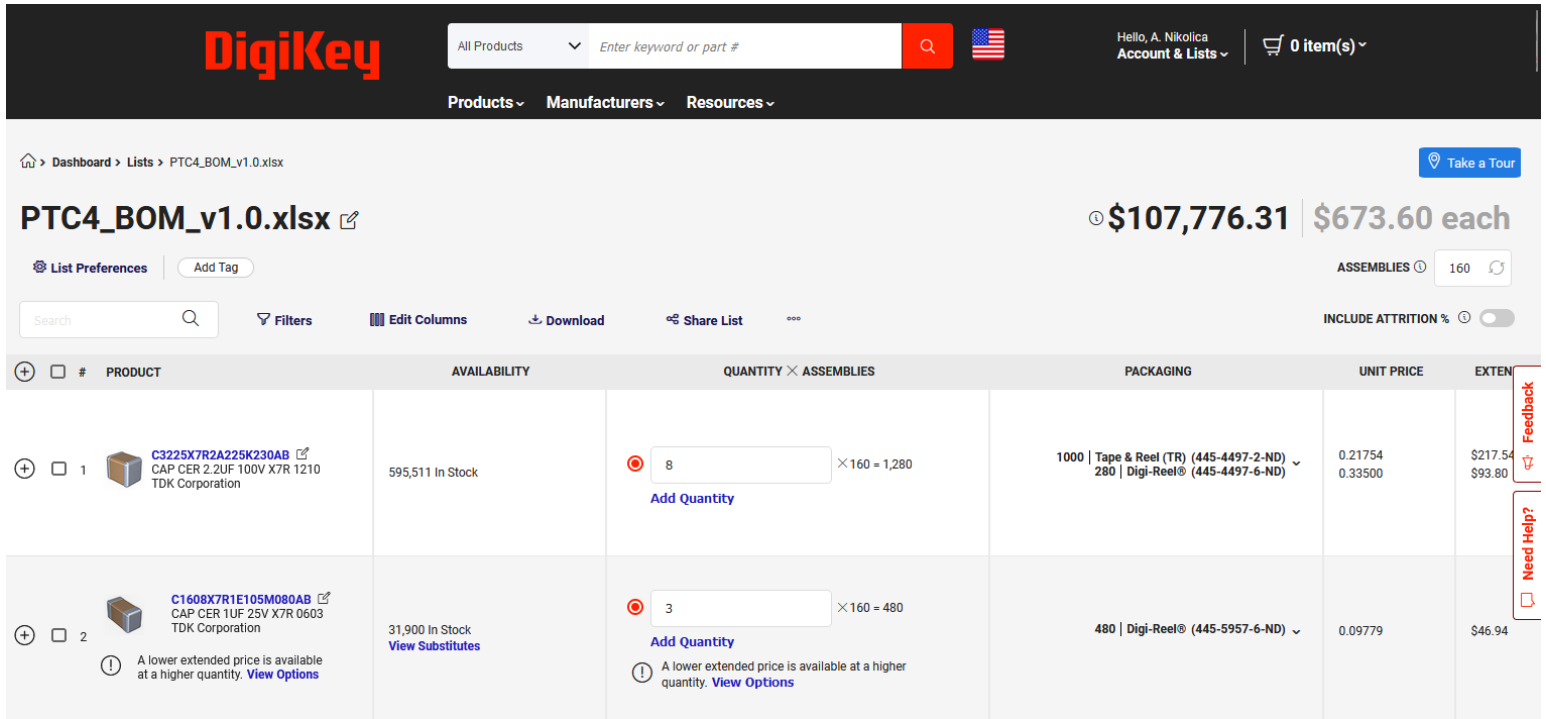
Component Procurement

Component procurement

- Three long lead time components already ordered:
  - Analog Devices **LTM8064 DC-DC converters**: 1120 components at Penn (160 PTC)
  - Analog Devices **LTC2945 power monitor**: 1694 components at Penn (160 PTC + ~10%)
  - Enclustra **Mercury XU5 (5EV variant) System-on-Module (SoM)**: 30 pieces at Penn, 145 pieces scheduled for July 2024 (for total 175 PTC)
- Remainder of components:
  - *O*(30) types of SMT resistors, *O*(20) types of discrete capacitors including one electrolytic and some tantalums
  - *O*(20) ICs, oscillators
  - *O*(10) connectors
  - A few assorted diodes, inductors, DIP switches, jumpers
  - Heatsinks, SFP cages
- Cost:
  - Most of the cost is in the FPGA, and DC-DC converters
  - A few large caps, inductors, connectors, and the microcontroller are the next relatively high cost items
  - All else is mostly passives that have a low cost
- Lead times
  - One critical component has a lead time of ~1 month (not a concern for our timescale)
    - **CDCLVD1208RHDT clock buffer** on order at DigiKey and Mouser
  - Not concerned with passives (SMT resistors and capacitors), as these are commodity components
    - Some SMT caps have lead times into July, but have many possible replacement parts

Distributors and stock

- DigiKey makes it easy to import BOM and check stock
- Connectors will likely be purchased directly through Samtec
  - Not all variants typically carried at DigiKey
- Some critical components will need to be purchased through multiple vendors, or only available at one vendor:
  - 100SXV15M electrolytic capacitor – DigiKey + Mouser have enough stock as of 3/19/24
  - FX10A-168P-SV(71) – through Mouser, ~2 month lead time through DigiKey (not a concern for our timescale)



Important schematic changes that affected BOM

- Added a fuse to between 12V DC-DC and SoM connector (request from FNAL safety review)
- Heatsinks for DC-DC converters and SoM (discussed in this presentation)
- Assorted P/N mistakes from first v4 schematic were corrected
  - There was one level translator that needed a variant with open-drain capability – we tested correct version on prototype
  - There were two level translators that needed a variant without “bus hold” – we tested correct version on prototype
  - One I2C switch went end of life – we identified a pin-compatible replacement
  - The temperature sensor variant we used went end of life – there is a pin-compatible replacement

Schematic changes TODO

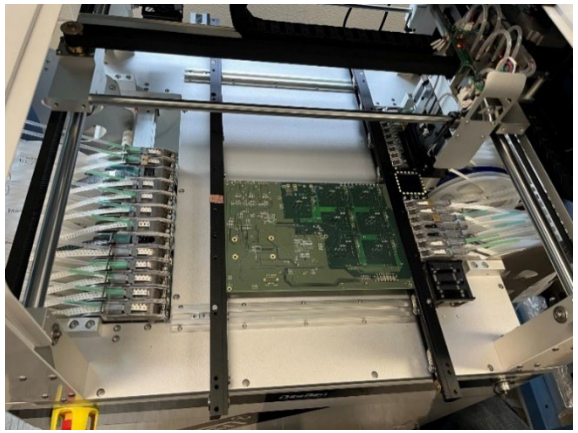
- Types of changes we are working on:
  - Stuffing options (e.g. “no not populate” resistors)
  - Signal polarity inversions (e.g. fixed function IC pins that drive LEDs)
  - Functional re-arrangements (e.g. placing a sensor on another I2C bus to mitigate address conflict)
- Other changes:
  - Minor silkscreen errors
  - Inner layer layout changes, mostly a consequence of the common mode choke rotation
  - Two minor footprint errors
- Important to note that these do NOT affect the BOM to any significant degree, meaning:
  - Quantities of minor components (resistors and single discretes) may change, but
  - NO untested components
  - NO components changes that require pinout changes (i.e. simple ICs may be substituted with pin-compatible variants based on availability)

Procurement flow summary

- [Charge question #4: Is there a credible plan in place for how the components will be procured? Are the required quantities including spares well understood?]
  - We understand the correct quantities of critical components based on the testing
  - Final schematic changes will likely result in small quantity changes of reel parts which is NOT a concern since reels are procured in such large quantities
  - We rely on DigiKey and Mouser to the first order, then individual vendors for unique components (e.g. Samtec)
  - Spares for assembly: Large components need 1 or 2 spares if at all, smaller components typically need ~5-10% depending on size (from candidate assembler)
- [Charge question #5: Is there a credible plan for how the components will be shipped, handled and stored before assembly on the PTC boards?]
  - Components are shipped directly to Penn and stored in a dedicated location with minimal personnel flow
  - No anti-static bags or vacuum seals are opened until the assembler receives them
- [Charge question #6: Is an effective QC plan for acceptance testing in place in order to ensure the parts received meet specifications?]
  - Because these are all COTS components, there are no special QC procedures for the components themselves
  - Assembler typically follows manufacturer instructions for baking components (if needed)
  - Prototypes use components from separately purchased small lots
  - All other QC is done at the PCB level, and is already covered here: https://edms.cern.ch/document/2815079/1.1

PTCv4A pre-production plan

- We will make 6 more PTCs this year
  - We have made 4 PTCv4 which were tested at Penn, CERN, BNL, and FNAL
  - The remaining 6 will be PTCv4A, which have schematic changes discussed in next slides
  - We already have components for these PTCv4As (we had originally planned to build 10 boards)
  - PTCv4A will be assembled at Penn on pick-and-place machine, as before
  - Essentially, these next 6 boards are our pre-production run
- These 6 PTCv4A will be re-tested at each site
  - Penn: functional tests
  - BNL: cooling test validation with new rotated CMC layout
  - FNAL: re-validate EtherCAT functionality with latest firmware
  - CERN: ultimate location of most prototype PTCs for NP04
  - If all tests go well, this design will be the production design
- Renew quotes with assembler -> Production



Pick-and-place setup

Summary

Summary

- PTCv4 arrived at Penn early March 2023, first board assembled in-house on pick-and-place machine
  - Design has been extensively tested
  - Old powering and timing schemes still work
  - All new interfaces tested (power/temp monitor, GbE, EtherCAT, WIB I2C)
  - Thus, we understand that all ICs and specialty components satisfy requirements
- We will need a minor board re-spin:
  - For the CMC rotation
  - And for some signal polarity reversals and a few minor connections
- FW and SW will continue to evolve towards optimized versions
- Needs for 2024:
  - 4 boards “in the wild”
  - Will need 6 boards for ProtoDUNE-II-HD or NP04 – these will be PTCv4A re-spins
  - Full detector will have: 150+10 PTCs for HD, and 80+10 PTCs for the VD
- Thank you to others who contributed significant testing or review/support: Roger Huang (LBNL), Shekhar Mishra (FNAL), Brandon Howe (FNAL), Trevor Nichols (FNAL), Jack Fried (BNL), Shanshan Gao (BNL), Manhong Zhao (BNL), Jason Farrell (BNL), Mike Reilly (Penn), Mitch Newcomer (Penn), Rick Van Berg (Penn), Nandor Dressnandt (Penn), Cheng-Ju Lin (LBNL), Dave Christian (FNAL)

Design Files

- PTCv4:
  - These design files are for the 4 boards that we have built and tested:
  - https://edms.cern.ch/document/2339398/2
- PTCv4A:
  - These are candidate files with minor schematic and BOM corrections
  - Layout files will be added once complete
  - https://edms.cern.ch/document/2339398/3