Report from STT Working Group

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SAND meeting
19 March 2024

OUTLINE

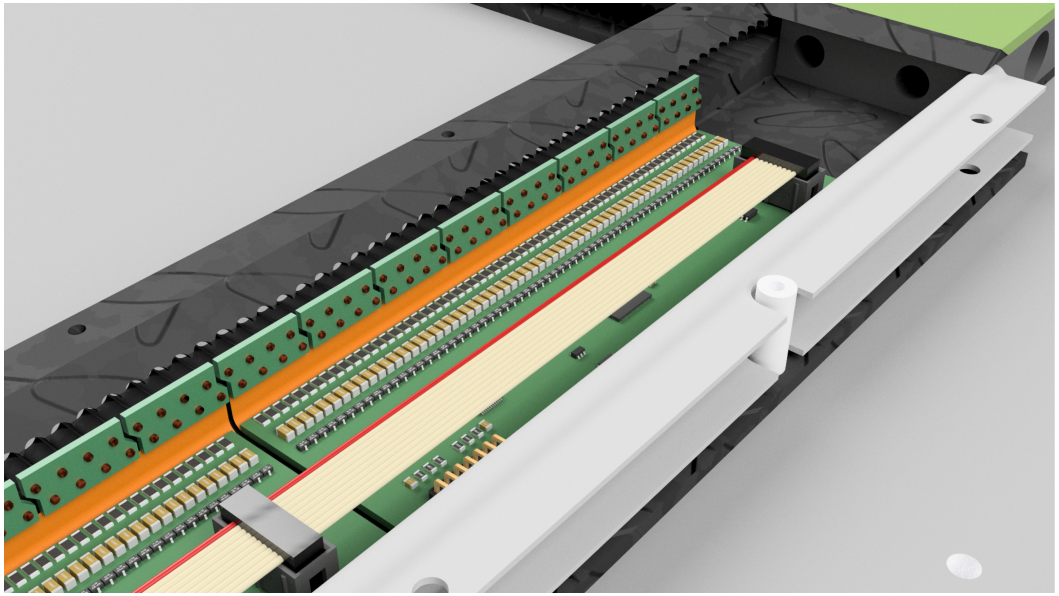
Focus on progress since January CM:

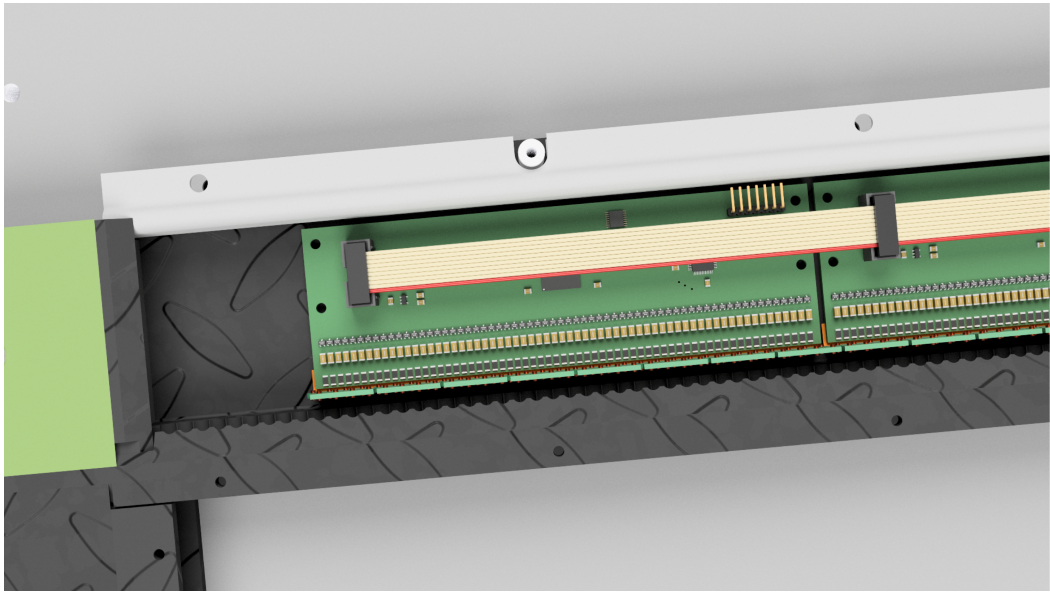
- *Demonstration of integrated STT readout boards with C-fiber prototype at CERN;*
- *Tests of the new crimping pins with mockup prototype;*
- *Tests of wire spacers with 4m straws;*
- *Thermal analysis of 4m STT module with new readout boards;*
- *Study of gas flow in full scale 4m STT modules;*
- *Connections of STT modules;*
- *Preparation for STT production at GTU.*

Material presented during WG meetings (Wednesdays, 8:00am Central Time / US) available on Indico:
`https://indico.fnal.gov/category/1402/`

INTEGRATED STT READOUT BOARDS

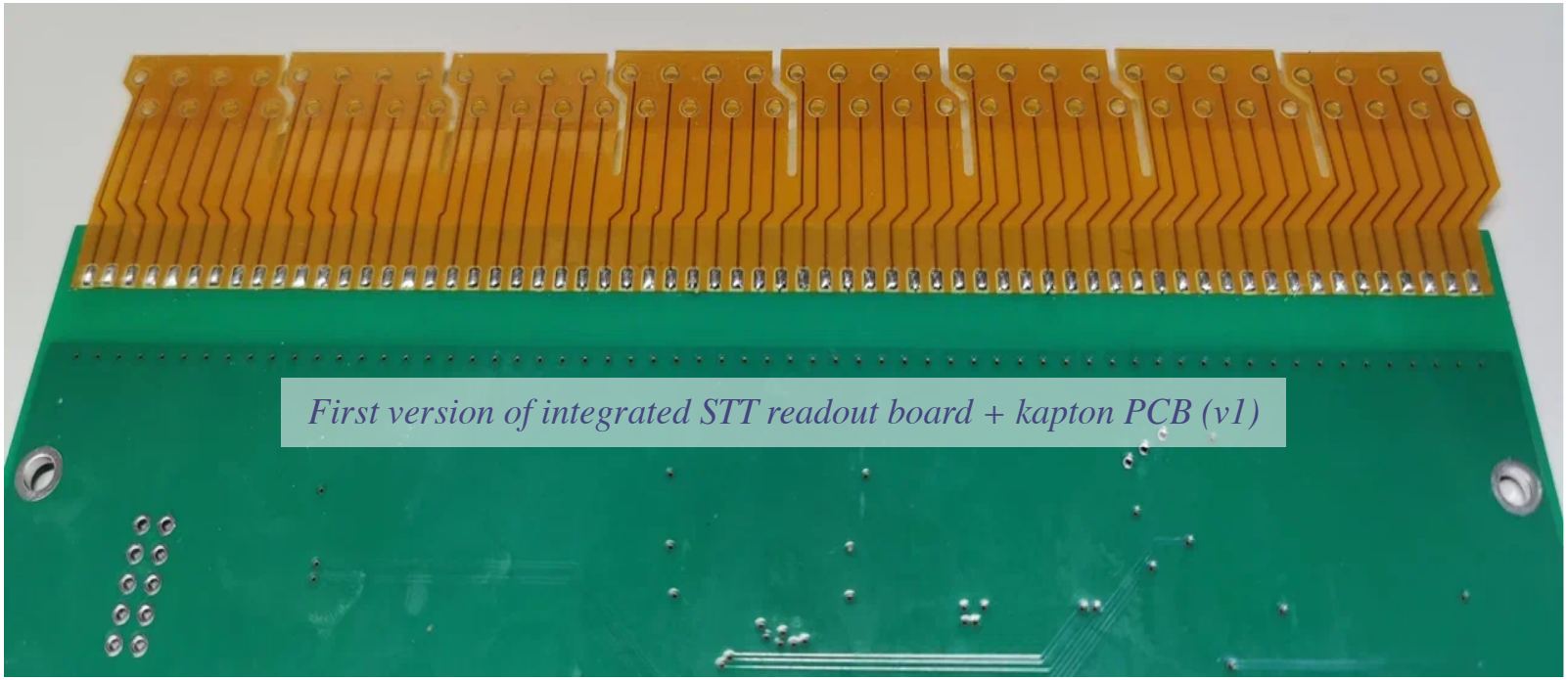
V. Bautin (JINR)



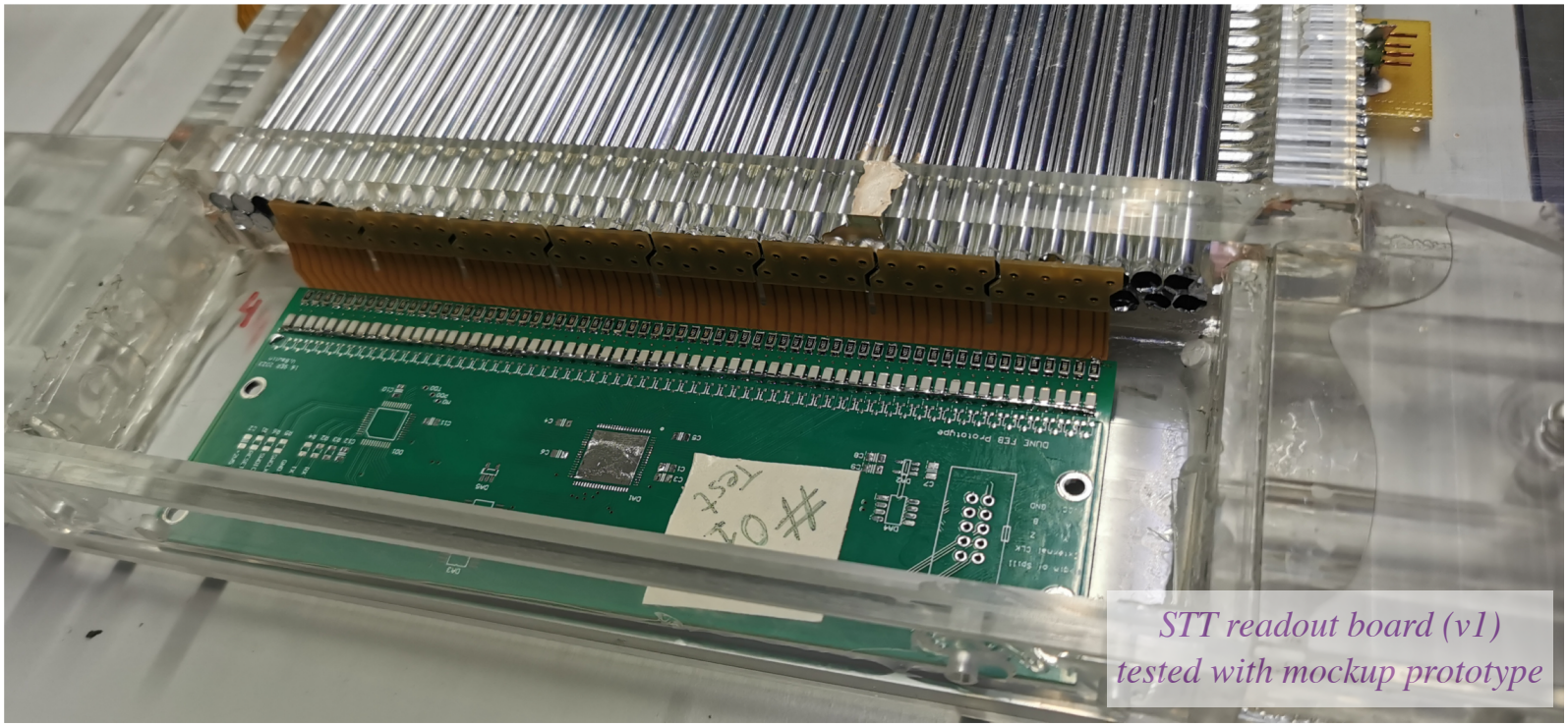


- *Small boards reading up to 64 straws each with ASIC + micro-controller (MCU);*
- *Connection with straw pins via flexible kapton PCBs;*
- *Off-the-shelf analog ASIC (G. De Geronimo) can be replaced with custom one;*
- *Low-power boards (~0.65 W each for 64 channels) minimizing signal path.*

$\Longrightarrow$ *First version (v1) successfully tested, revised version (v2) in preparation with PCIe connector*

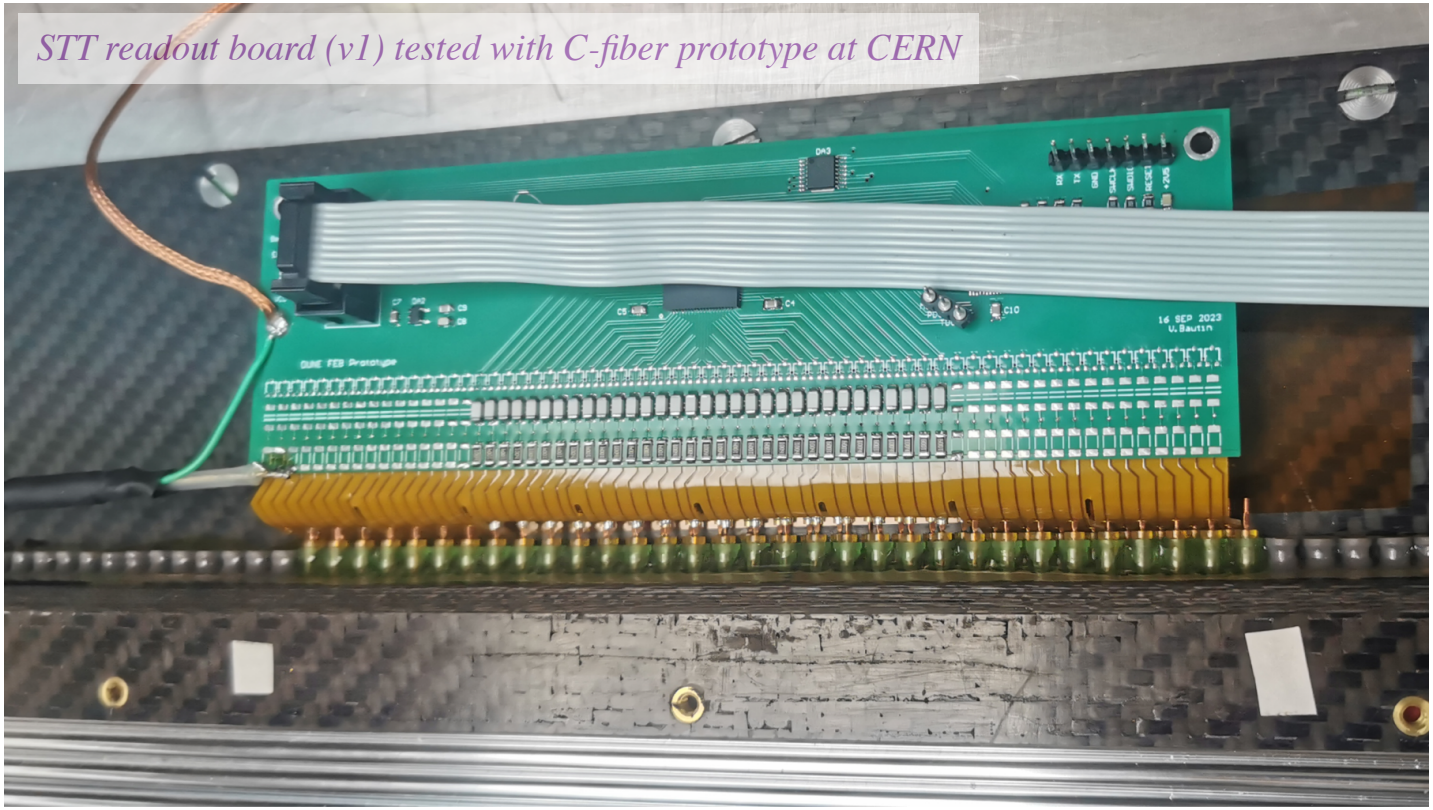


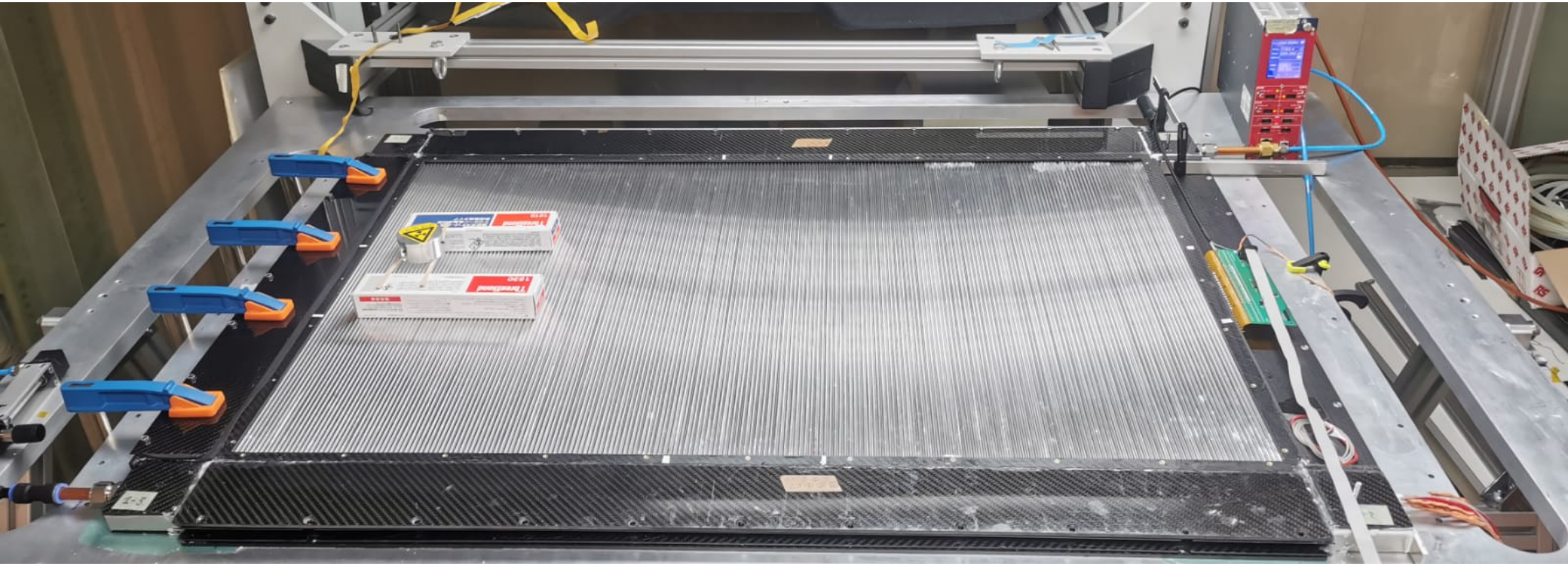
First version of integrated STT readout board + kapton PCB (v1)

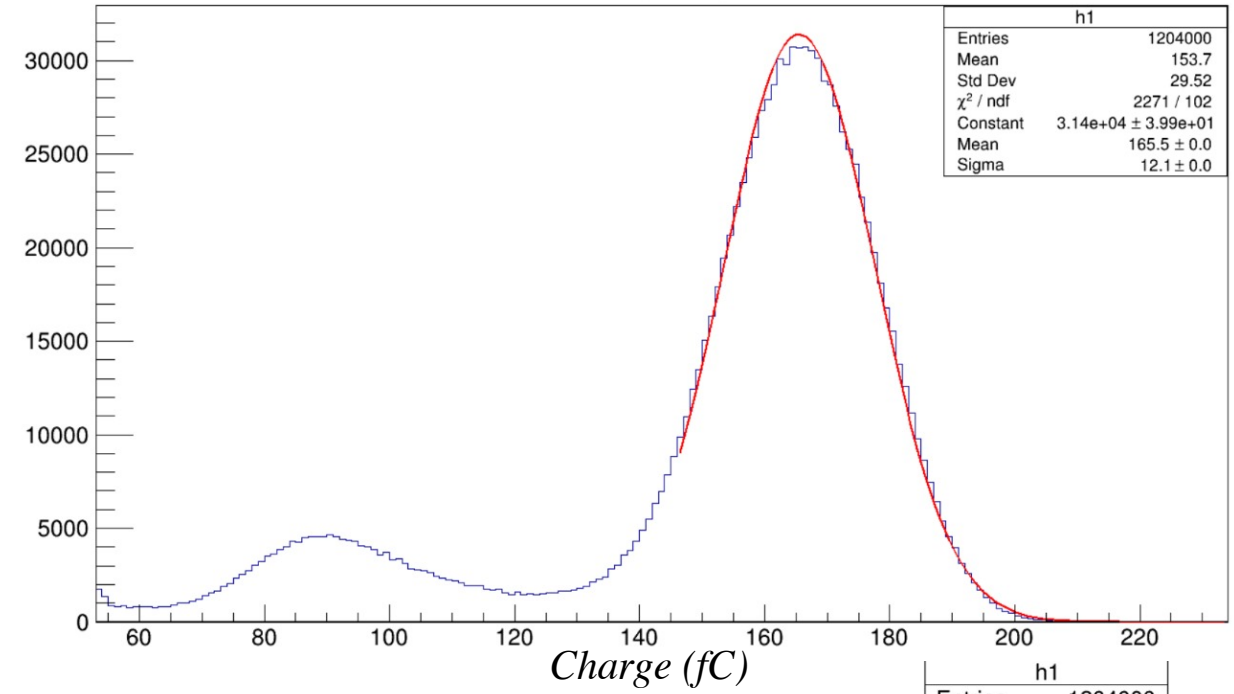


STT readout board (v1) tested with mockup prototype

STT readout board (v1) tested with C-fiber prototype at CERN



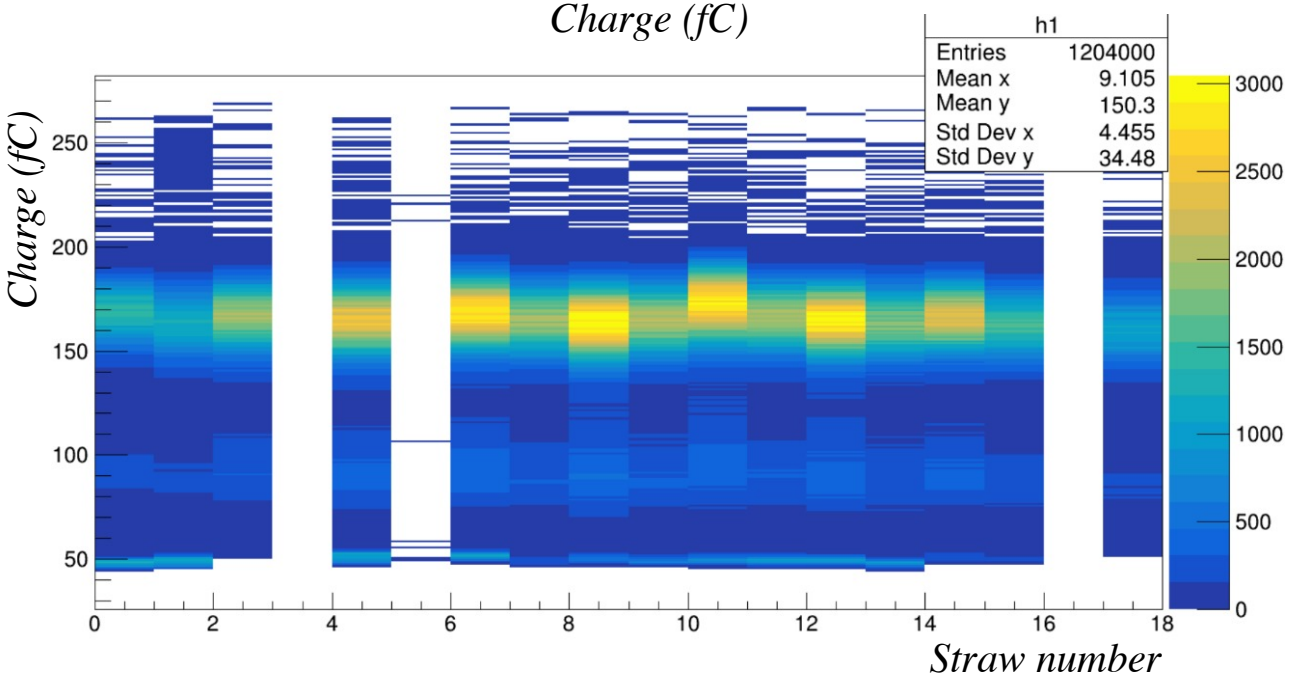




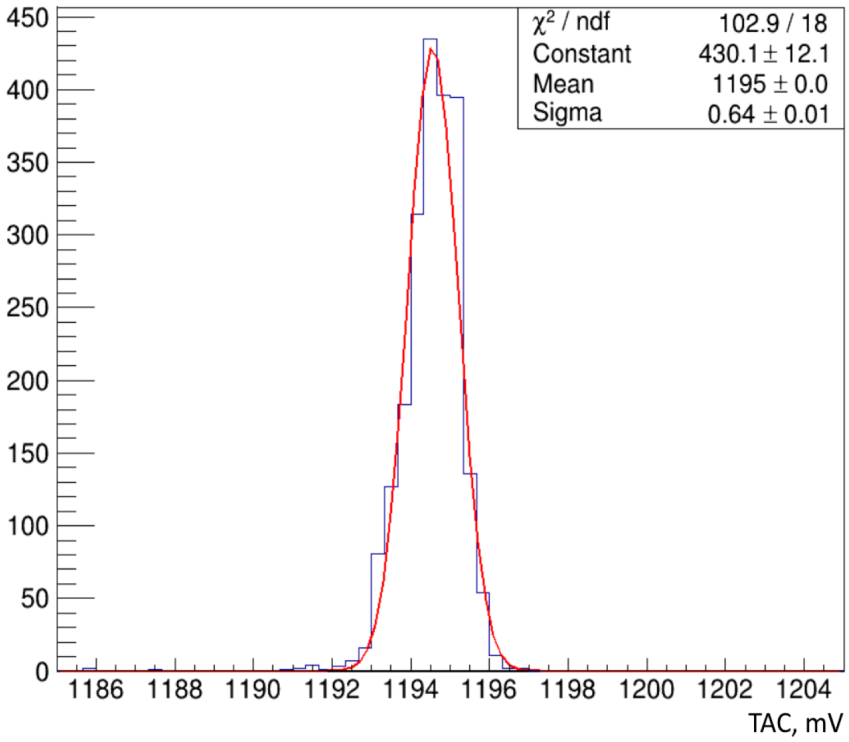
Demonstration of integrated STT readout board with STT prototype at CERN:

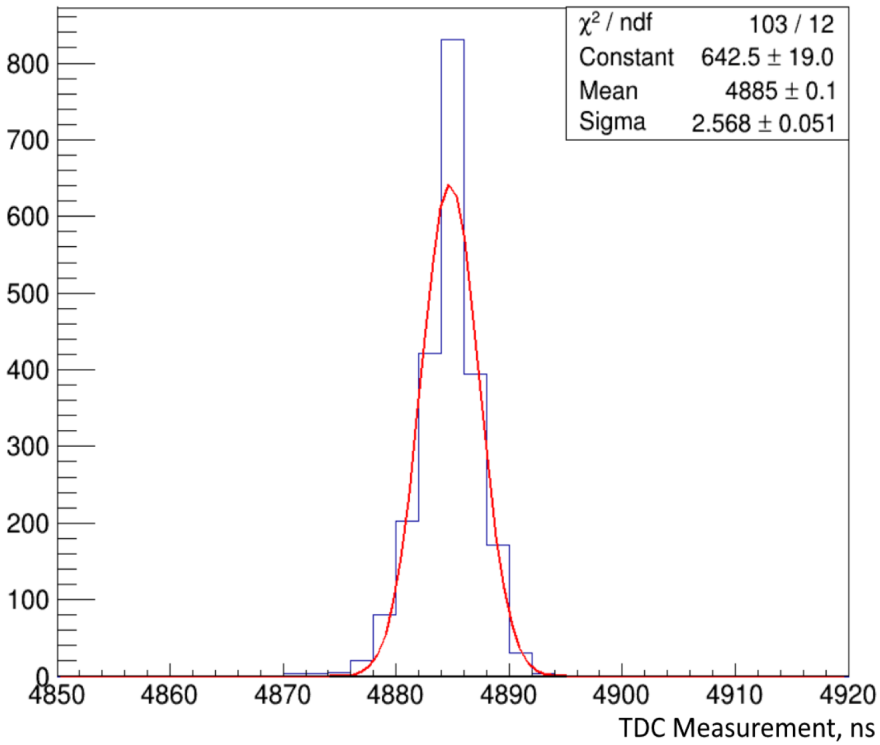
Ar/CO_2 70/30

^{55}Fe measured charge spectrum



^{55}Fe charge spectrum as a function of the straw number in the STT prototype
(3 dead ASIC channels)

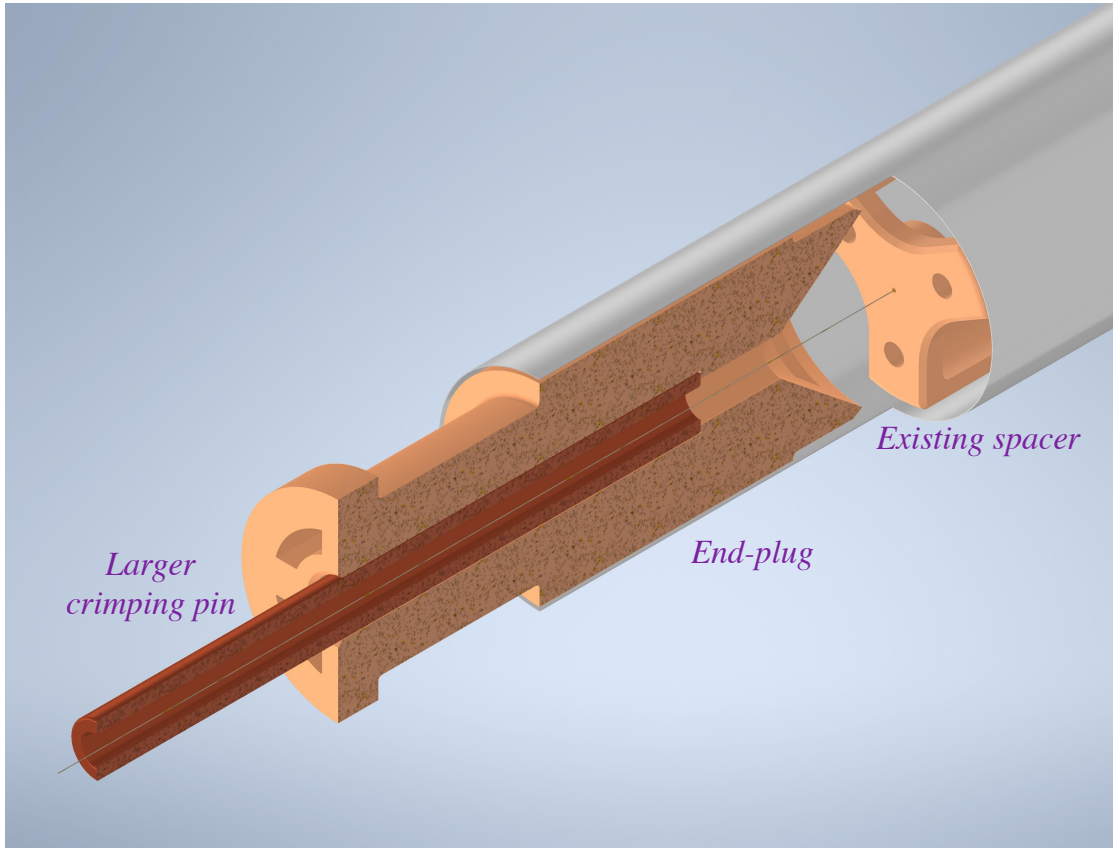




- *Resolution of TAC amplitude < 1mV resulting in TDC measurement FWHM <0.125%;*
- *Timing resolution within simulated 8 µs spill using the 12 bit ADC in MCU;*
- *Preliminary results comparable with the ones obtained with VMM3 and Tiger at testbeam.*

NEW CRIMPING PINS

RP (USC)

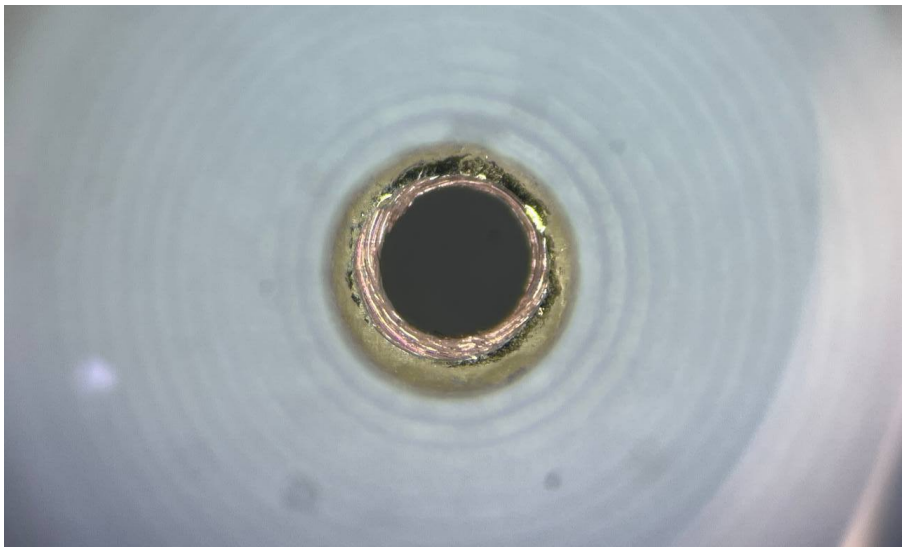


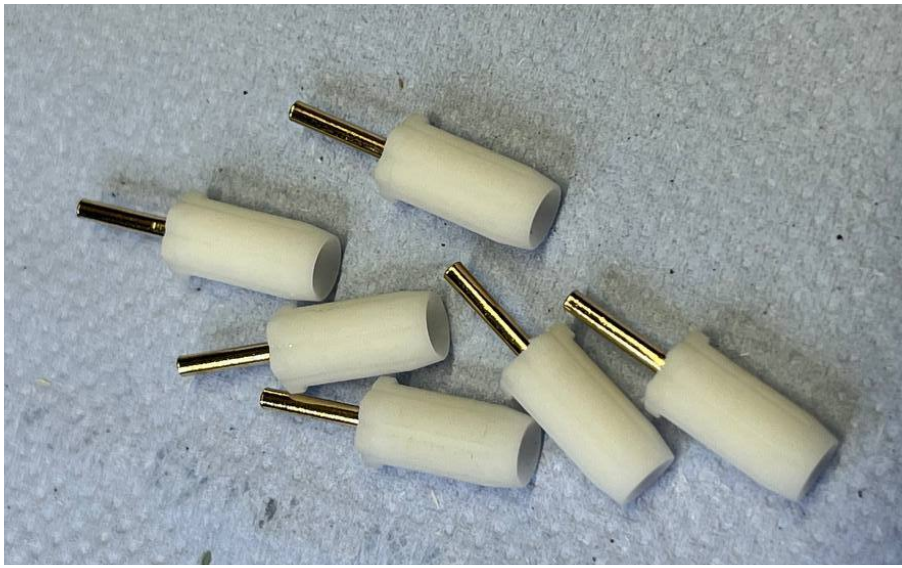
- *New large crimping pins to fix the wire* + *extra spacer for wire centering:*
  - *Reduced costs (~$1.1M savings) and easier supply of pins;*
  - *Simplified assembly procedure: self-centering of wires with glued spacers insensitive to endplug misalignments.*
- *Samples of the final revised pins (v2) delivered to CERN (3,000 pieces total)*

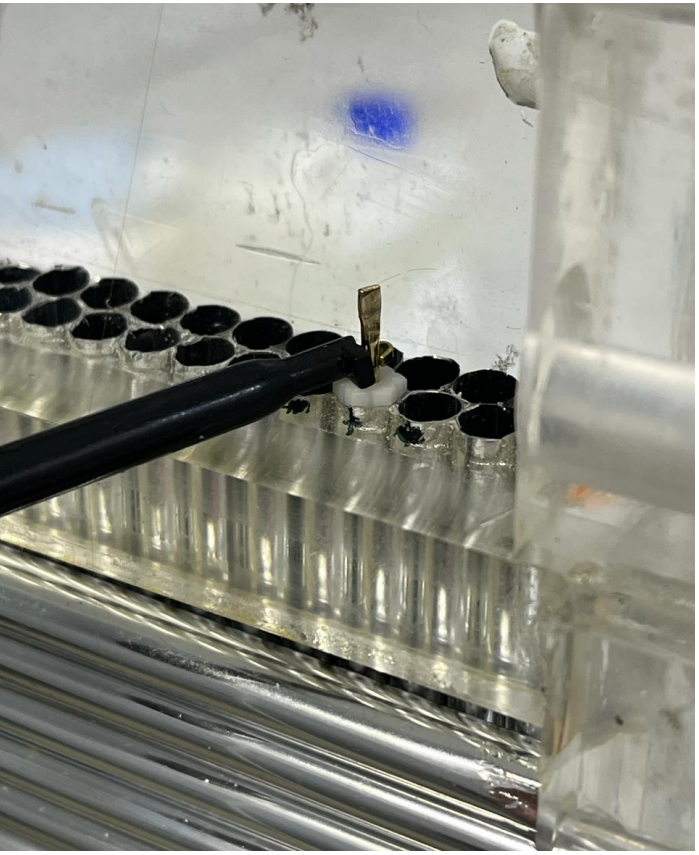
TESTS OF NEW CRIMPING PINS

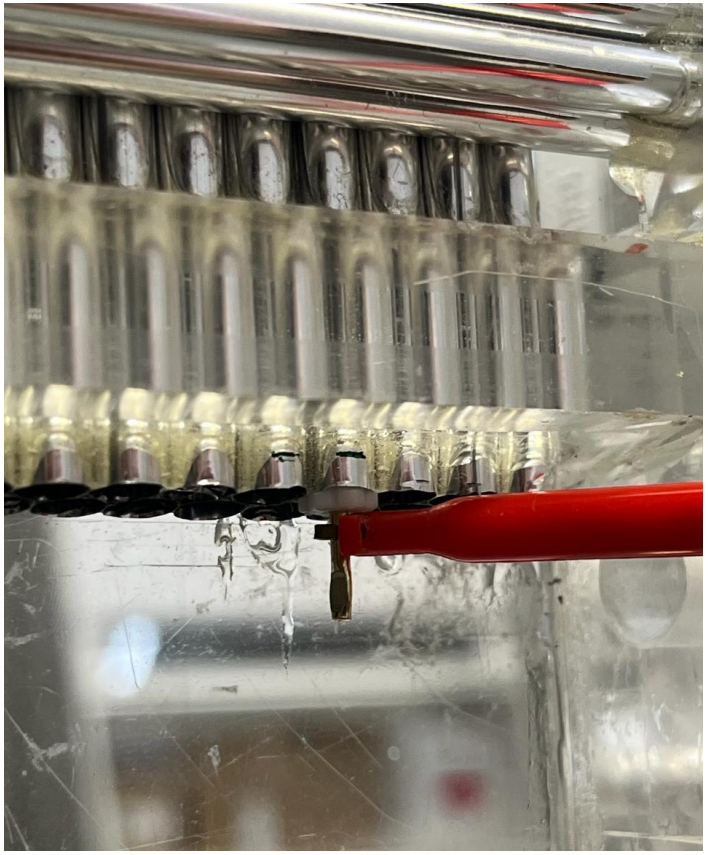
T. Enik (INP)

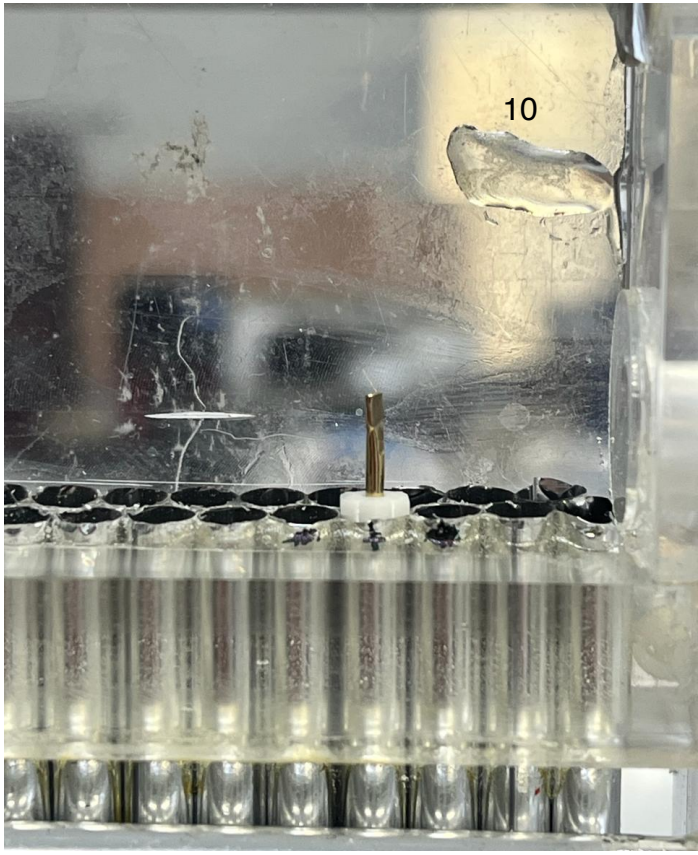
After smoothing the edge of the central hole the sample pins (v1) tested on the mockup STT prototype using temporary 3D printed endplugs

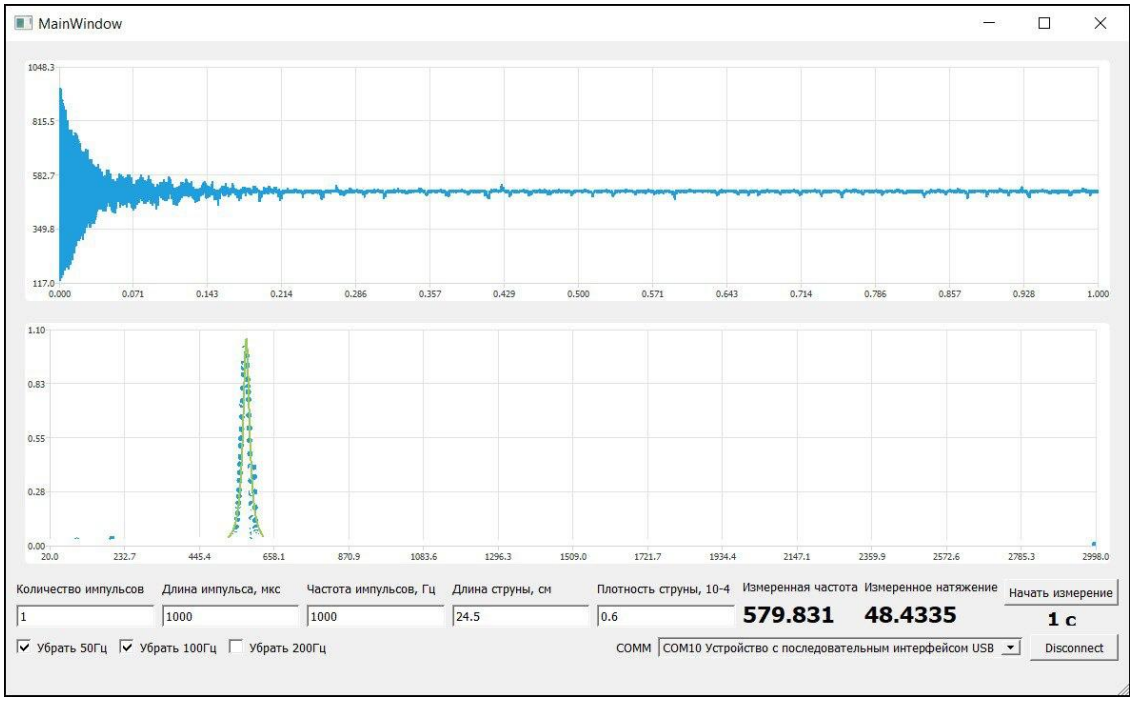










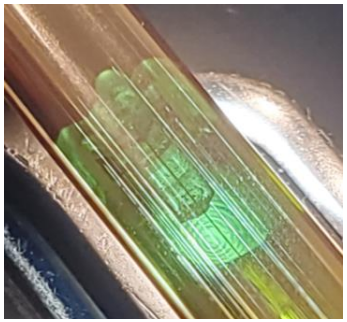
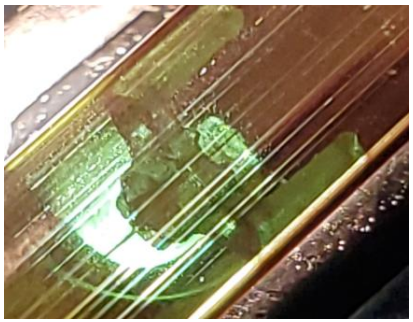
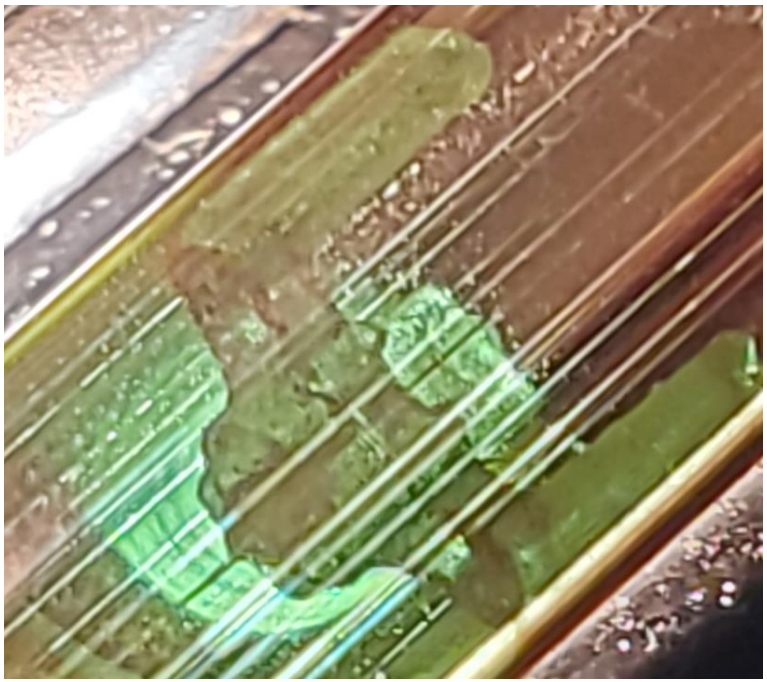
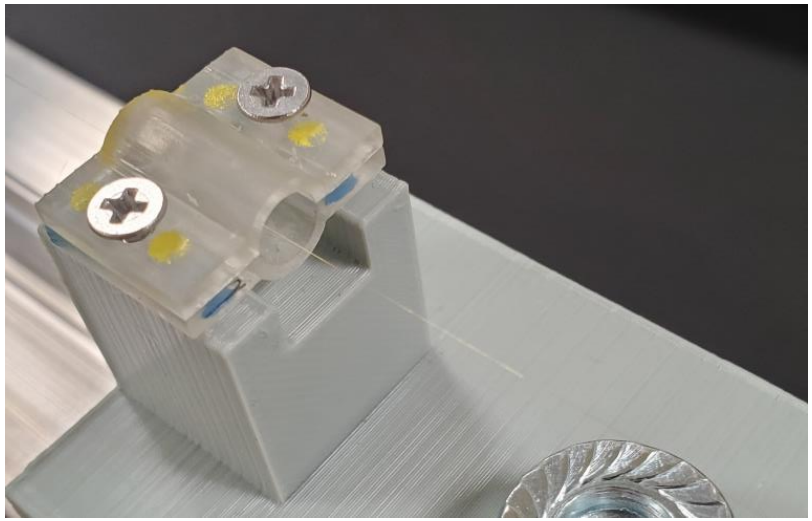
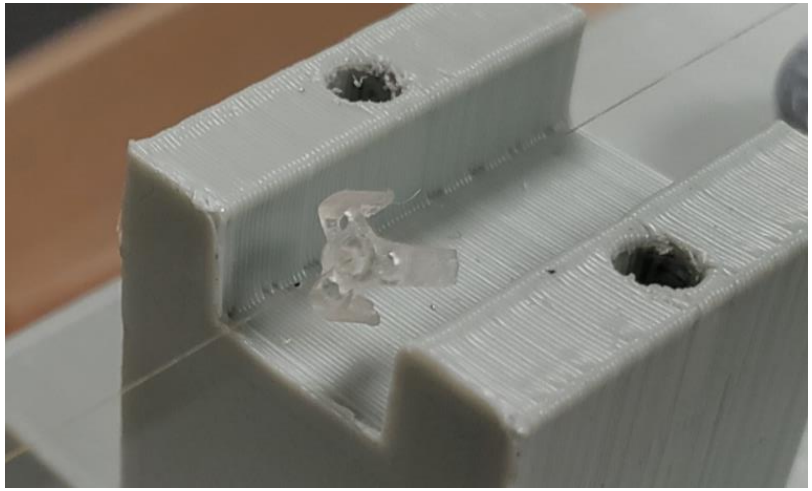


The new pins (v1) can be crimped using the ATLAS tool and hold the LUMA W/Re wire with the correct nominal tension

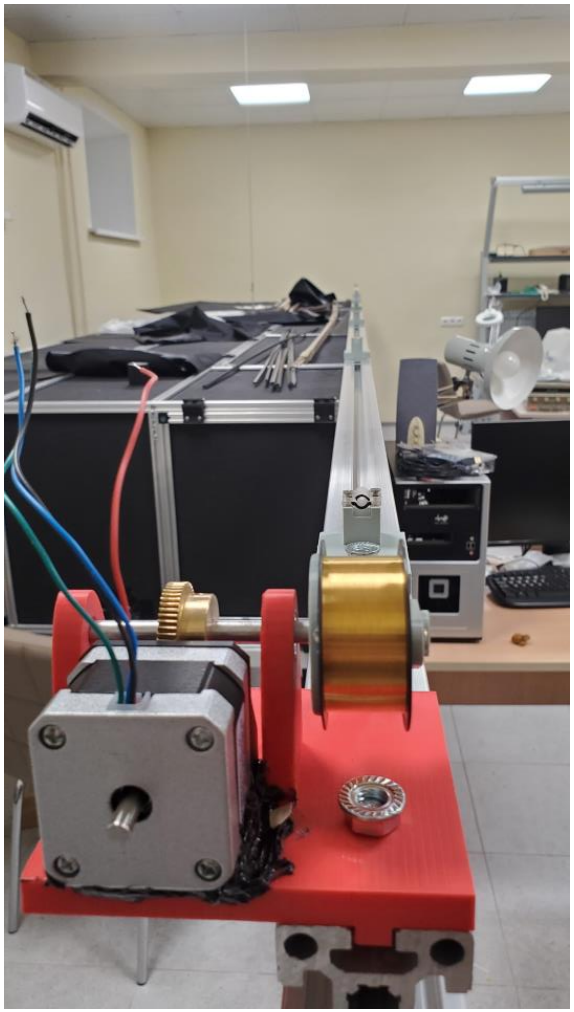
USC

TESTS OF WIRE SPACERS WITH 4m STRAWS

N. Tsverava (GTU)

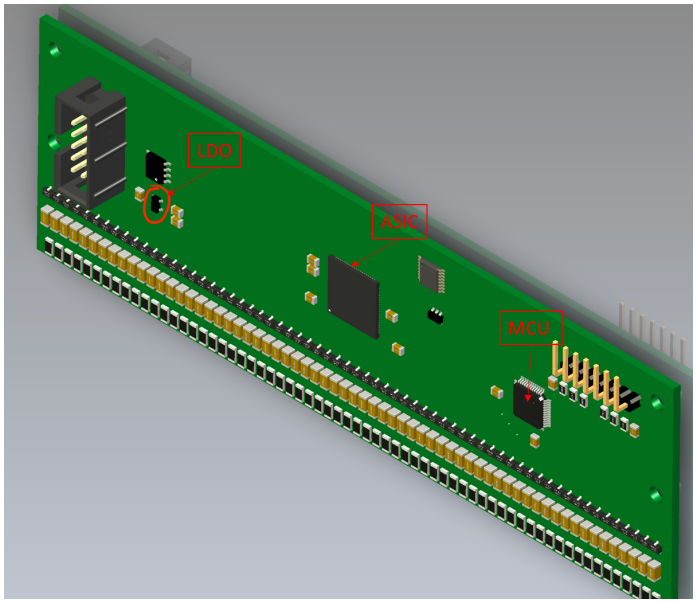
- *Samples of wire spacers produced with UV 3D printing (100 µm hole);*
- *Special Cu/Au straws produced with thin metallization to allow visual inspection of spacers inside;*
- *Drop of dual-component cyanoacrylate glue used to fix the spacer position along the wire.*

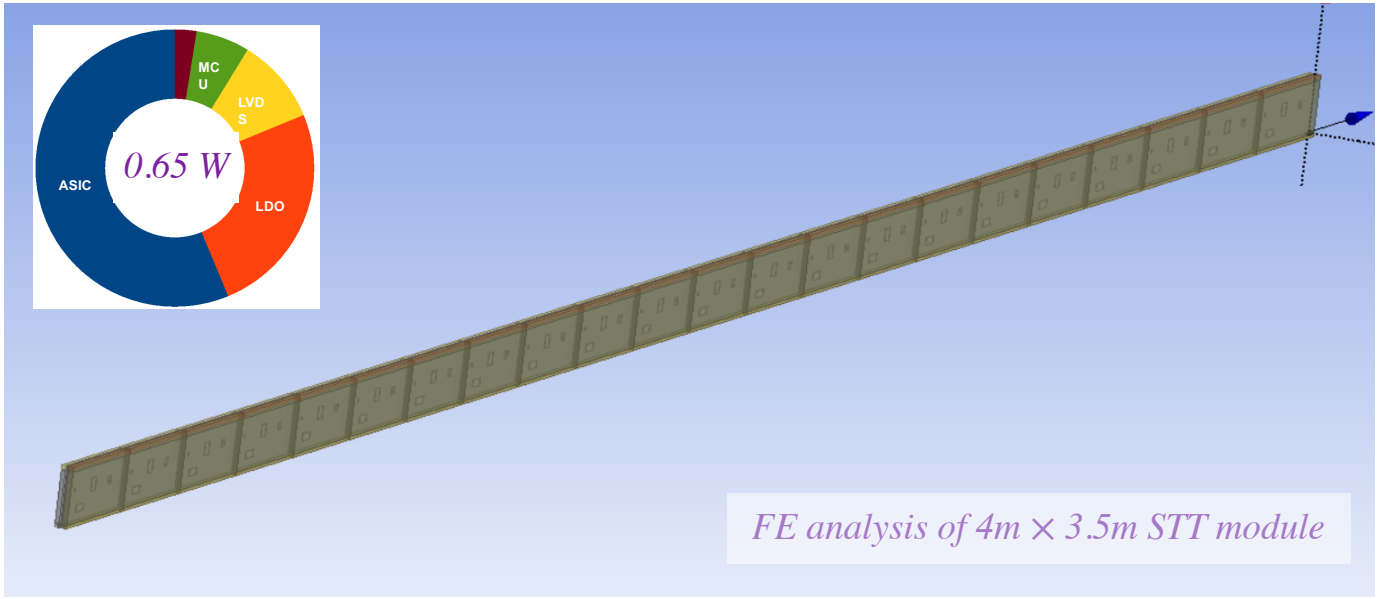


- *First test of wiring 4m straws with 3 spacers along the wire;*
- *Successful wiring if spacer within tolerances and with smooth external surface;*
- *Additional studies to be done: wiring in vertical position, rate of broken wires or wire slippage.*

THERMAL ANALYSIS AND GAS FLOW STUDIES

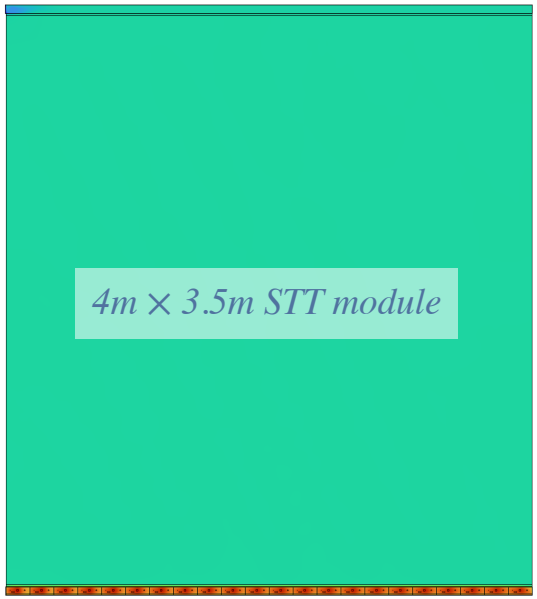
O. Kemularia (GTU)





FE analysis of 4m × 3.5m STT module

- *Thermal analysis of full scale STT module with 22+24 integrated readout boards;*
- *Self-cooling design with expected total power dissipation about 0.65 W per board (mostly ASIC);*
- *Study of gas flow within the STT module to verify uniformity and inlet/endplug design.*



Report Name	Value	Unit
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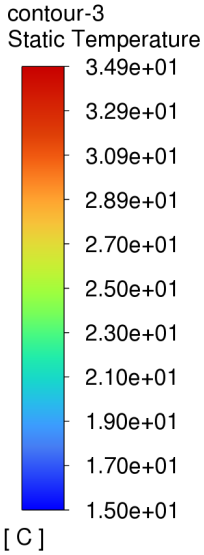
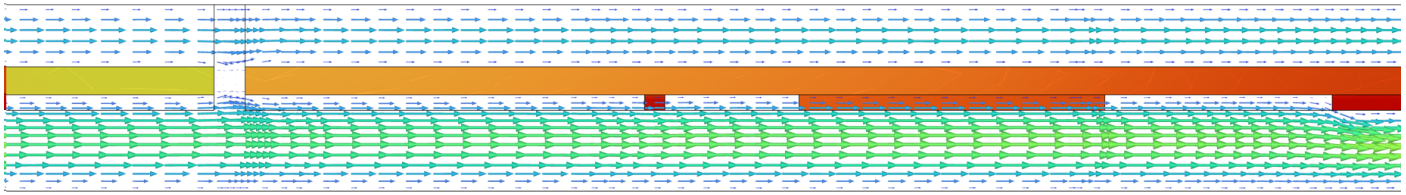
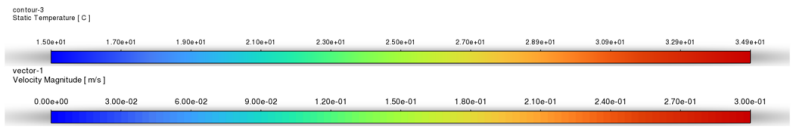
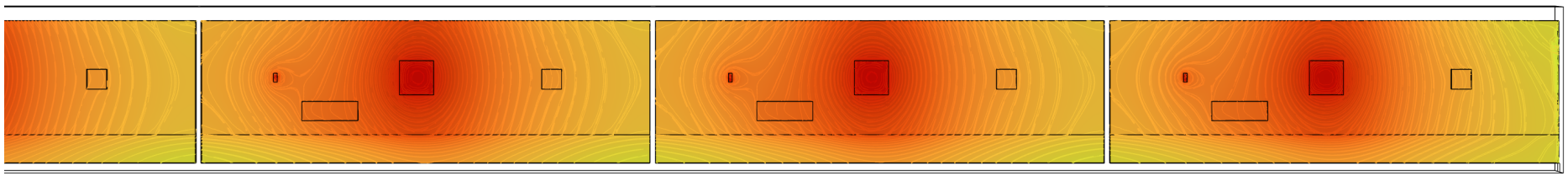
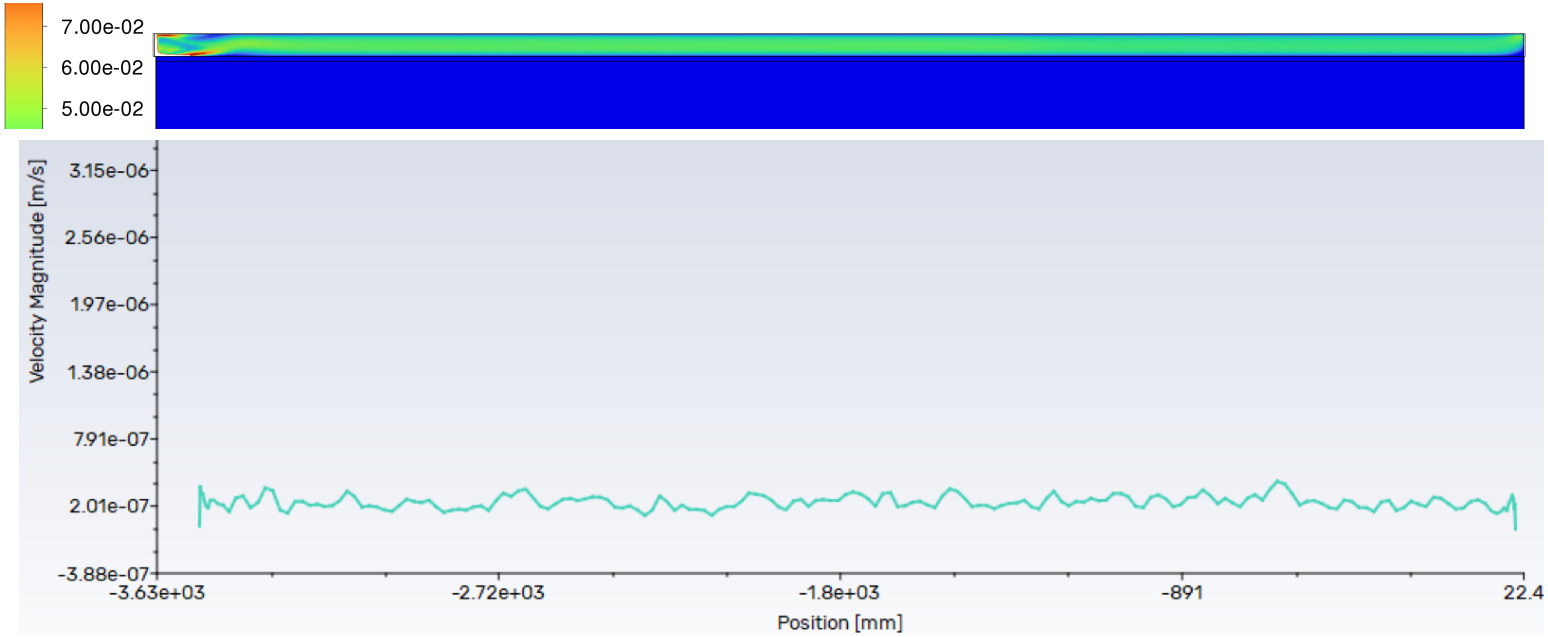
ldo-max-temp	33.675995	
mcu-max-temp	31.036987	
other-max-temp	33.552429	

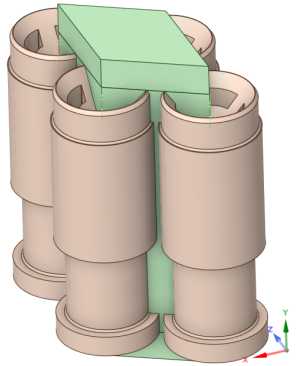










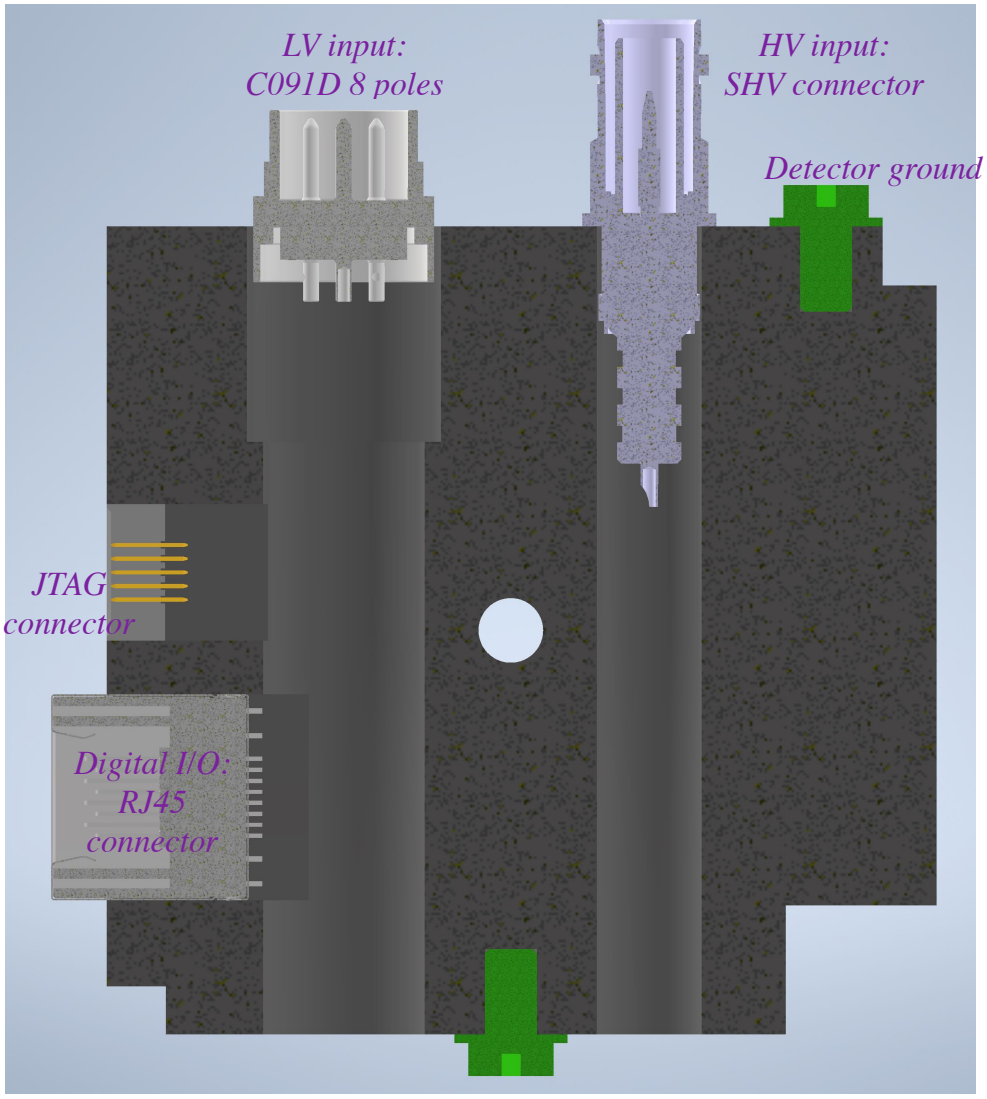


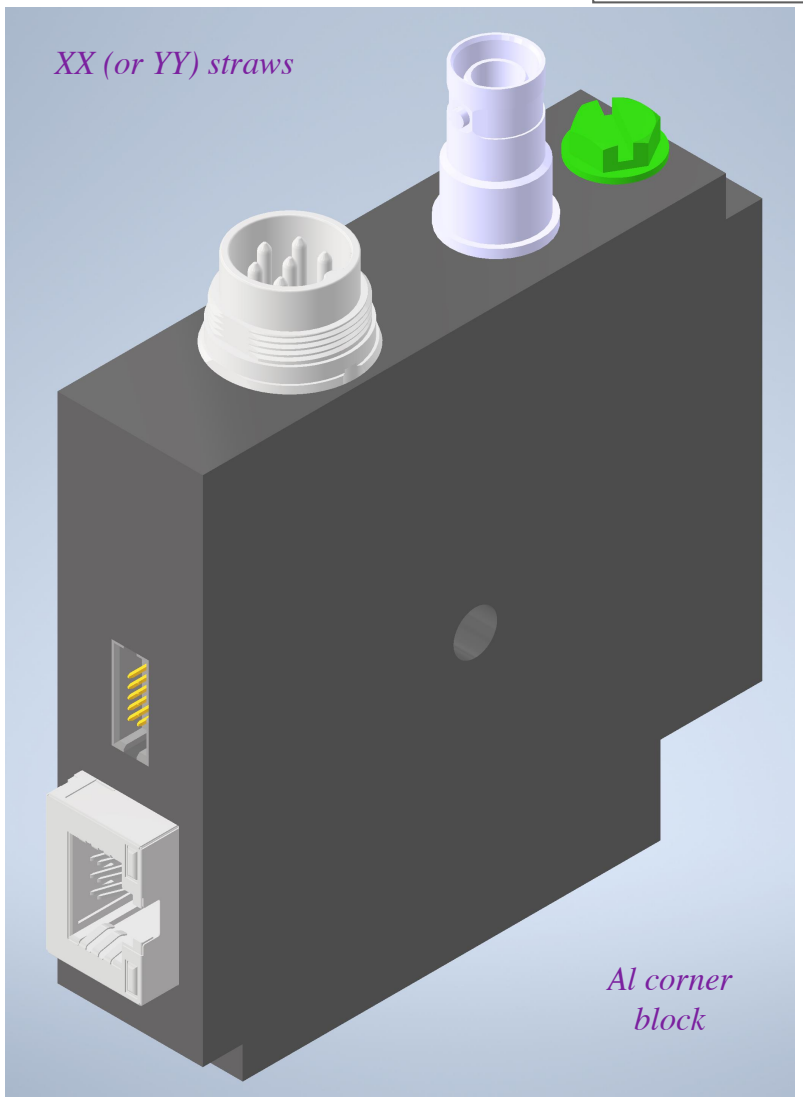
Viscous resistance	1/a	243783132
Inertial resistance	C2	7891.40893
porosity	0.19	

Preliminary results indicate that we can achieve steady state with uniform gas flow across the 4m manifold

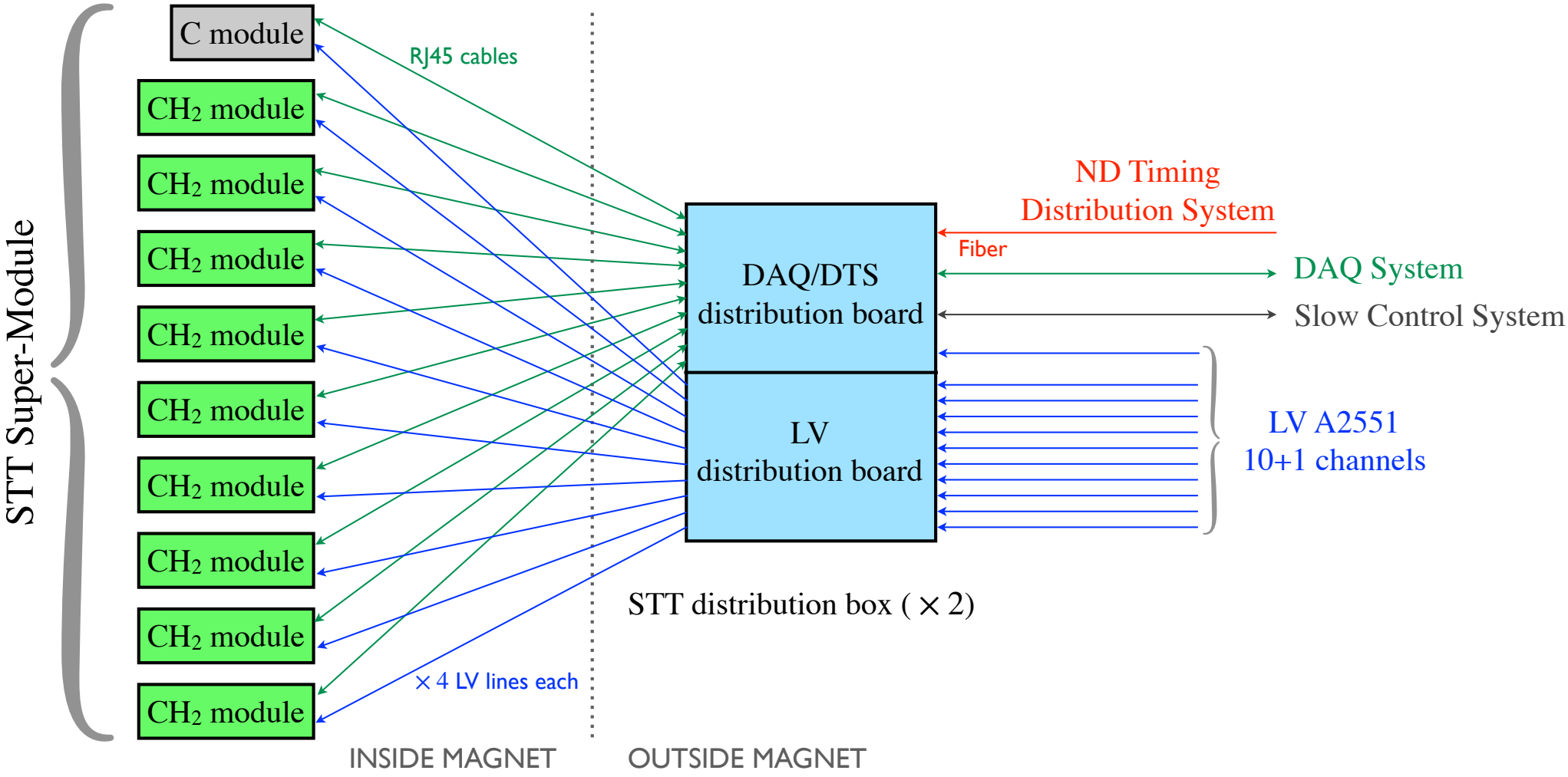
ELECTRICAL CONNECTIONS

RP (USC)





Details of the electrical input/output connections of STT modules (independent for XX and YY layers)



Schematic diagram of the DAQ/DTS and LV connections for one STT Super-Module

DAQ/DTS+LV DISTRIBUTION BOARDS

✦ *Two DAQ/DTS distribution boards per supermodule separate for XX and YY straws:*

- *DAQ/DTS endpoints with FPGA common to other systems;*
- *10 RJ45 shielded cables (one/STT module) from all XX (or YY) straws in a supermodule;*
- *Total of 16 DAQ/DTS distribution boards / endpoints for entire STT.*

$\Longrightarrow$ *Plan to use common DAQ/DTS boards with GRAIN (N. Tosi)*

✦ *One LV distribution board for each DAQ/DTS board:*

- *10 (one/STT module) + 1 (DAQ/DTS) LV channels feeding all XX (or YY) straws in supermodule;*
- *Maximal number of output LV cables: 4×10 depending on input lines in STT module;*
- *Same modularity for DAQ/DTS and LV distribution grouped within same distribution box.*

✦ *Each DAQ/DTS+LV distribution box outside of magnet close to supermodule:*

- *Minimize length of cables as distribution boards close to corner blocks with electrical connections;*
- *All RJ45 & LV cables connected to a DAQ/DTS distribution boards will have identical length.*

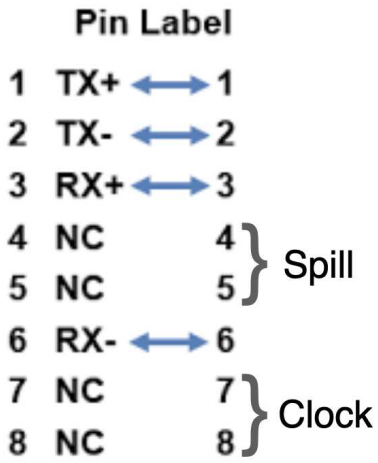
DIGITAL I/O CONNECTIONS

✦ *RJ45 digital I/O connector for XX (or YY) readout boards:*

- *4 pairs of LVDS signals: data TX, data RX, begin of spill, machine clock;*
- *All XX (or YY) FE boards share common TX and RX lines like in RS422 protocol (V. Bautin);*
- *All FE boards can receive data at all times, but only one transmits at a time;*
- *MODBUS (or similar) request-response protocol.*

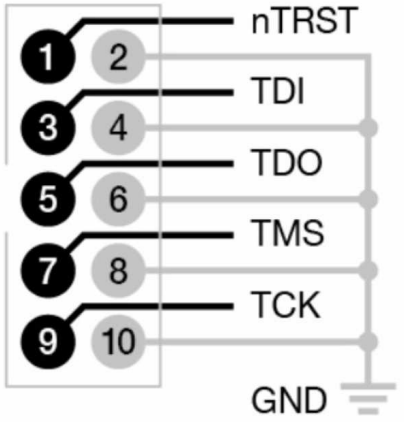
✦ *JTAG connector for firmware update in all XX (or YY) readout boards:*

- *After detector commissioning & initial runs we do not expect frequent updates;*
- *No need of permanent cable to DAQ/DTS distribution boards.*



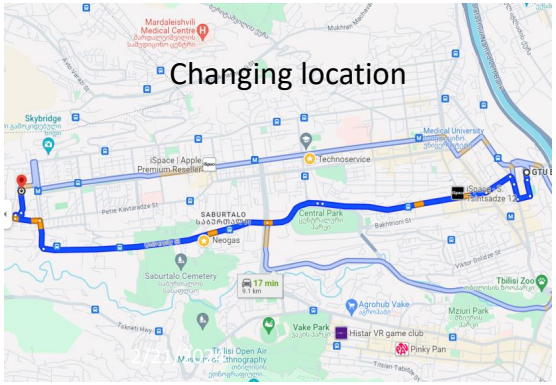
RJ45 connector

JTAG connector



PREPARATION FOR STT PRODUCTION AT GTU

N. Tsverava (GTU)



- *Preparation of new larger laboratory for STT production in Tbilisi;*
- *Double straw production line (2×5m) with ultrasonic welding moved to new laboratory;*
- *Straw production lines being upgraded with new parts to improve accuracy.*

Backup slides

PROTOTYPING & TESTS

Demonstrate all aspects of the STT design in increasing order of complexity:

- ☑ *Produce straws of required quality & maximal length with ultrasonic welding (UW)*
  $\Longrightarrow$ *Validation of model production lines at JINR (5m) and GTU (2m)*
- ☑ *Verify UW straws fulfill requirements from STT conceptual design & assembly procedure*
  $\Longrightarrow$ *Measurement of maximal internal pressure, radial and longitudinal deformations vs. pressure, relaxation vs. time and humidity, gas tightness, etc.*
- ☑ *Verify XXYY straw layer assembly*
  $\Longrightarrow$ *Gluing and pressure tests of 1m $\times$ 1m XXYY test assembly*
- ☑ *Verify assembly procedure of XXYY straws to frame, gas tightness, etc.*
  $\Longrightarrow$ *Assembly and tests of mockup prototype with plexiglass frame*
- ☑ *Verify module design with C-composite frame and related performance*
  $\Longrightarrow$ *Complete 1.2m $\times$ 0.8m prototype with XXYY straws and actual STT frame design*
- ☐ *Verify full scale module ("module 0") with maximal straw length and complete assembly*
  $\Longrightarrow$ *Complete 4m $\times$ 3m prototype with XXYY straws and C-composite frame*

Demonstrate readout performance:

- ☑ *Verify charge measurement with ^{55}Fe source & cosmics*
  $\Longrightarrow$ *Readout small STT prototype with Mu2e FE boards with VMM3 ASICs*
- ☑ *Verify time measurement with signal generator*
- ☑ *Verify time and charge measurement at testbeam*
  $\Longrightarrow$ *Readout small STT prototype with FE boards with VMM3 and Tiger ASICs*

	VMM3	TIGER
Number of channels	64	64
Clock frequency	10...80 MHz	160...200 MHz
Input capacitance	<300 pF	<100 pF
Dynamic range	Linearity within ±2% up to 2 pC	50 fC
Gain	0.5, 1, 3, 6, 9, 12, 16 mV/fC	12 mV/fC
ENC (energy branch)	<3000 e^-	<1500 e^-
TDC binning	~1 ns	50 ps
Maximum event rate	4 MHz/ch	60 kHz/ch
Consumption	15 mW/ch	12 mW/ch