Cold Electronics Development for LAr TPC

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On behalf of the Cold Electronics Team

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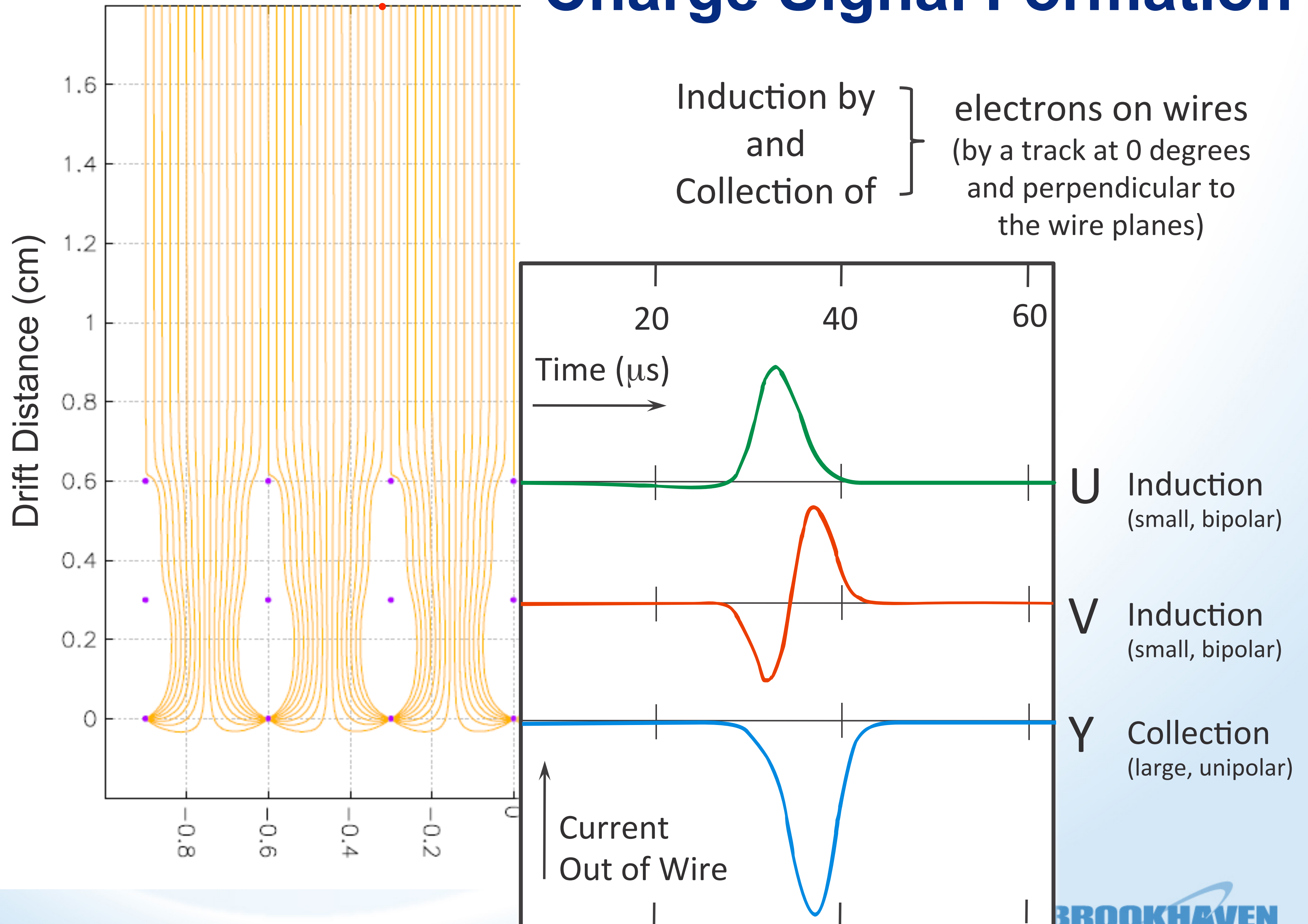
BROOKHAVEN NATIONAL LABORATORY

a passion for discovery

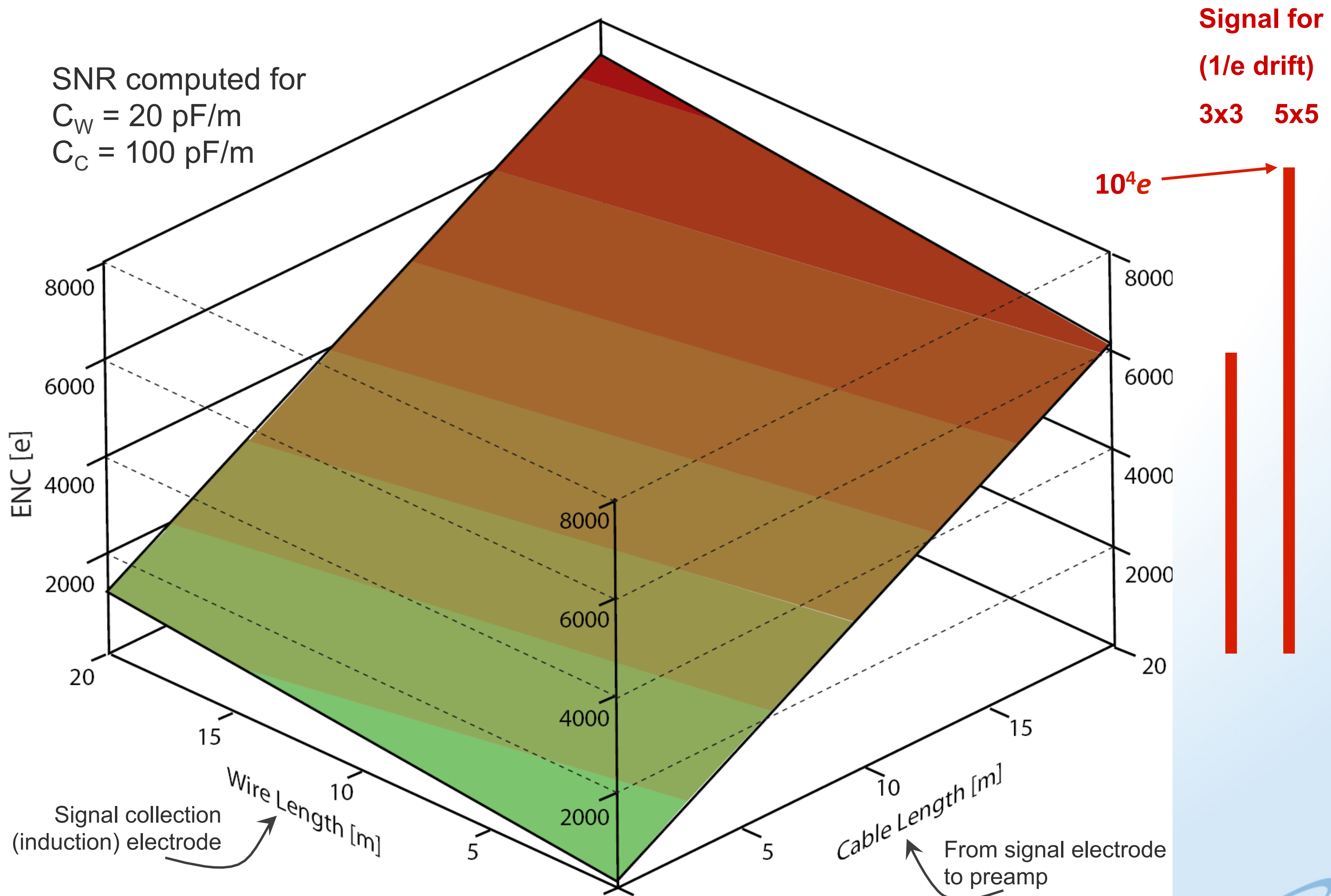
Outline

- **Introduction**
  - **LAr TPC Signal Properties**
  - **Why Use Cold Electronics**
- **Cold Electronics Development**
  - **MicroBooNE**
  - **LBNE**
  - **35 Ton**
- **CMOS Lifetime**
  - **CMOS in DC operation: analog FE ASIC**
  - **CMOS in AC operation: logic circuit and FPGAs**
- **Summary**

Charge Signal Formation



Why Use Cold Electronics



Signal for (1/e drift)

3x3 5x5

$10^4 e$

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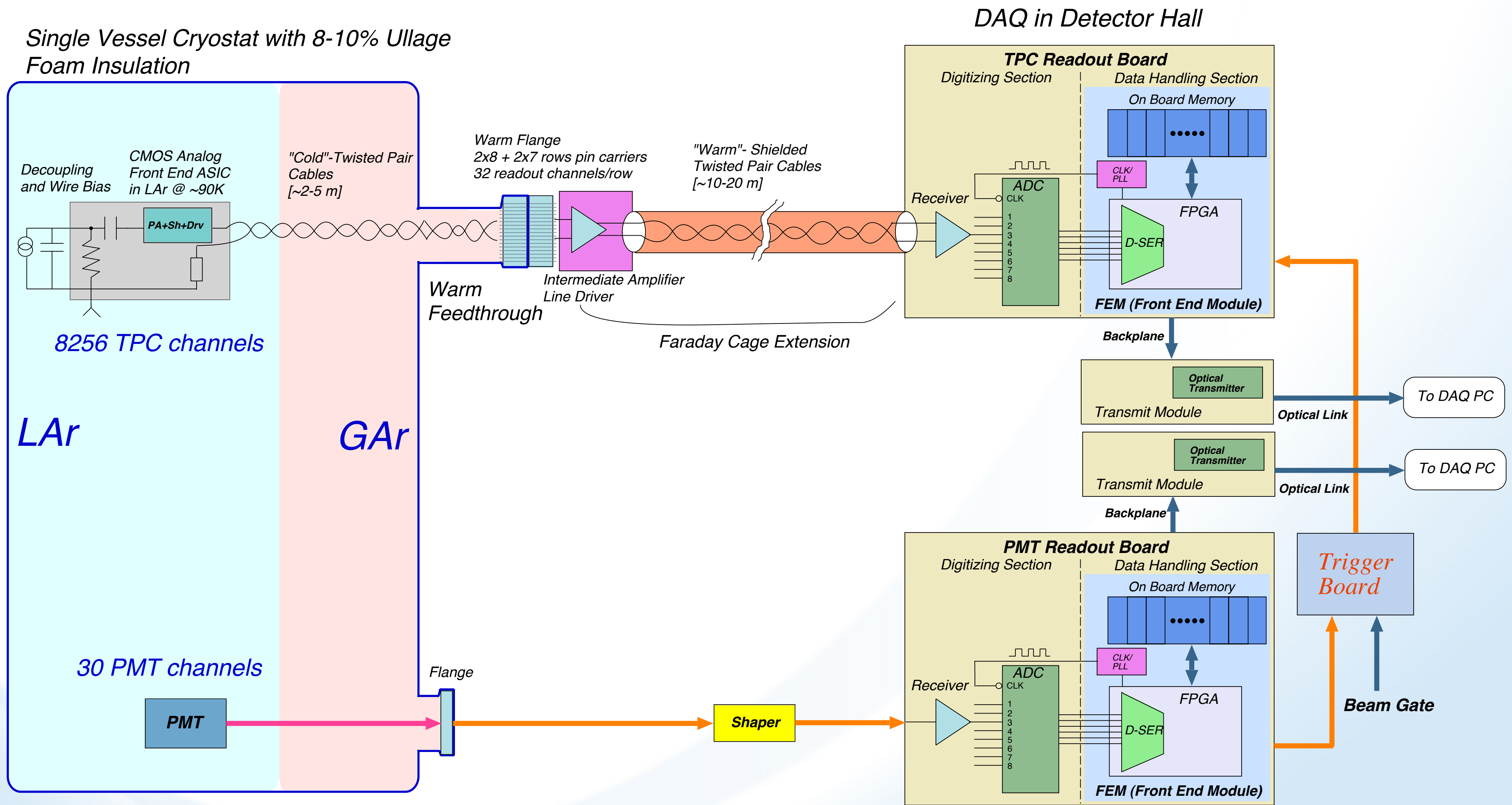
- **Cold Electronics Development**
  - **MicroBooNE**
  - **LBNE**
  - **35 Ton**

MicroBooNE Readout Electronics System



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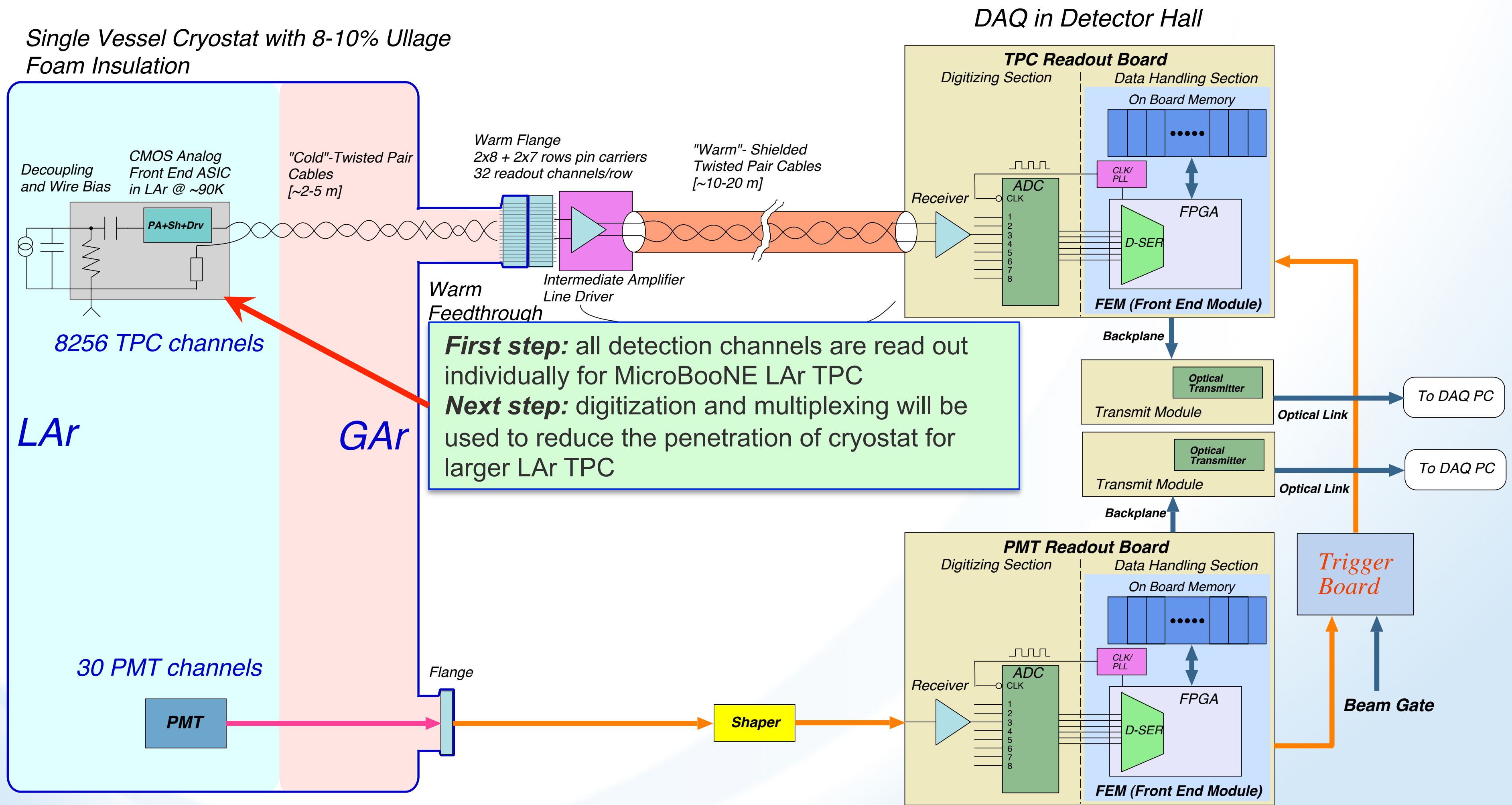
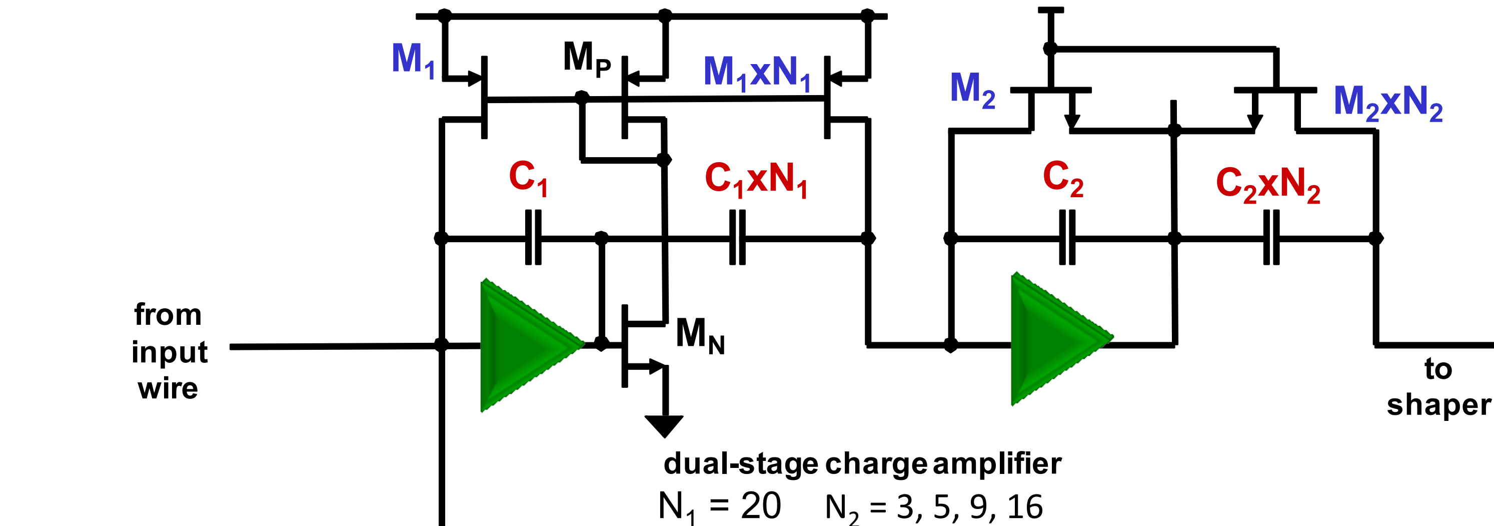
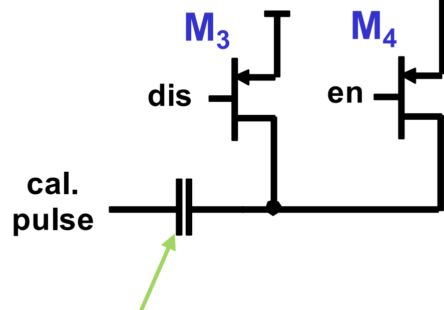
MicroBooNE Cold Electronics

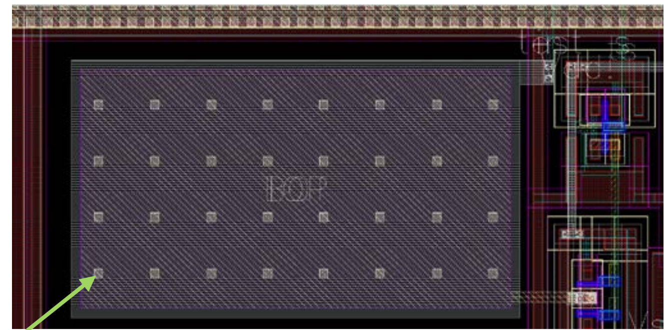


First step: all detection channels are read out individually for MicroBooNE LAr TPC
Next step: digitization and multiplexing will be used to reduce the penetration of cryostat for larger LAr TPC

Cold Electronics ASIC - Front-End Detail and Calibration Scheme







$C_{INJ} \approx 180$ fF

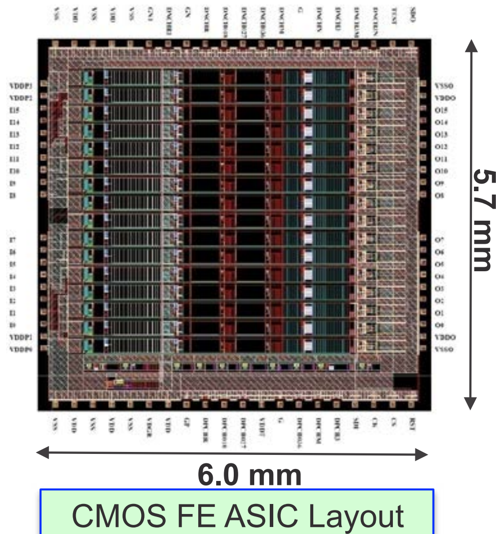
Integrated injection capacitance (10 x 18 μm²)

Measured with high-precision external capacitance

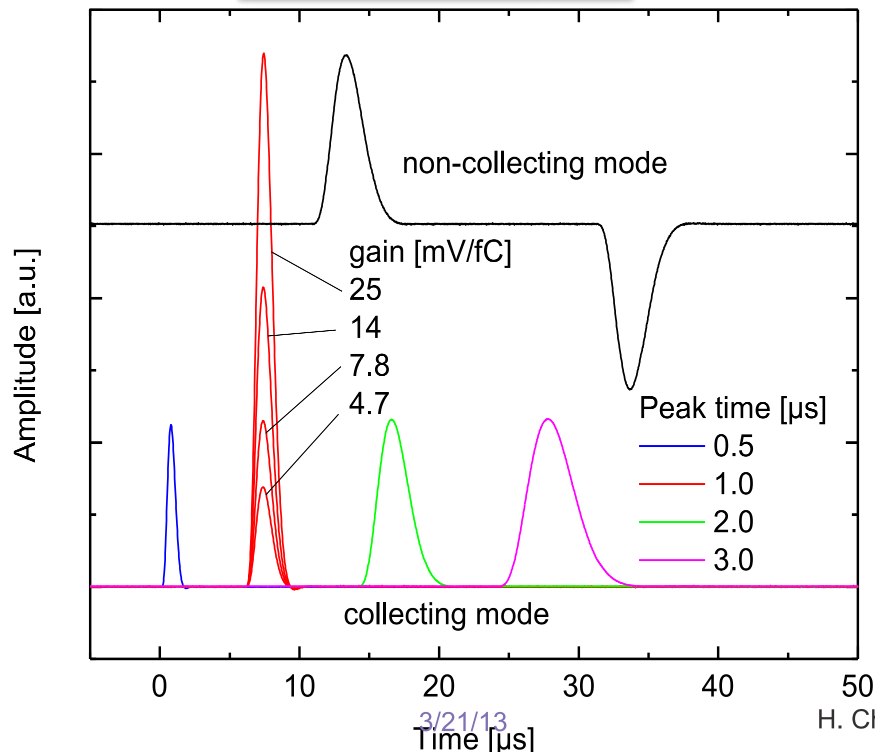
$$C_{INJ} \approx \begin{cases} 184\ fF \ \ at\ \ 300K \\ 183\ fF \ \ at\ \ 77K \end{cases}$$

Charge sensitivity calibration of entire TPC during assembly, cooling and operation

MicroBooNE Cold Electronics

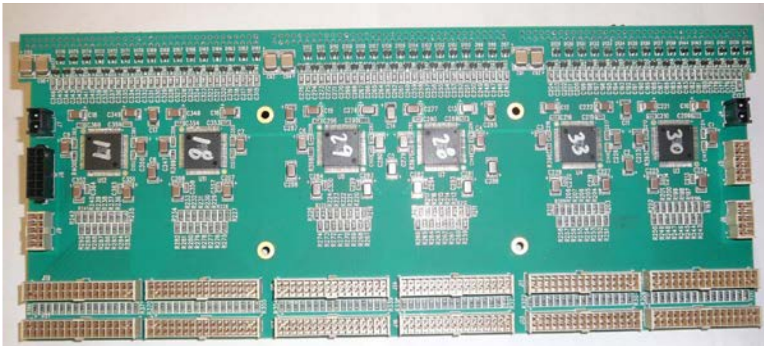


CMOS FE ASIC Layout

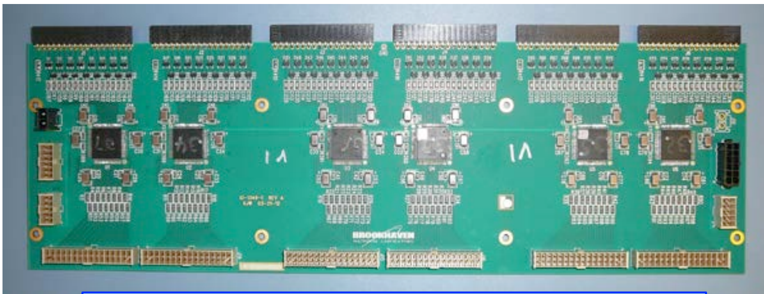


- **CMOS Analog Front End ASIC**
  - **16 channels per chip**
  - **Charge amplifier, high-order filter**
  - **Adjustable gain: 4.7, 7.8, 14, 25 mV/fC (55, 100, 180, 300 fC)**
  - **Adjustable filter time constant (peaking time): 0.5, 1, 2, 3 μs**
  - **Selectable collection/non-collection mode (baseline)**
  - **Selectable dc/ac (100 μs) coupling**
  - **Rail-to-rail analog signal processing**
  - **Band-gap referenced biasing**
  - **Temperature sensor (~ 3mV/°C)**
  - **136 registers with digital interface**
  - **5.5 mW/channel (input MOSFET 3.6 mW)**
  - **~ 15,000 MOSFETs**
  - **Designed for long cryo-lifetime**
  - **Technology CMOS 0.18 μm, 1.8 V, 6M, MIM, SBRES**

MicroBooNE Cold Electronics



Horizontal cold motherboard with 12 ASIC chips (192 channels) populated



Vertical cold motherboard with 6 ASIC chips (96 channels) populated

- **Cold Mother Board**
  - **House front end ASIC**
  - **Rogers 4000 series base material**
  - **Provide detector signal interconnections**
  - **Provide ASIC control and monitoring signals, calibration network**
  - **Provide bias voltage distribution for wire planes**
  - **Horizontal version**
    - **96 “Y” channels**
    - **48 “U” channels**
    - **48 “V” channels**
  - **Vertical version**
    - **96 “U” or “V” channels**

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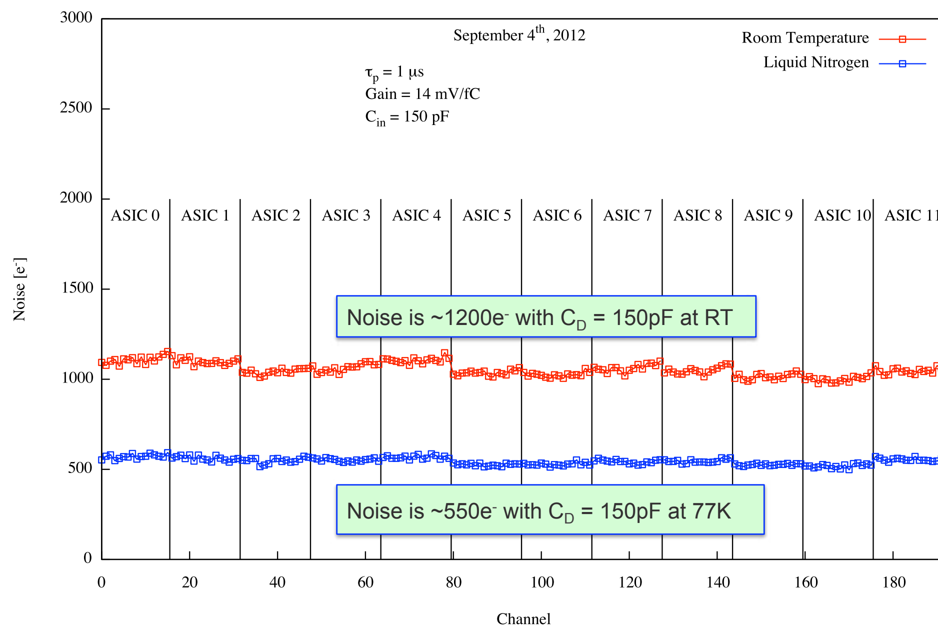
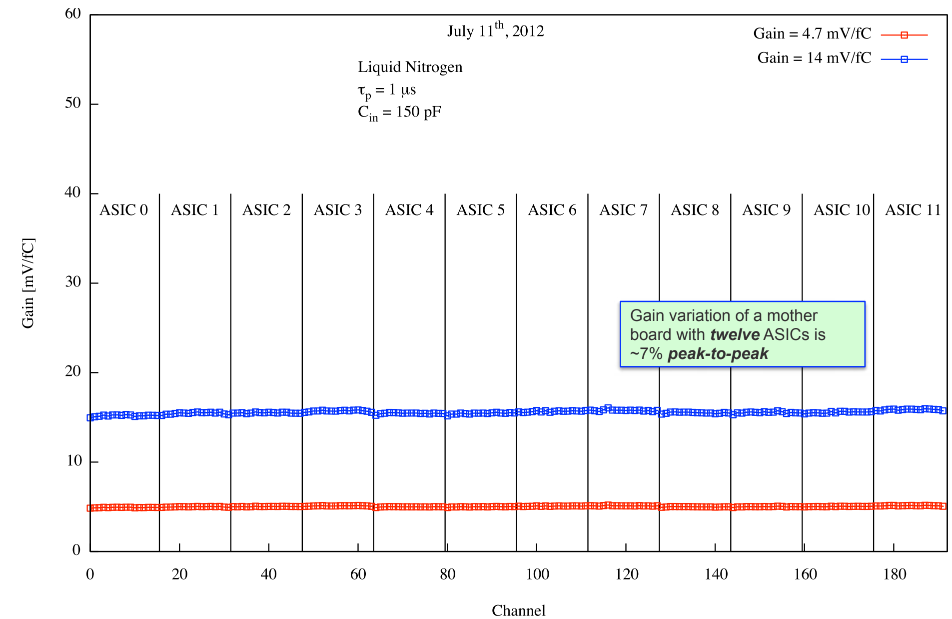
MicroBooNE Cold Electronics

Noise *vs.* Temperature: 12 ASICs (192 channels)



ASICs Gain Uniformity: 12 ASICs (192 channels)



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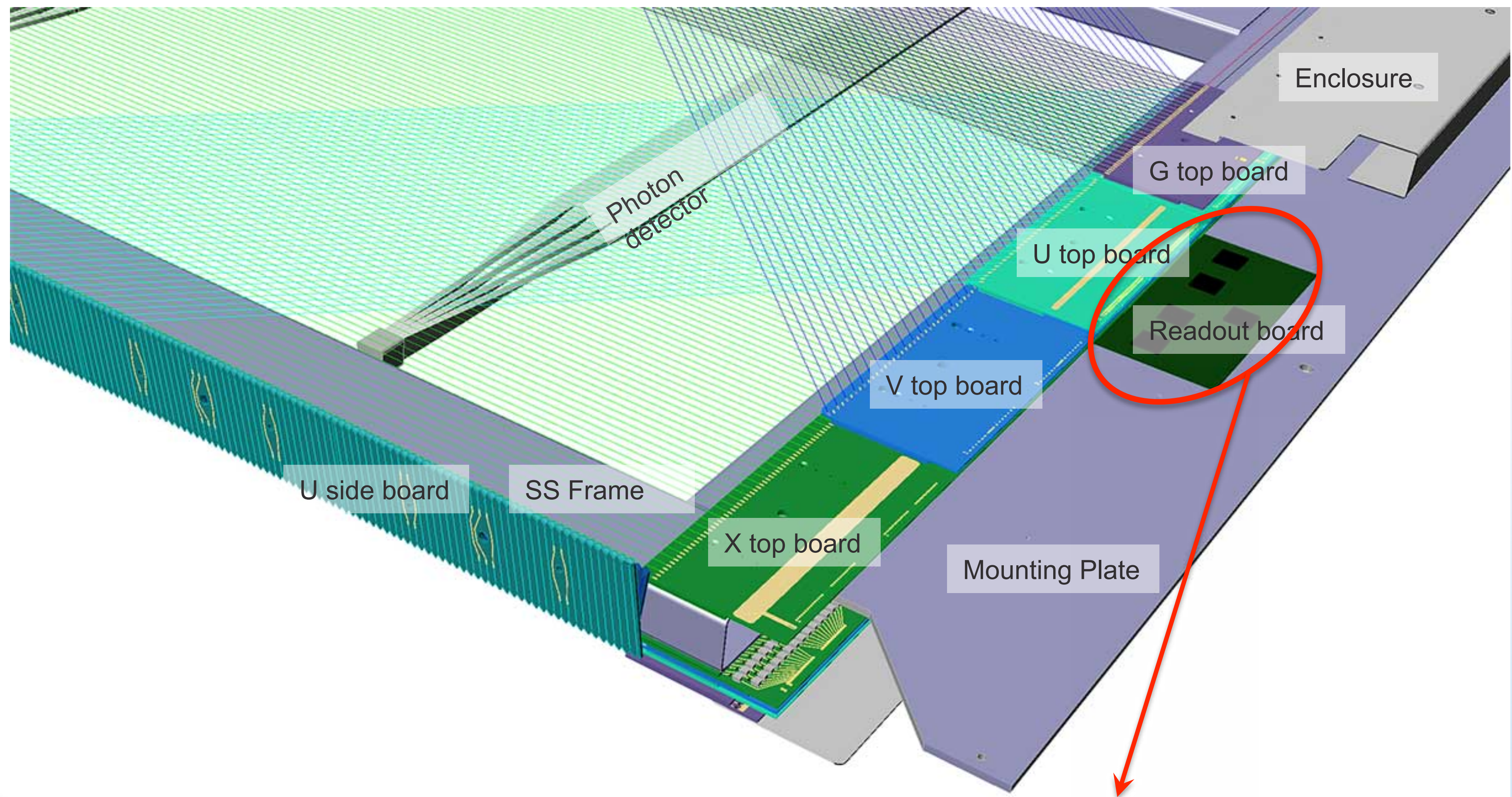
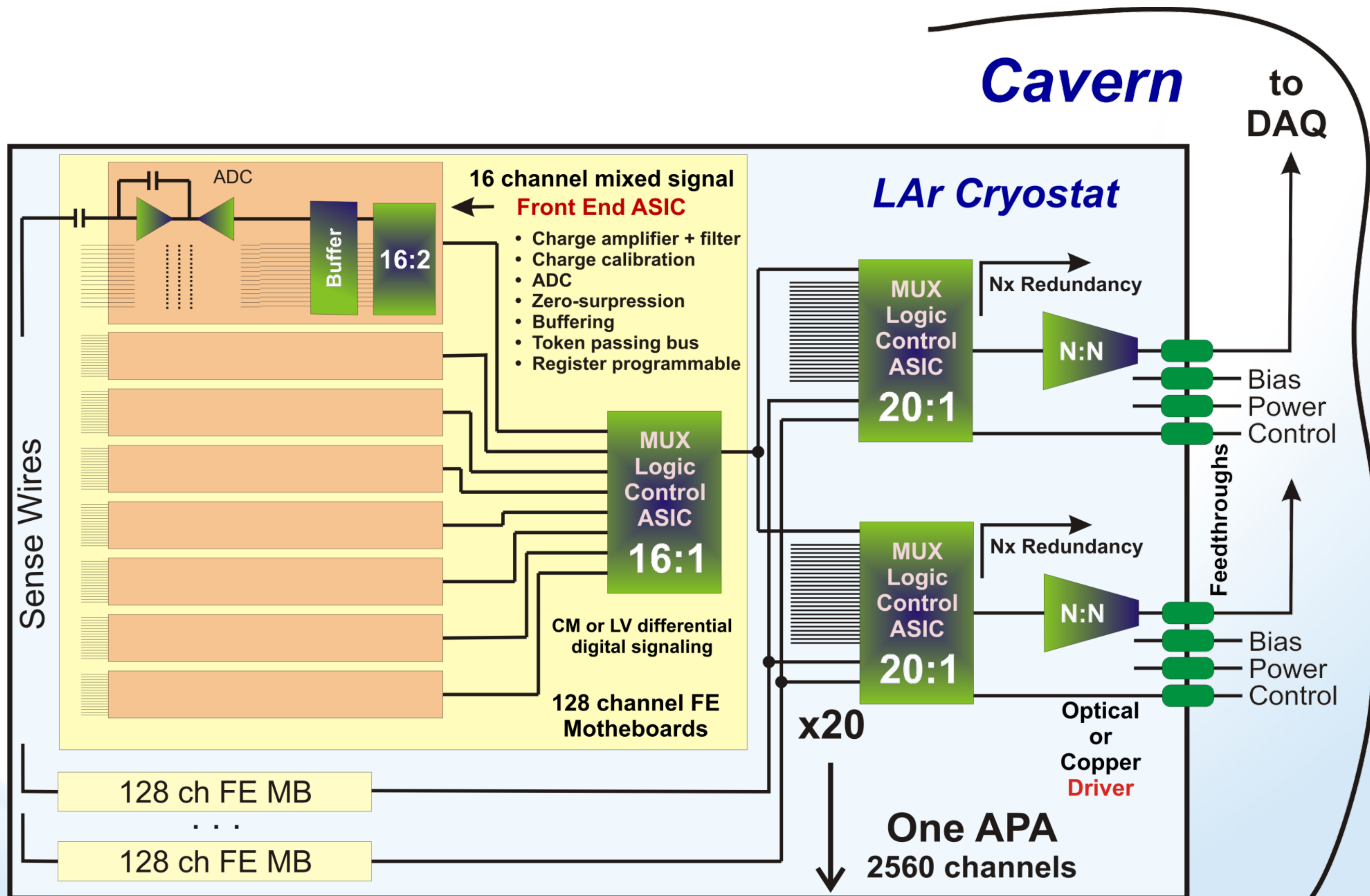
- **Cold Electronics Development**
  - MicroBooNE
  - **LBNE**
  - 35 Ton

Cold Electronics for LBNE LAr TPC



- **1 APA – 2560 wires**
  - **1120 X wires @ 4.5mm pitch**
  - **720 U wires @ 4.9mm pitch**
  - **720 V wires @ 5.0mm pitch**
- **Front End Mother Board**
  - **128 channels: 56X, 36U,36V**
  - **20 mother boards mounted on one end of the APA frame**

Cold Electronics for LBNE LAr TPC



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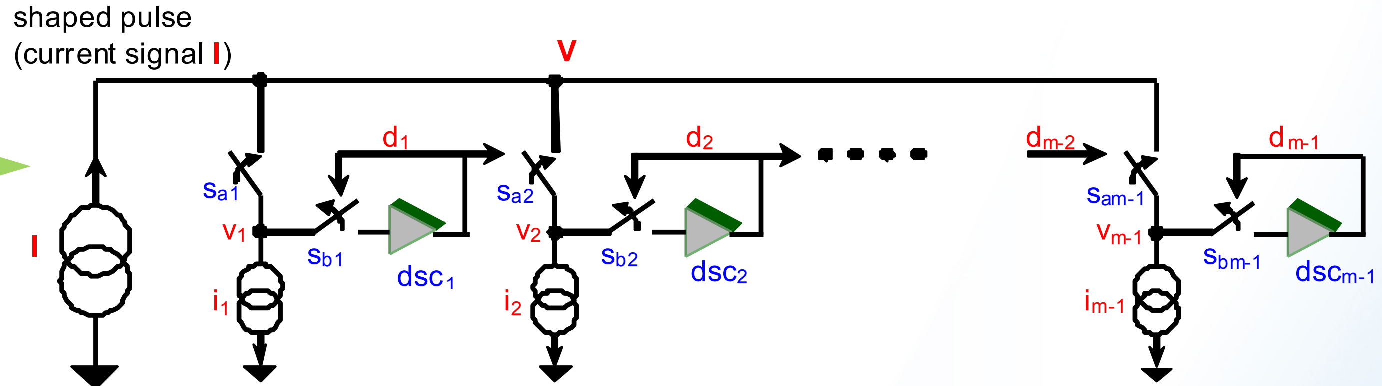
ADC - Architecture

Clockless Low Power Current Mode ADC

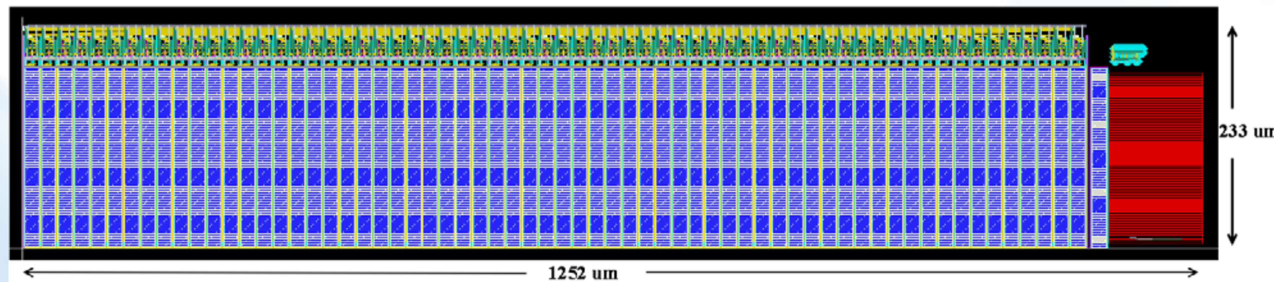
One ADC stage



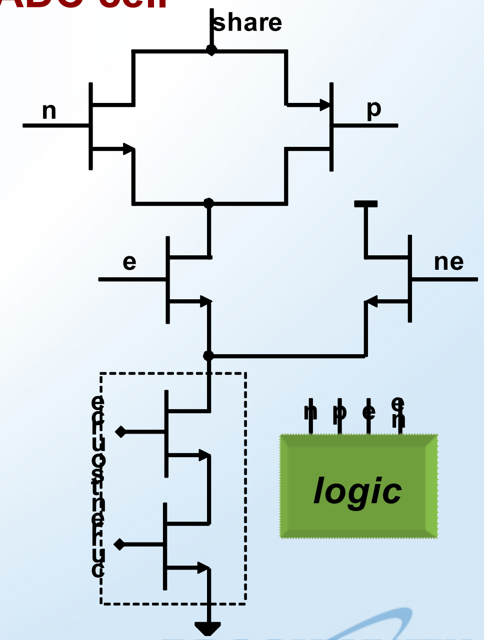
Fabricated in ASIC for SNS, see De Geronimo, et al., *IEEE Trans NSS*, **54** (2007) 541.

Design

- Dual stage: 6-MSBs in 150ns, then 6-LSBs in 250ns
- Single conversion trigger per stage
- 12-bit resolution
- 2 MS/s conversion rate
- Power dissipation 3.6 mW at 2 MS/s
- Power-down option
  - Wake up in few tens of ns
- Layout size: 0.23 mm x 1.25 mm



ADC cell



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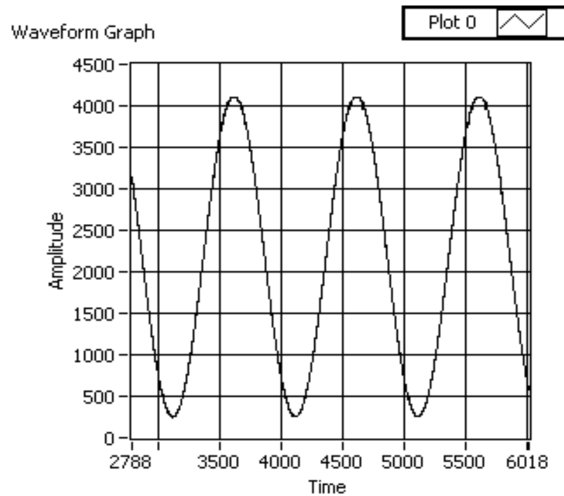
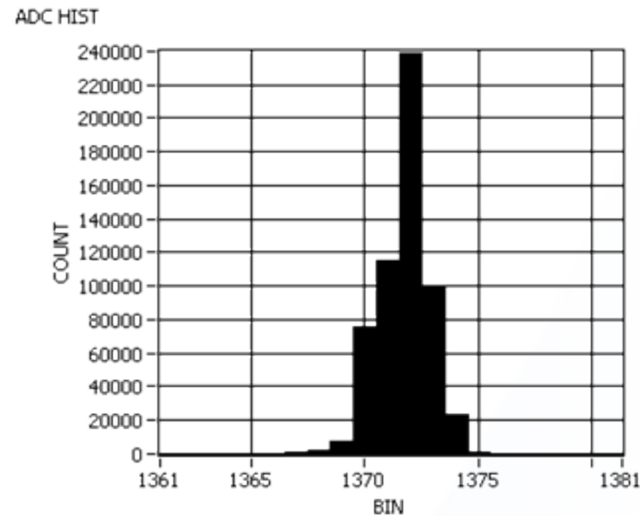
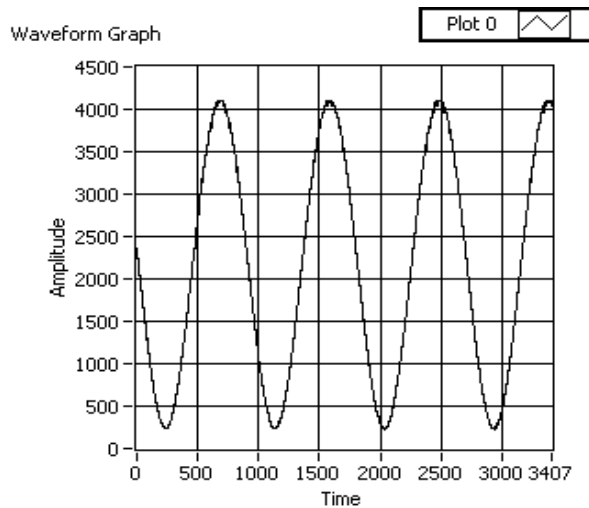
Single Cold ADC Test Results



Sinewave at RT



ADC Output Histogram DC



Sinewave at 77 K

- **Measured linearity**
  - **DNL < 1.5 LSB for majority of codes**
  - **INL ~1% of Range**
- **Equivalent input noise measurement**
  - **1.27 LSB**
  - **Effective resolution: 11.6 bits**
- **The ADC has been tested with an FPGA, both immersed in LN_2**

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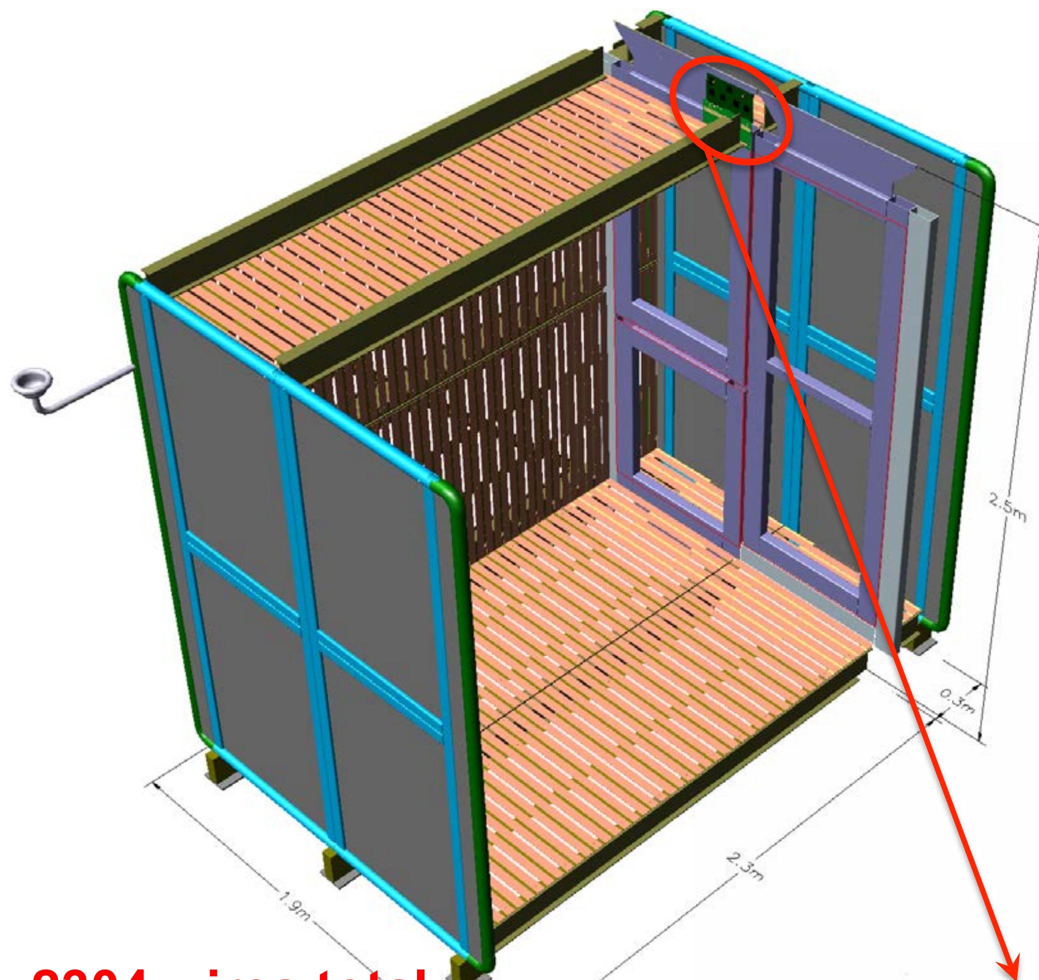
  - **LBNE**
  - **35 Ton**

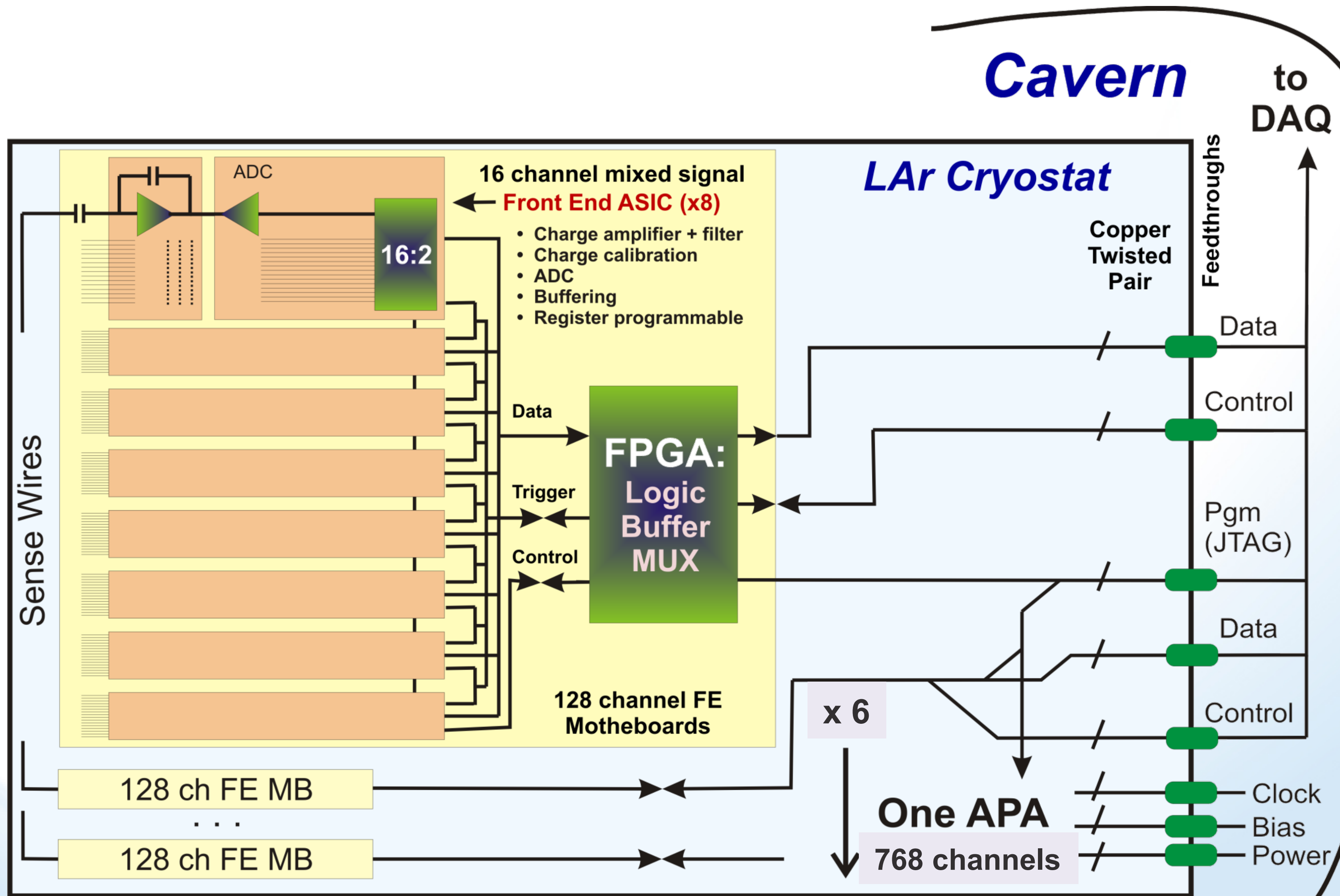
Cold Electronics for 35T LAr TPC



- **3 APA – 2304 wires total**
  - **Each APA has 768 wires**
  - **336 X wires @ 4.5mm pitch**
  - **216 U wires @ 4.9mm pitch**
  - **216 V wires @ 5.0mm pitch**

- **Front End Mother Board**
  - **128 channels: 56X, 36U,36V**
  - **6 mother boards mounted on one end of the APA frame**

Cold Electronics for 35T LAr TPC



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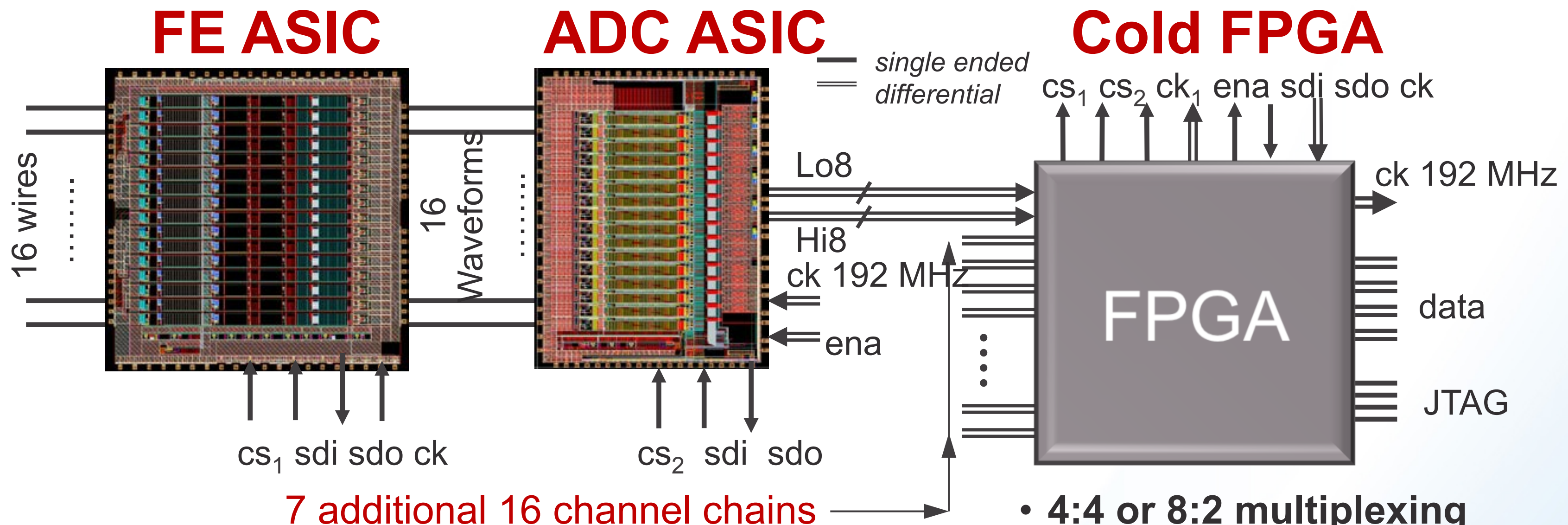
Key Components of Cold Electronics



- low-noise analog amplification
- programmable gain, shaping, coupling, …
- charge calibration over all chips, channels and temperatures to 1%

- ADC 12-bit 2MS/s
- small buffer
- 2 x **8:1 multiplexing**

- **4:4 or 8:2 multiplexing** (total 32:4 or 64:2)
- timestamp
- compression
- zero suppression
- neighbor triggering
- ***support non-reduction transparent mode***
- ***max output data rate 960Mbit/s or 1.92Gbit/s with overhead of 8B/10B***

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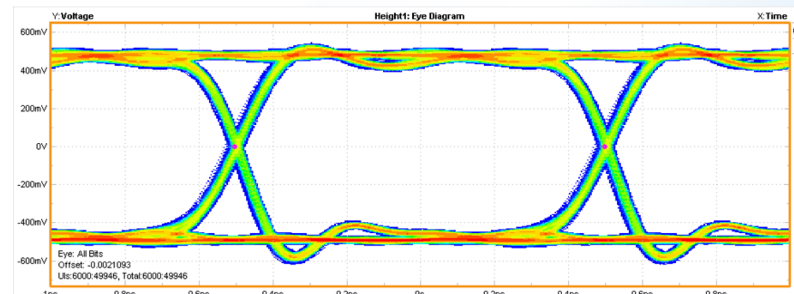
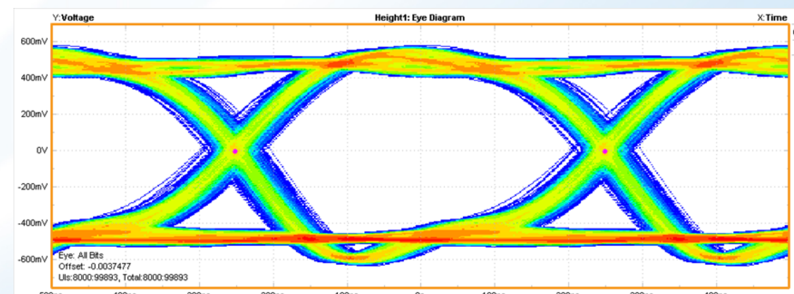
Cold FPGA Test

Vendor	Family	Technology	Speed of GTX [Gbps]	# of GTX	Memory [Mbit]	Core Voltage [V]	Status
ALTERA	Arria GX	90nm	3.125	4 - 12	1.2 - 4.5	1.2	Tested by BNL
ALTERA	Arria II	40nm	6.375	8 - 24	2.9 - 16.4	0.9	Tested by BNL
ALTERA	Stratix II GX	90nm	6.375	4 - 20	1.4 - 6.7	1.2	Tested by SMU
ALTERA	Cyclone IV E	60nm	N/A	N/A	0.3 - 3.9	1.0, 1.2	Tested by BNL
ALTERA	Cyclone IV GX	60nm	3.125	2 - 8	0.5 - 6.5	1.2	Being tested at BNL
ALTERA	Cyclone V GX	28nm	3.125	4 - 12	1.2 - 12.2	1.1	To be tested
XILINX	Virtex 5	65nm	6.5	0 - 24	0.9 - 18.6	1.0	To be tested

Cyclone IV GX Transceiver Starter Board



Eye Diagram @ 1Gbit/s



Eye Diagram @ 2Gbit/s

- **Test of Cyclone IV GX Transceiver Starter Board in LN_2**
  - **Transceiver works well at both 1Gbit/s and 2Gbit/s**
  - **JTAG configuration works**
  - **AS configuration works with Altera EPCS device**
  - **Internal memory works with SignalTap**
  - **Internal PLL and fabric work for clock generation**
  - **On board SRAM works with BIST**

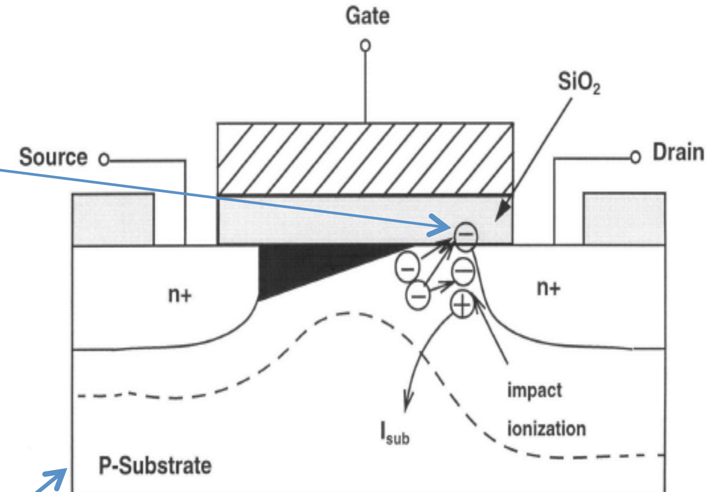
Impact Ionization and CMOS *Lifetime*

Chemistry slows down at 89K.

What is left of aging processes?

•***Impact ionization .*** Creation of *interface states* by (*some*) hot electrons causes a decrease in mobility, transconductance (gain), f_t, and a threshold shift.

• This limits the effective ***lifetime*** of the device at any temperature (defined in industry as *10% decrease in transconductance* g_m).

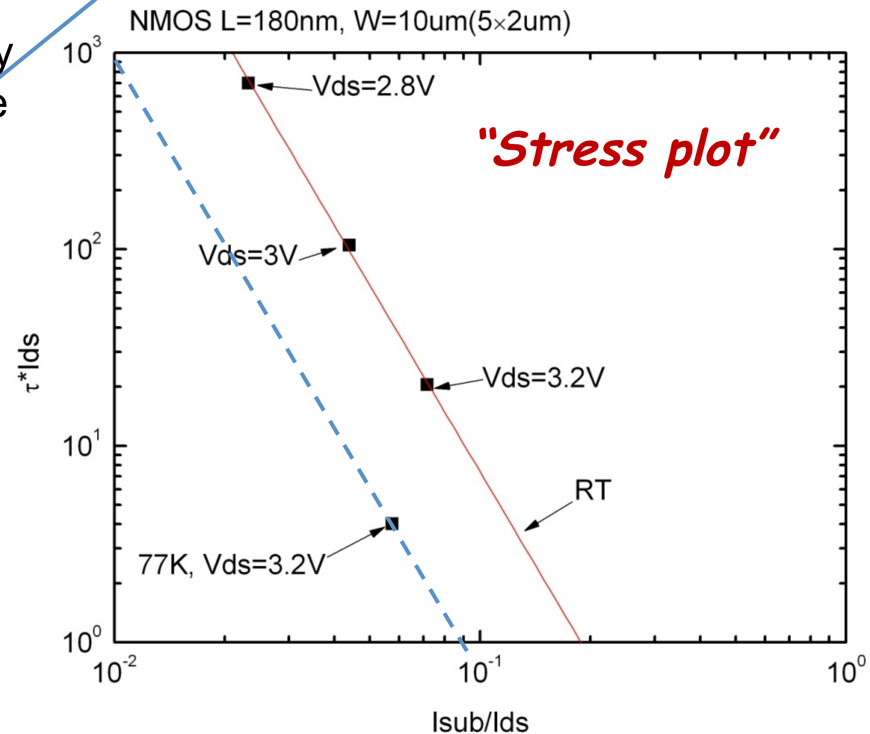


•***Accelerated lifetime testing*** is performed by stressing the device, at increased drain-source voltages and by measuring the ***substrate current*** (*a very sensitive quantitative indicator*) .

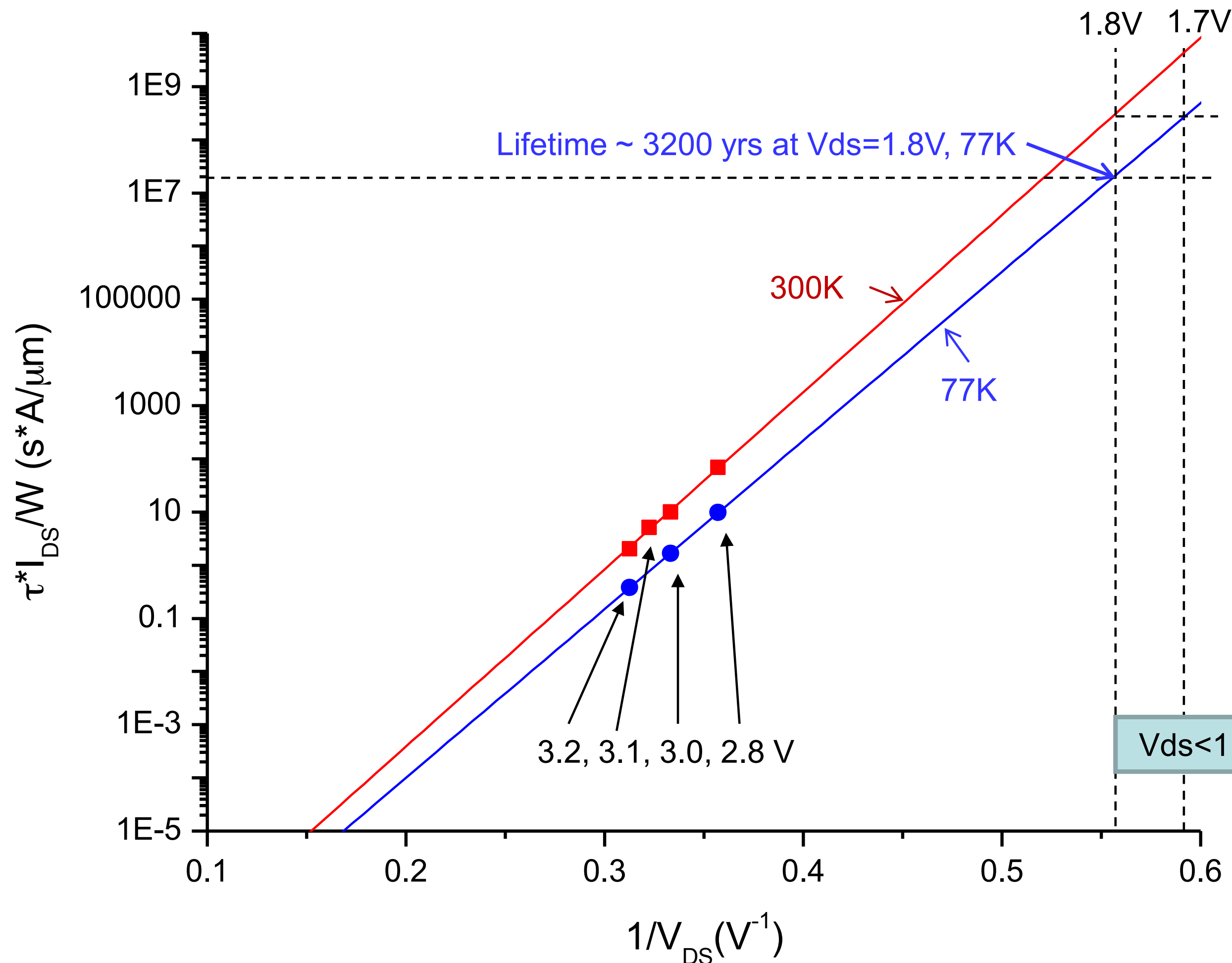
$$\tau I_{ds} \Big/ W \propto \frac{1}{\left(I_{sub} / I_{ds}\right)^a}$$

$$a = \varphi_{it} \Big/ \varphi_i \; ; \; 2.9 - 3.2$$

$$\varphi_i \; ; \; 1.3eV ; \varphi_{it} \; ; \; 3.7eV - 4.1eV$$



Lifetime *vs* $1/V_{ds}$ extracted from the stress measurements



$$\ln\left(\frac{\tau I_{ds}}{W}\right) \propto \frac{\varphi_{it}}{q\lambda E_m}$$

$$\propto \frac{1}{V_{ds} - V_{dsat}}$$

negligible for moderate/ weak inversion in low-power design.

Vds<1.8V

ASIC design: Vds<1.5V

NMOS L=180nm, W=10µm (5x2µm); nominal core voltage 1.8V. The projected lifetime at 300K is ~ an order of magnitude longer than at 77K. **Reducing V_{ds} at 77K by ~ 6% makes the lifetime equal to that at 300K. Design at low I_{ds}/W for longer lifetime.**

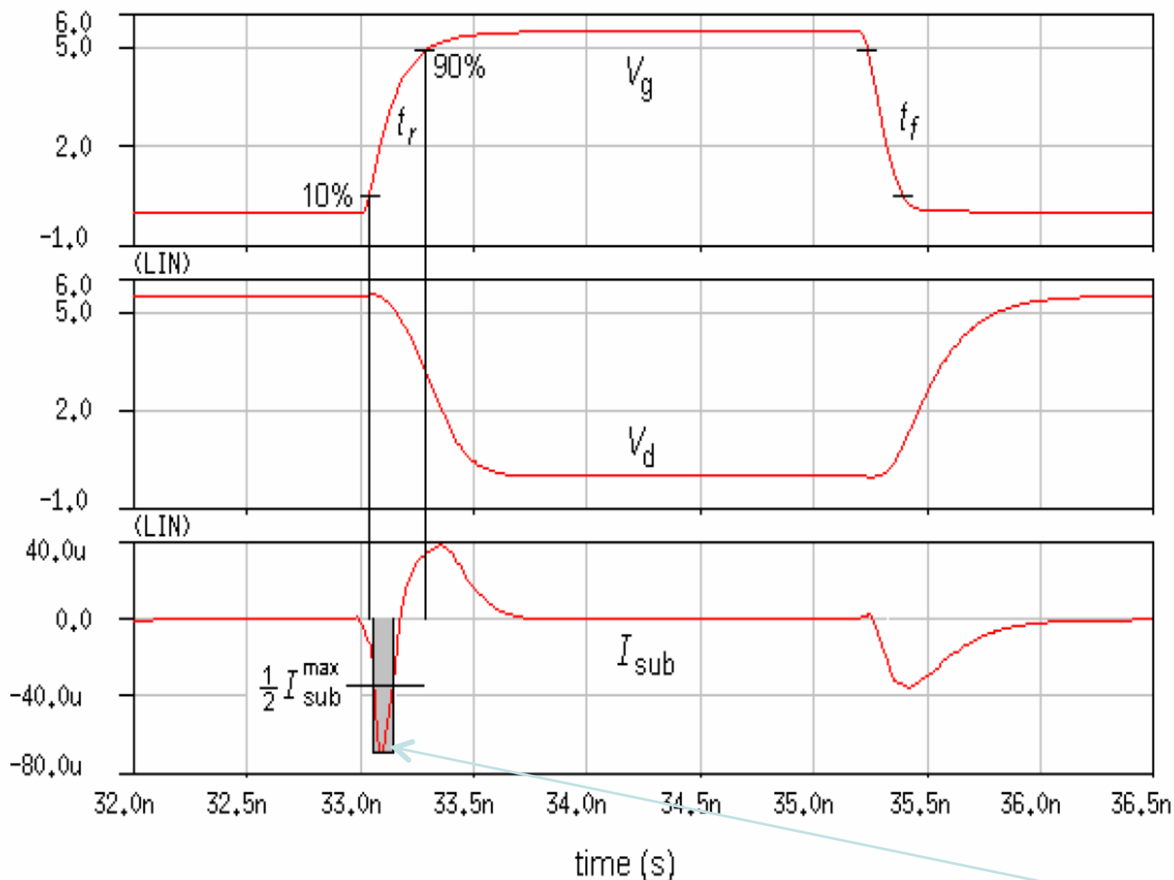
CMOS in *AC* operation: Logic Circuits and FPGAs

• It has been long established, e.g. Quader&Hu et al. (1994), that ***ac*** and ***dc*** hot-carrier induced degradation is the same if the ***effective stress time*** is taken into account. This quasi-static model, confirmed recently by White&Bernstein (2006), considers the ***ac*** *stress as a series of short* ***dc*** *stresses strung together*.

• The lifetime of a logic circuit driven at a clock frequency can be related to the lifetime of the NMOS transistor under continuous ***ac*** operation in terms of the ratio of the effective stress time during a change of state and the clock period. Thus the *lifetime of digital circuits (**ac** operation) is extended by the inverse duty factor* $4/(f_{clock}t_{rise})$ *, compared to **dc** operation.* This factor is large (>100) for deep submicron technology and clock frequencies needed for LAr TPC readout.

• Design guidelines for digital circuits and FPGAs: *Keep the inverse duty factor high*. As a an additional conservative measure, reducing V_{ds} *by 10%* adds an order of magnitude margin to the lifetime.

Effective Stress Time is a small fraction of the *Clock Cycle:*



$$\left[\frac{ac\ stress\ time}{dc\ stress\ time}\right] \approx \left(f_{clock} t_{rise}\right) / 4$$

Standard method for accelerated stress testing of FPGAs: ***observe ring oscillator frequency under severe V_{ds} stress (Wang et al. 2006)***

(Degradation of I_{ds} leads to increased rise (propagation) time and reduced ring oscillator frequency.)

Hot-carrier induced degradation occurs only when the *substrate current* is high, i.e., nominal V_{ds} and high I_{ds}.

Summary

- **Cold electronics installed close to the detector elements is critical to make possible giant LAr TPCs and improve signal to noise ratio**
- **CMOS at Low Temperature**
  - **Started from .18um CMOS technology with only 300K models for analog front end; parameters extracted at 77K**
  - **CMOS found functioning at cryogenic temperature with *increased* gain (g_m/I_{ds}) and *lower* noise**
- **Development of Cold Electronics for LAr TPC**
  - **The CMOS analog FE ASICs equipped mother boards are being tested for final production of MicroBooNE experiment**
  - **We have accumulated *~1500 chip•immersions* in LN_2 without any failures due to thermal contraction/expansion**
  - **ADC characterization test and cold FPGA lifetime study are being conducted**
  - **Analog FE ASIC + ADC ASIC + Cold FPGA will be used to equip the 35 Ton LAr TPC**