MicroBooNE DAQ

Eric Church, Yale

CPAD LArTPC Meeting

20,21-March-2013

Outline

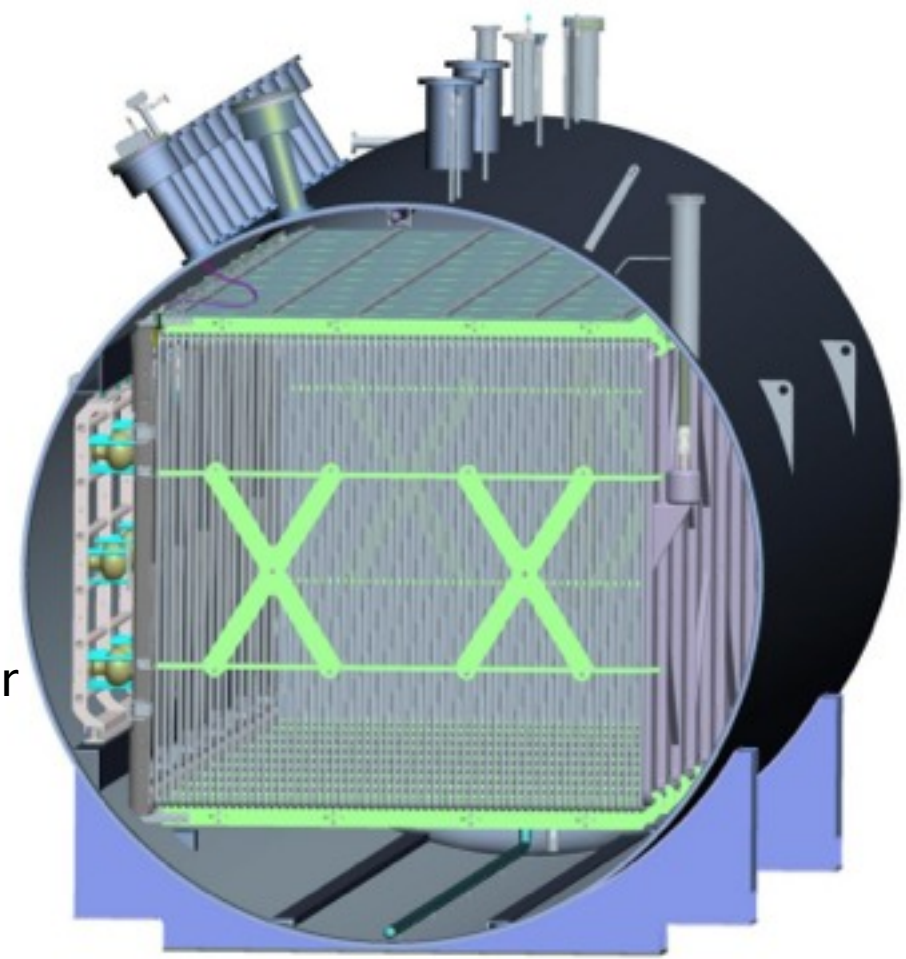
- Overview
- MicroBooNE DAQ Teststands
  - People/Institutions
- MicroBooNE DAQ System Overview
- System Components at DAB Teststand
- Progress so far
- Ongoing Work: stuff we're still building
- Charge Injection Calibration
- Summary and Outlook

MicroBooNE Status

- CD3b March, 2012.
- CD4 in Summer, 2014
  - MicroBooNE collaboration and project hope to be ready earlier.
- Electronics Reception Tests will test out much of the full DAQ and its moving parts starting mid-May!

MicroBooNE instrumentation

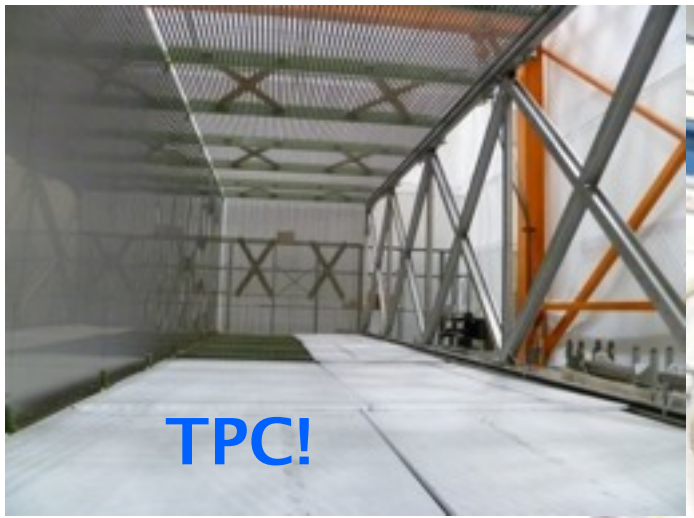
- 8256 wire channels
- 30 PMTs



data on Wires are the projections in 3 views. Allows reconstructing back to 3D tracks and showers.

PMT data to trigger, to determine t0 for cosmics subtraction, and perhaps late/early light for pID.

MicroBooNE TPC/Cryostat pictures

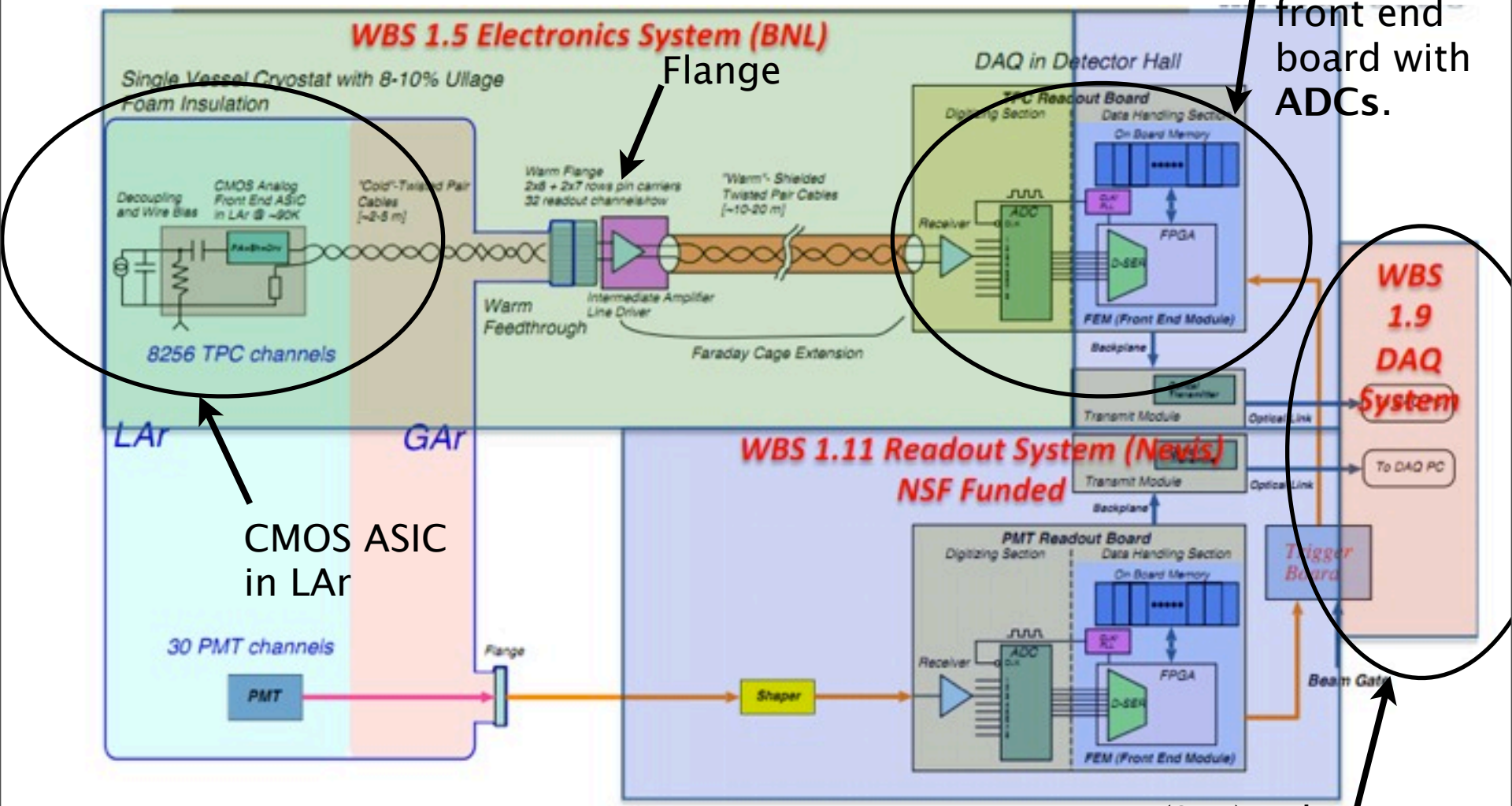


TPC!

Cryostat!

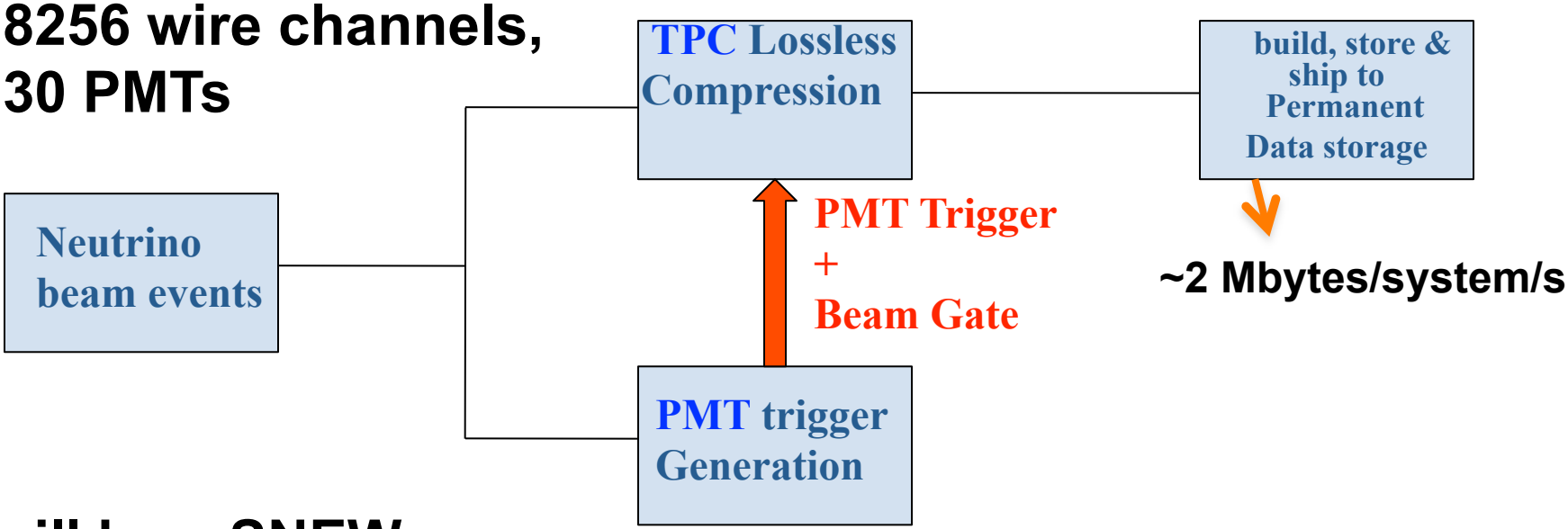
No longer so abstract.

System Overview



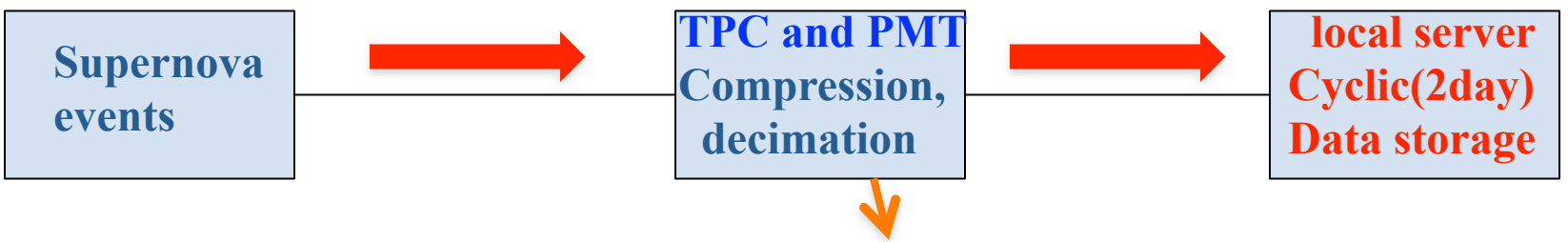
Digitizing Boards: MicroBooNE design

8256 wire channels, 30 PMTs



We will be a SNEWs *consumer*.

Continuous TPC and PMT readout



Use the SN data stream to select and study K background events

2 data streams

- Beam physics: triggered stream
  - confirm/refute/dispute miniBooNE BNB sub-500 MeV excess
  - x-sections in Argon
  - But also: NuMI events
  - Laser calibrations
  - “Strobe” events
- non-Beam physics: Supernova stream
  - Every single 1.6 msec frame, one after the other
  - Will fill seven 2 TB disks in two days on each crate.
  - GPS time of event will allow to dig through and recover 1-2 hrs around the candidate SN, as reported from SNEWS
  - non-trivial disk-read, network-heavy task.
    - data moving, reaping; other bkgd processes always running

Resources

- Work on the DAQ is ongoing at Nevis/FNAL through 2013. Moving to LArTF (MicroBooNE enclosure), we hope, end of 2013.

- The MicroBooNE DAQ team is comprised of the following institutions :
  - Yale, LANL, FNAL, Nevis/Columbia, Va Tech, KSU, MIT, UT-Austin

D0 (DAB) and Nevis Teststands

- This talk will mostly focus on the DAB (D0 Assembly Building) teststand, on which the MicroBooNE DAQ team is developing the DAQ.

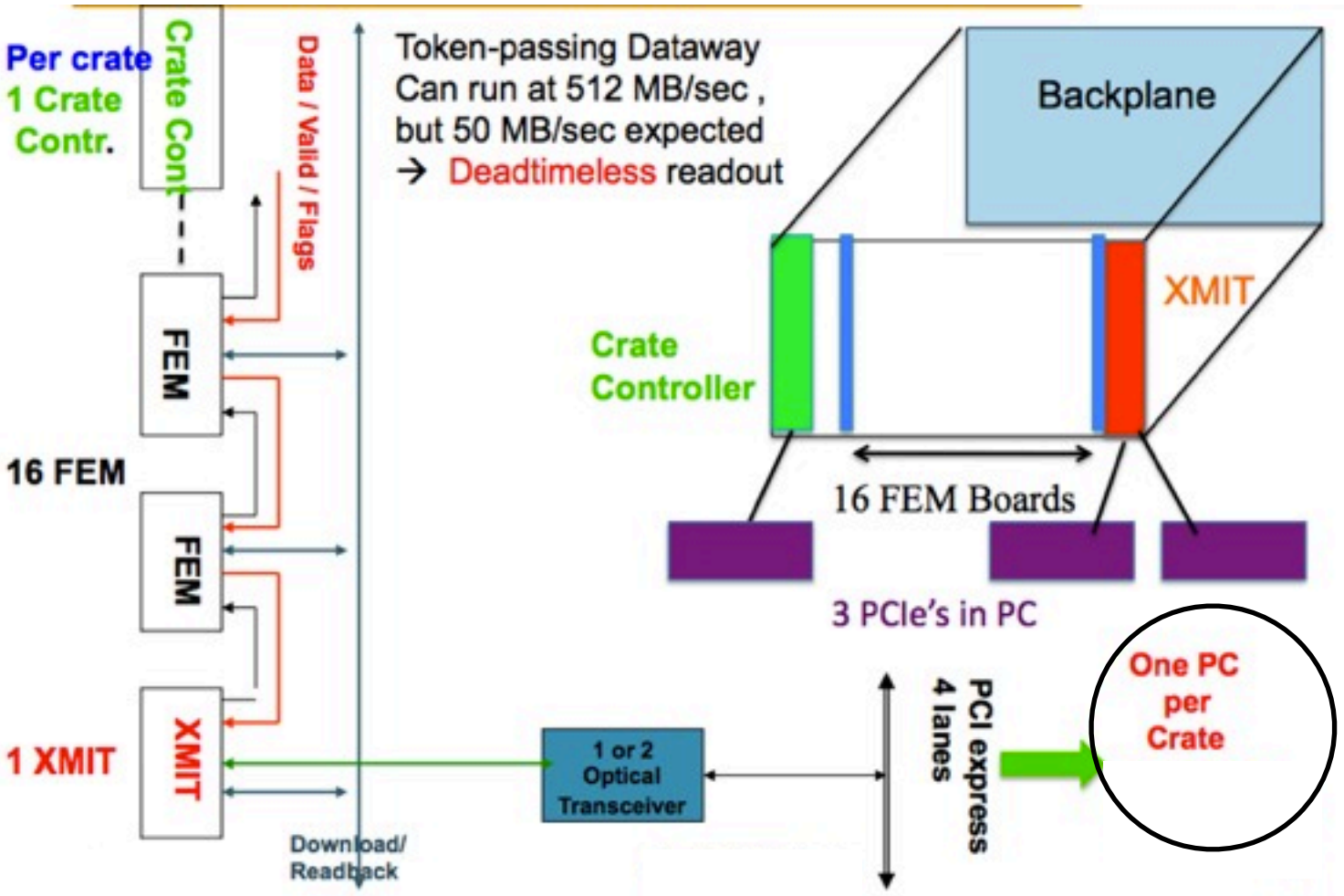
- Nevis runs its own test stand, where they run code and pass readout knowledge to us. And also, where they perform characterization of the electronics as it is fabricated and shipped to them.

Other uB-related Test Stands

- BNL maintains a front-end electronics test stand at which they test ASICS, motherboards, pre-amps, intermediate amplifiers, ...

- There is a Test Stand at PAB at FNAL that reads out PMTs in actual liquid argon.
  - No wires, no E-field, reading out through Controller Card.
  - They are reading PMTs, and fitting to early/late light components
  - Doing dE/dx studies with an alpha source
  - Nitrogen impurity measurement
  - Shaking out PMT DAQ components, generally

Nevis TPC Crates (x9)



Wires are sampled@2MHz, 2 bytes

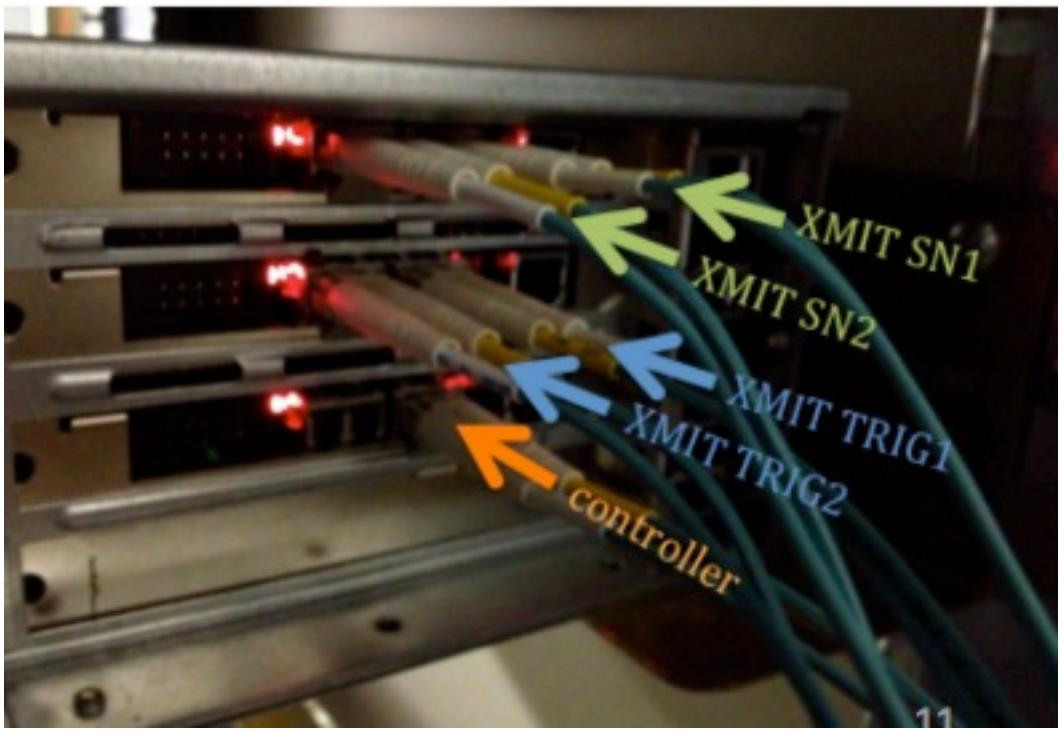
Fibers into SEB-computers

SEB == Sub Event Buffer <==> basically one crate.

One SEB computer services one crate.

There are two data streams.
(1) Triggered
(2) Supernova:
continuous stream

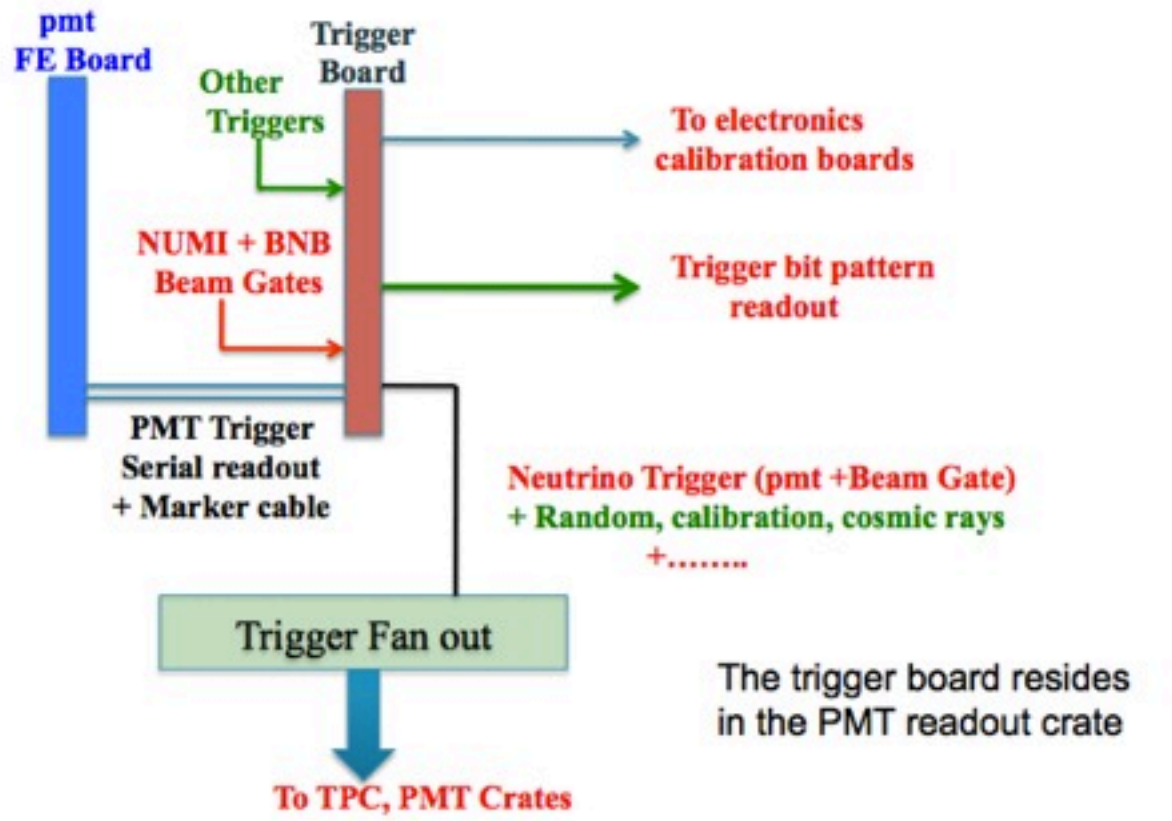
Both come through the "XMIT" card on duplex fibres.



Three NEVIS custom PCIe cards per SEB.

Nevis Trigger Crate

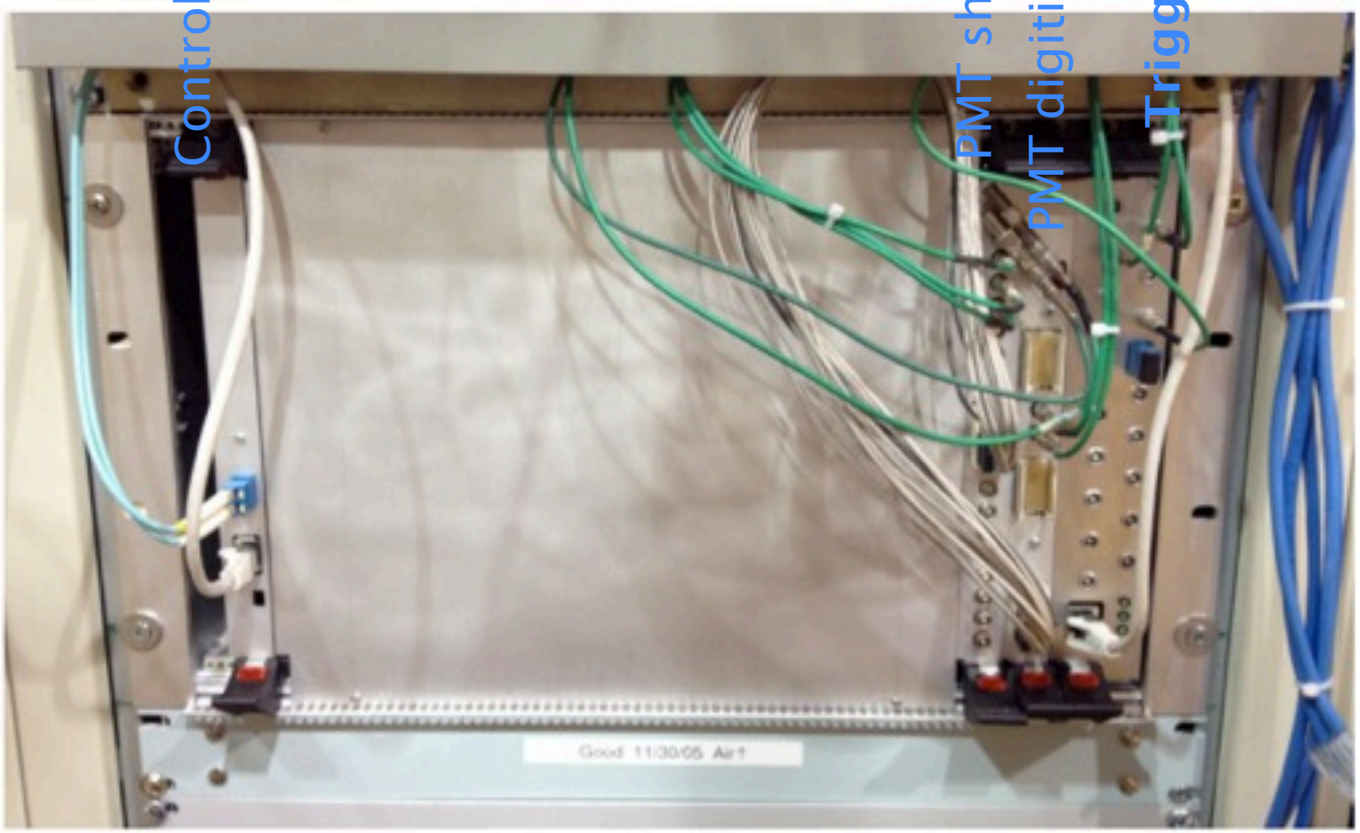
Overview: Trigger scheme



The trigger board resides in the PMT readout crate

PAB Teststand

Special, Trigger/PMT crate



PMTs sampled@64MHz, 2bytes

Figure 2: PMT Crate Physical Setup (as of Oct. 10, 2012)

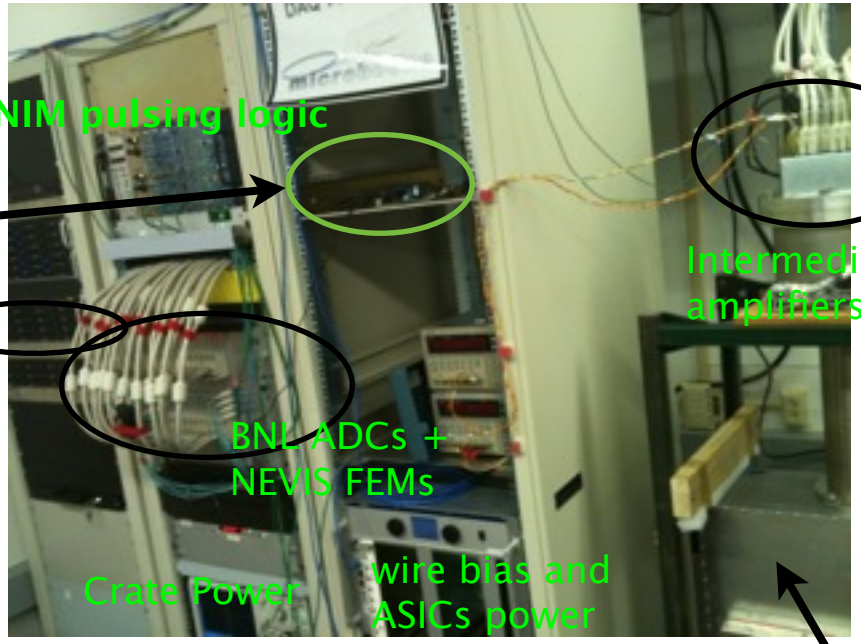
Overview of DAQ Project

- The MicroBooNE DAQ is responsible for reading out, assembling events, writing them to file.
- But also:
  - Monitoring and Control,
  - Beam data concatenation,
  - Run stop/start: State Machine
  - Calibration runs, Laser Runs, ...
  - Online and Nearline processes,
  - File management, ...

The MicroBooNE DAQ writ small: the DAB TestStand

- BNL: ASICs through ADC

uboonedaq-seb-01.fnal.gov



- Nevis readout:
  - Crate cards through PCIec ards
- DAQ: computers, software, glue

Technical Progress

- Glomation SBC as the slow mon/control hub: one per rack.
- ACNET data, file management will come from supported CD IF Data Logging project and CD Enstore/ Sam solutions, respectively
- Readout established
- State Machine Built, Message Passing working
- Code build specified
  - We have a very extensible model: ups'es where possible, git repository, CMake build system, C++ codebase

Technical Progress, contd

- EPICs IOCs (Input/Output controllers) accessing shared memory already demonstrated. SMNP to control/monitor most power supplies and monitor computer environment variables.
- Online data health via Ganglia: very powerful http-served monitoring tool.
  - JSON plots, ala finance.google.com, etc
  - Easily scaled and intuitive
  - Simple definition of the metric in the code. Time-series chart appears, nicely laid out. Layout is easily configurable.

Ganglia

Custom Metrics

For Online Monitoring of raw system, and also stuffed at the ~1Hz level into EPICS slowmon dB

Trig DMA Rate

Assem -bler write Rate

SN DMA Rate

Status of Work: recent accomplishments

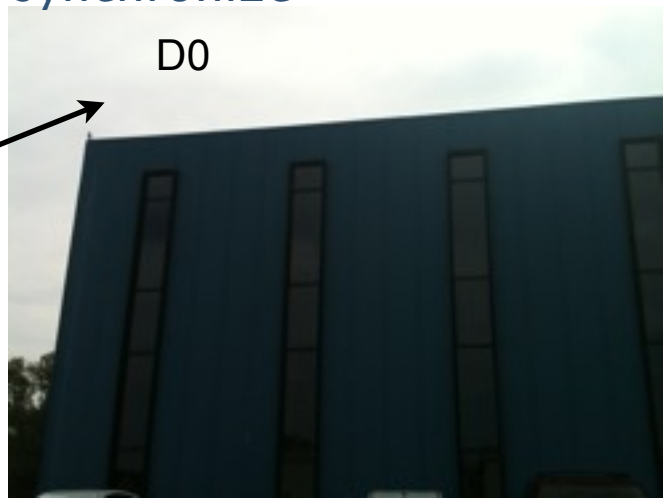
- Event building done so far with uBooNE-specific DMA'd data files. A full, detailed fake data transport mode completed.
  - it remains to exercise this on multiple actual crates, live -- Fall, 2013.
- Serialized/archived output data format defined. In a boost::serialized class
  - "serialized", "archived" meaning data laid out in order, with versioning that makes everything backward compatible as code evolves
  - Methods to write out binary chunks into file and read it back and unwind it to level desired

GPS

- Absolute time into header: GPS card
  - Code in place to allow Pulse Per Second (PPS) interrupt to capture/synchronize DAQ clock to GPS.

In progress

D0



This $3k Symmetricom PCIe card advertises 170 nsec accuracy.

Trigger card stores the DAQ clock value on each GPS Pulse Per Second input. We then will grab that value and the GPS time and shove it into the trigger data header. Will propagate to the overall global header from there. All code already written.

PCIe card works with new antenna, driver, code.

Status of Work: things in progress 2

- Processes for Nearline monitoring (LArSoft)
  - Swizzle from RawData into ARTDAQ (LArSoft) format.
- EPICS, ongoing
  - Server imminently to be installed on its machine,
  - Alarming, Archiving, Control/Display GUI
    - Being written now
  - IOCs reporting all data on list to EPICS dB
- Understanding nuance of Readout and FEM FPGA code ...

Status of Work: done!

- Message Passing System to effect State Machine transitions: Configure, Connect, Run, Pause, Configure, Run, Stop, etc.
  - Code does not just fall through. This is a crucial step of sophistication that allows multi-mode running
  - Done.
  - Now ready for Calibration runs: we want to run the special calibration trigger and configure hardware and pulse/read Nx100 times all within N unambiguously labeled runs with subruns: Pause, Re-config hardware, pulse/read, Pause, etc.

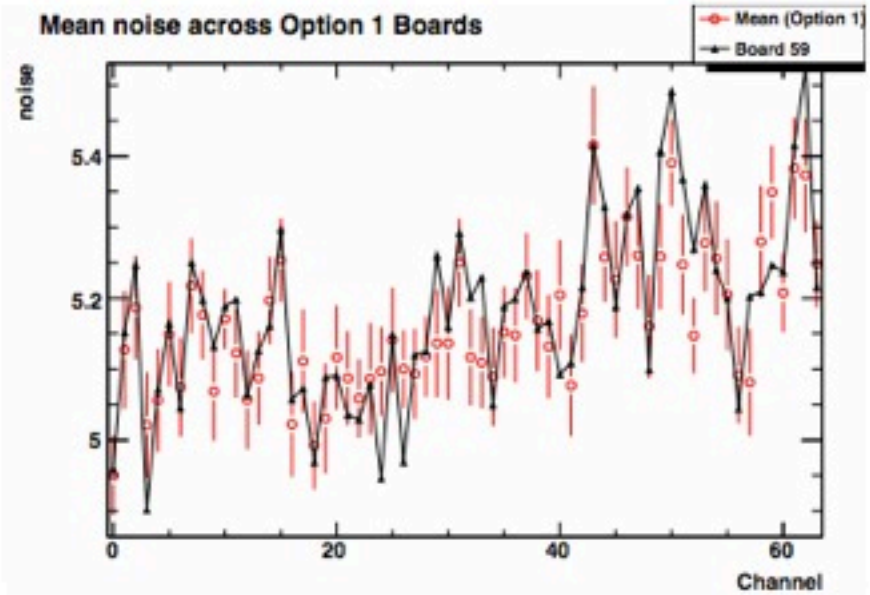
Test Stands through 2013

- The Test Stand at DAB at FNAL will serve as an acceptance test station before buttoning-up, when/as all of the electronics boards are shipped to FNAL.

- 4-phase plan to test all Front End channels
  - walk through crates with test flange
  - walk through again, changing cold cable
  - walk through, on real Cryostat flanges
  - do it again after cap is welded back on!

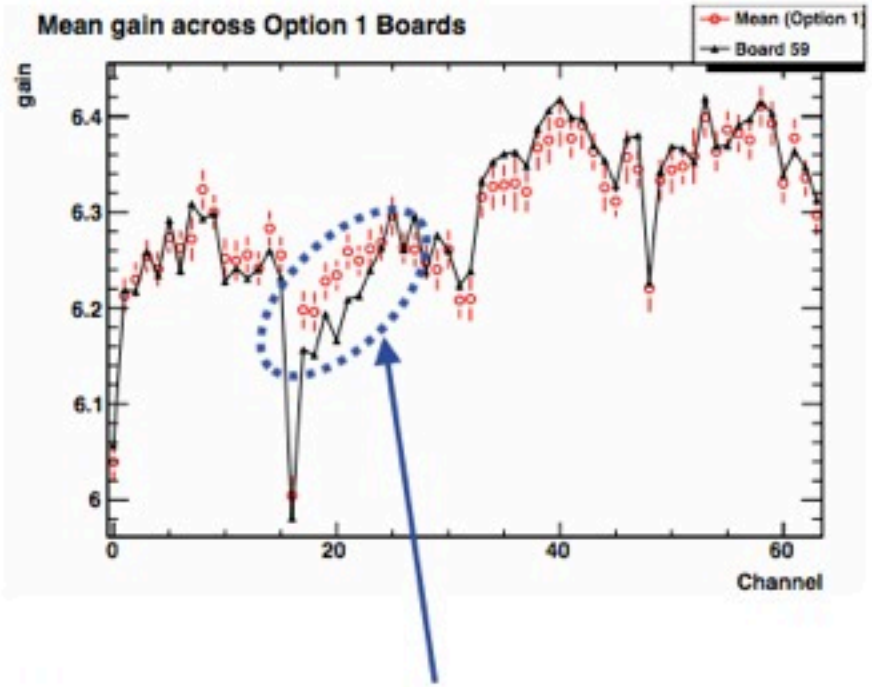
Electronics testing at BNL

ADC pedestals from reading signals with no input pulse.



Noise looks OK.

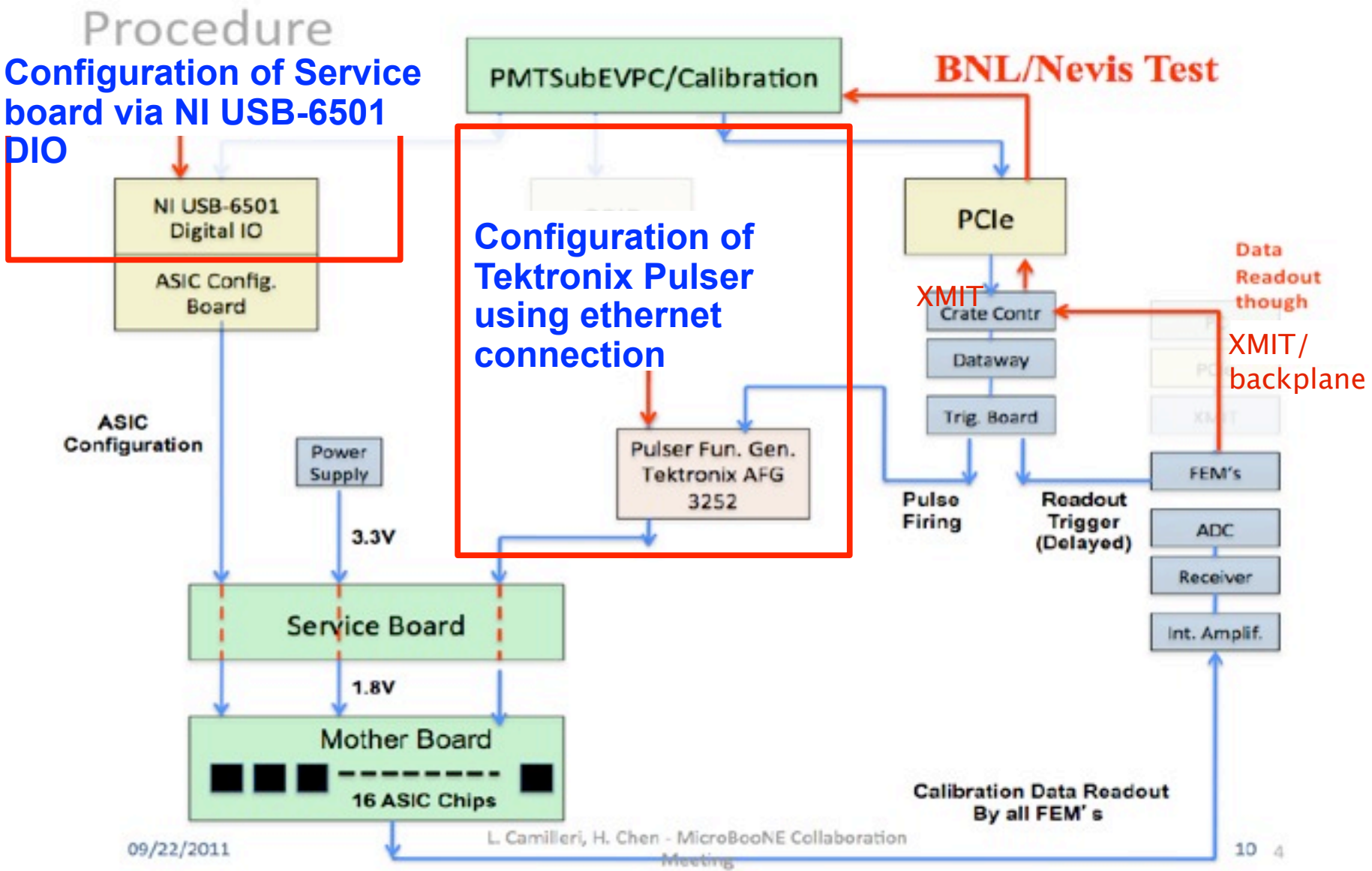
Calculated by pulsing multiple times at N~8 input amplitudes.



Gain in some channels significantly low.

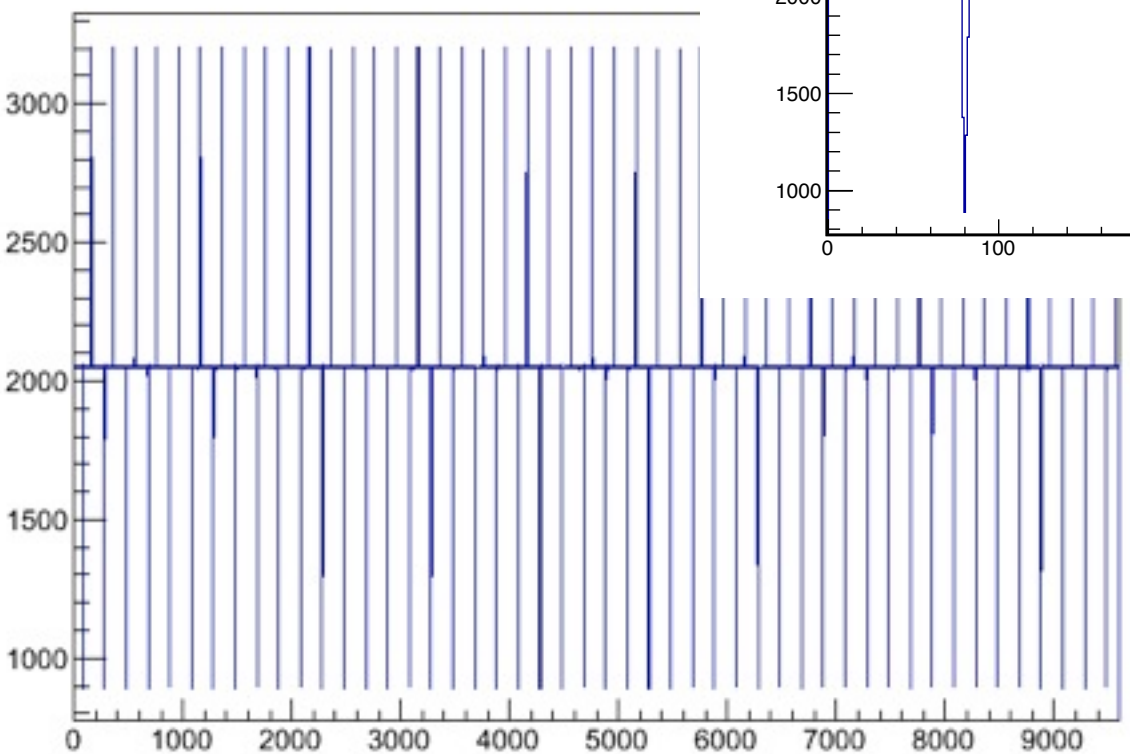
Wes Ketchum and Sarah Lockwitz

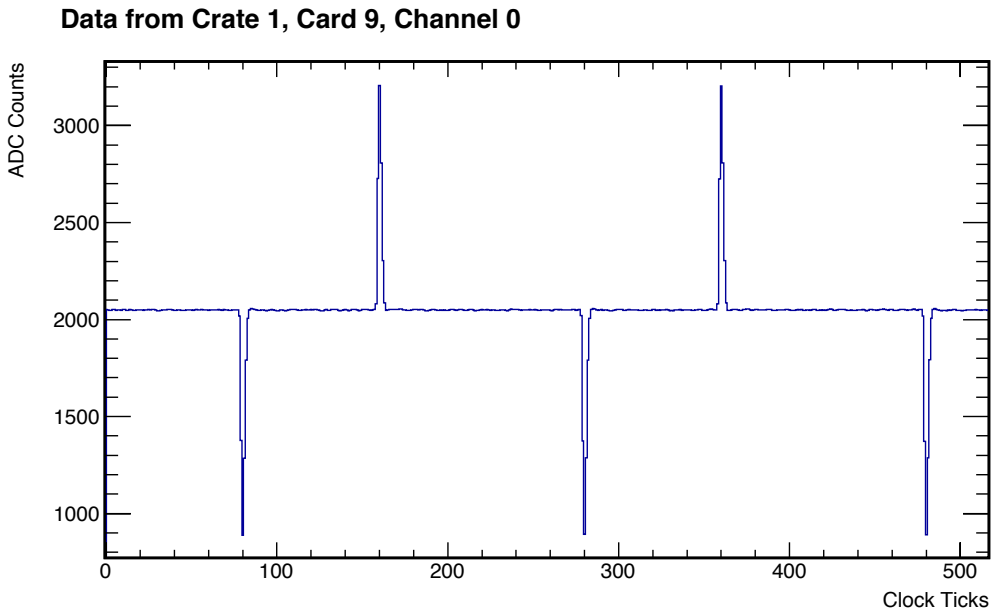
Calibration Hardware



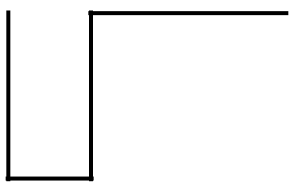
Calibration Run: we've done it

Continuous Pulse. Needs to be Burst





The input signal is 10 kHz.
It is a negative-, then positive-going square-wave signal, of width 40 usec.



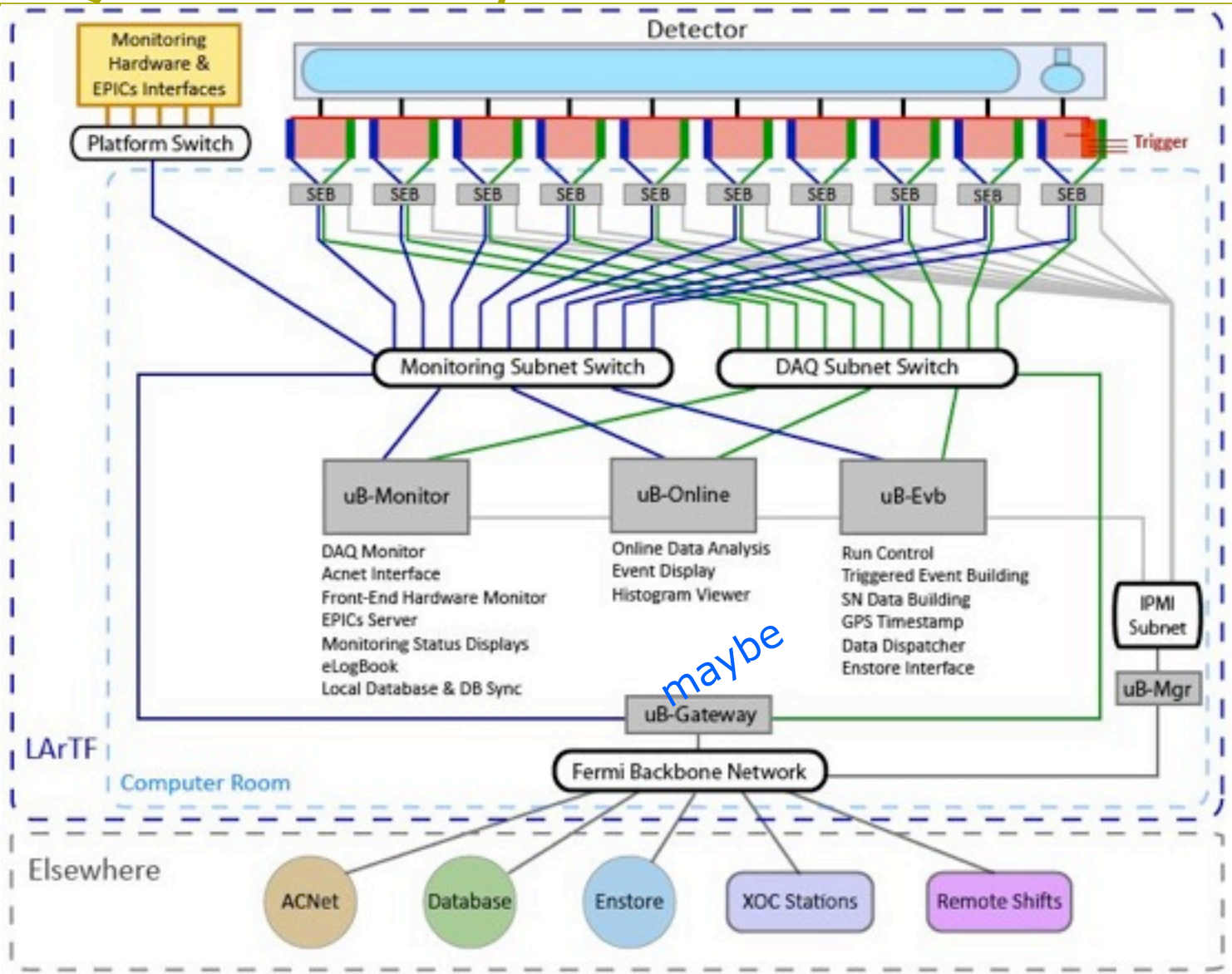
Full 3x1.6msec frame read-out.

Summary

- All the DAQ moving parts are accounted for and in mature development or complete.
- PO's going out for computers/switches, sundry hardware now.
- (Will be) Ready for turn-on and data-taking in 2014
- Exciting times for MicroBooNE!

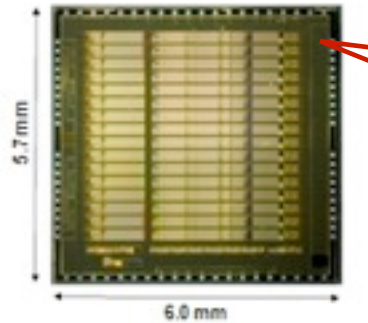
Backup Slides

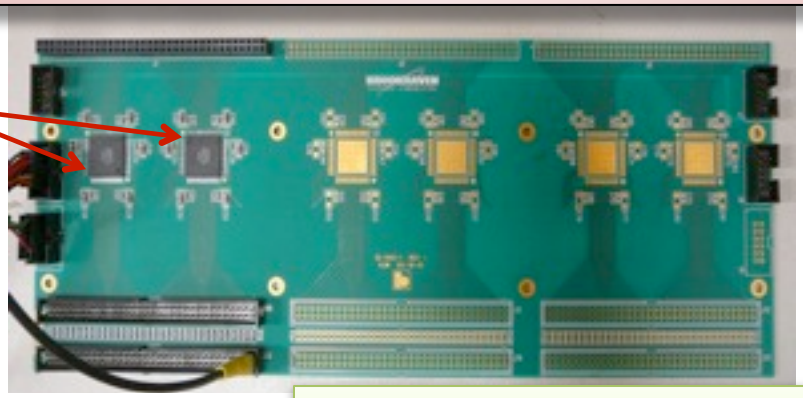
DAQ Network/Process Overview



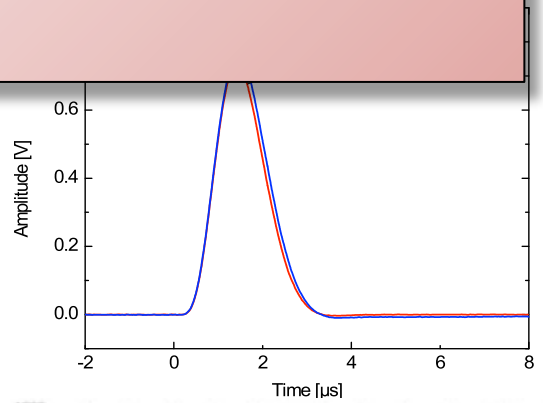
Cold CMOS Analog Front End ASIC & Motherboard

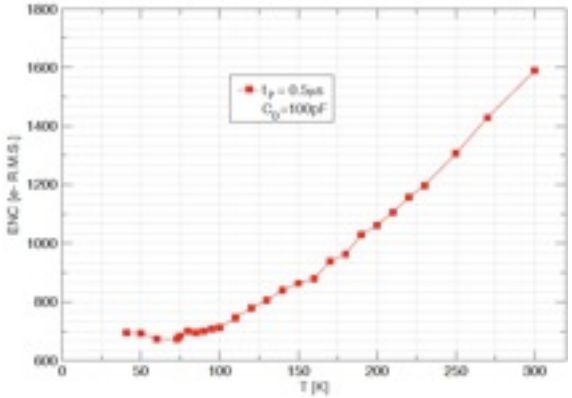
ASIC die & package



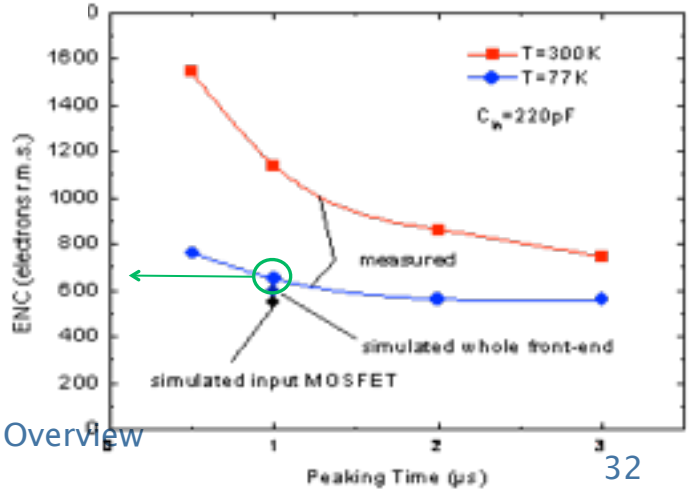


Cold motherboard with 12 ASICs chips (2 shown)



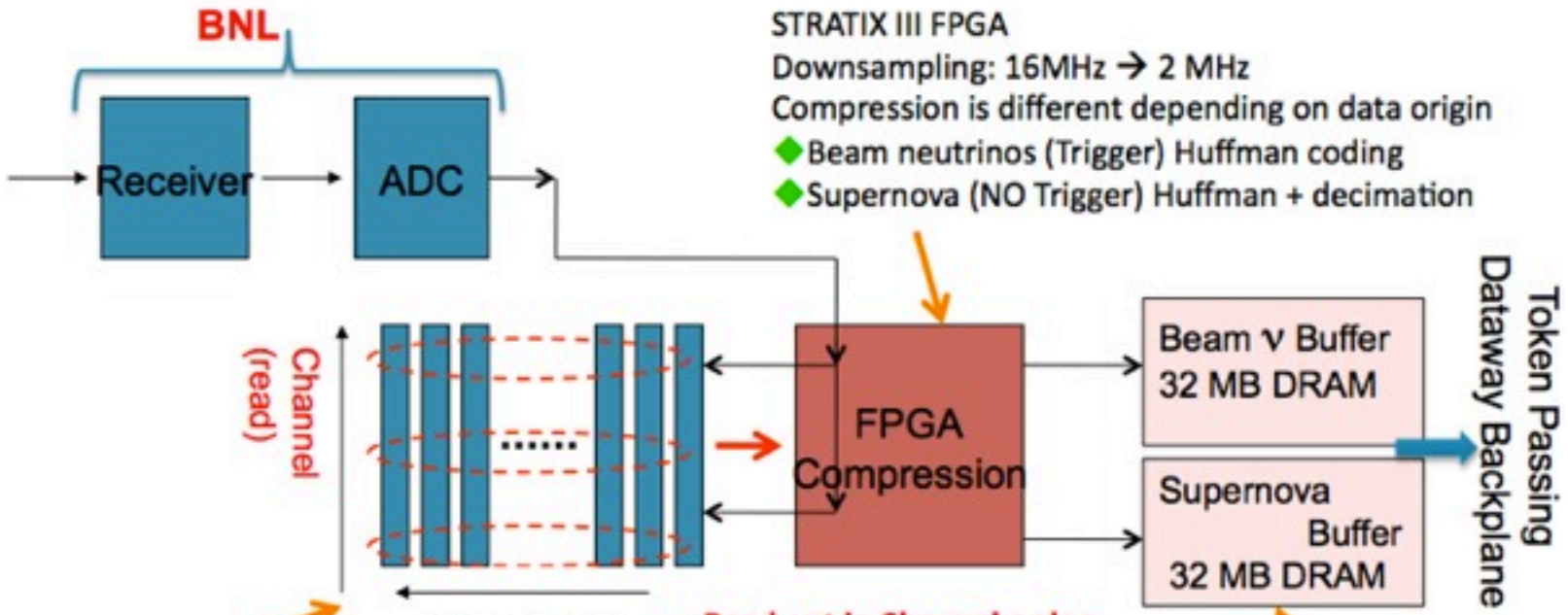


- 16 channels per chip
- Charge amplifier, high-order filter
- Adjustable gain: 4.7, 7.8, 14, 25 mV/fC (55, 100, 180, 300 fC)
- Adjustable filter time constant (peaking time): 0.5, 1, 2, 3 µs
- Selectable dc/ac (100 µs) coupling
- 136 registers with digital interface
- 5.5 mW/channel (input MOSFET 3.6 mW)
- Designed for long cryo-lifetime
- Circuit performance is almost identical at 300K and 77K, except noise is ~2x lower
- Calibration capacitor on ASIC changes by ~0.5% from 300K to 77K
- **Cycle #4* chips: Passed all tests**

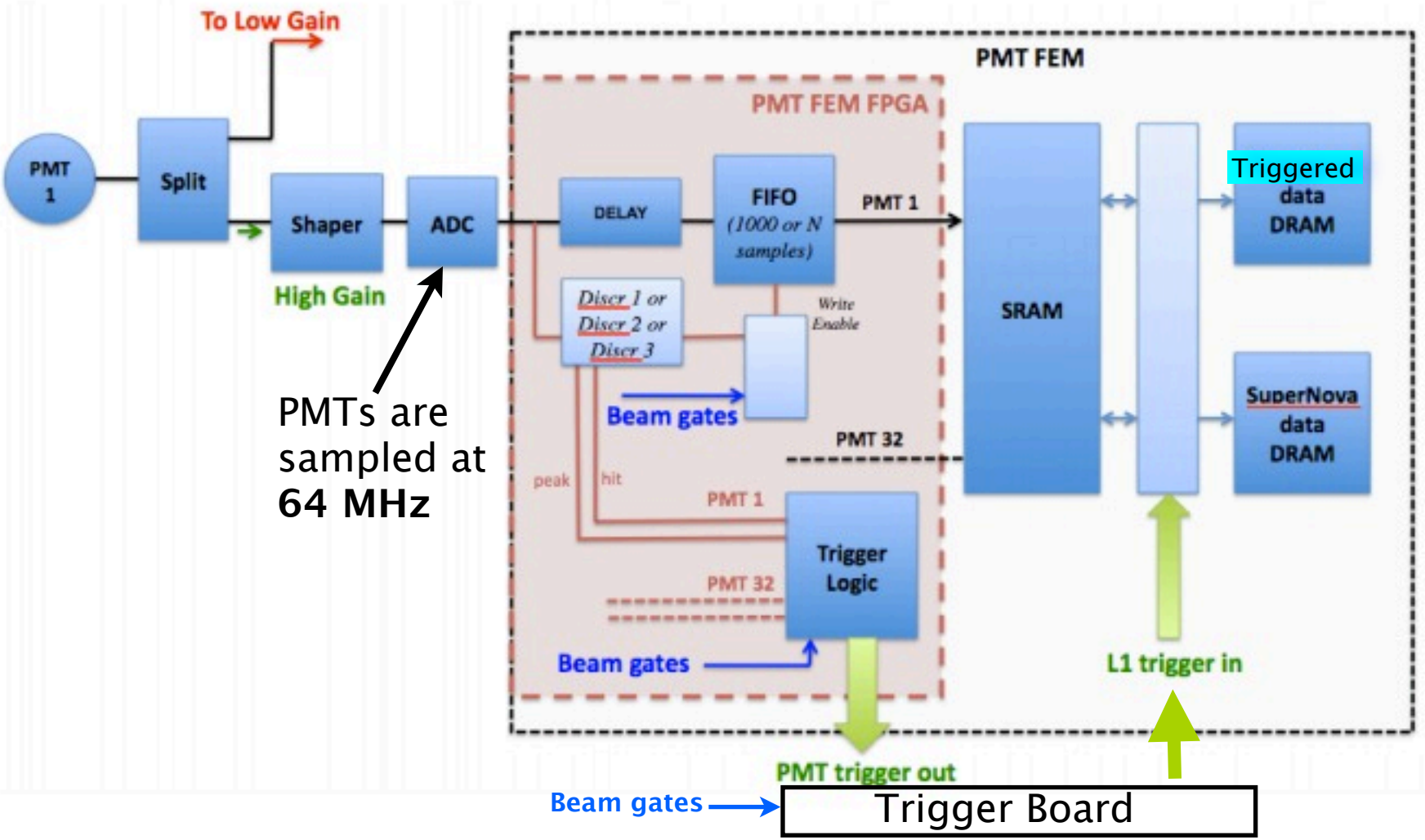


Overview: Digitizing Boards: Hardware and Tasks

Continuous Data rate per card: 64 wires x 2 MHz = 128 MHz 12 bit ADC words.



Trigger


To Low Gain
PMT 1
Split
Shaper
ADC
High Gain
PMTs are sampled at 64 MHz
PMT FEM
PMT FEM FPGA
DELAY
FIFO (1000 or N samples)
PMT 1
Discr 1 or Discr 2 or Discr 3
Write Enable
Beam gates
PMT 32
peak
hit
PMT 1
PMT 32
Trigger Logic
Beam gates
SRAM
Triggered data DRAM
SuperNova data DRAM
L1 trigger in
PMT trigger out
Beam gates
Trigger Board

BNL Nevis Electronics status

- Motherboard production fabrication starting next week. Received at BNL by end of March.
- ADC boards shipped now to NEVIS.
- Then, to FNAL::DAB
- Into Racks in Spring

Nevis Status

- We now have >90% of boards in hand (from assembler):
  - All FEMs
  - All XMITs
  - All clock cards
  - All Controllers
  - All PMT shapers

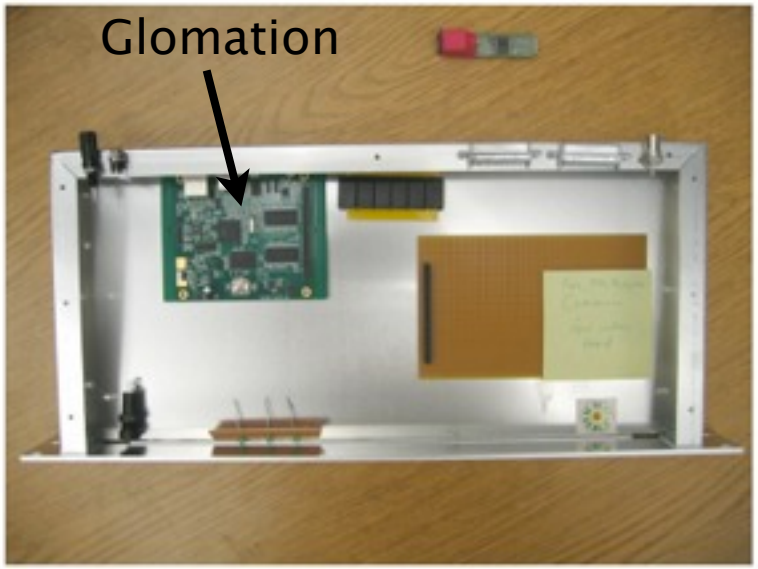
BNL fabrication and testing

These are so-called Cycle 4* ASICs. Final Cycle.

- CMOS Analog Front End ASIC
  - ASICs were delivered in early December
  - ASIC incoming test is ~~ongoing~~ done at room temperature
    - 593 ASICs have been tested, 529 ASICs passed the test
    - Yield is ~89.2%
  - ASIC cold screening test is finished
    - 201 ASICs have been tested in LN_2, 195 ASICs passed the test
    - Very stringent criteria to screen chips in LN_2, for 6 chips that did not pass the test
      - 4 chips: each has a channel with slightly a reduced dynamic range
      - 2 chips: each has a channel with a slightly larger undershoot
    - **Cold/Warm Yield** is ~97%

Glomation Single Board Computer GESBC-9G20

- SBC includes
  - Linux OS
  - Ethernet
  - RS232
  - USB
  - 40 digital I/O
  - 4 ADC
  - I2C and SPI bus



- Interfaces directly with
  - **Glassman Drift HV – RS232**
  - **Rack Temperature – I2C bus using Maxim DS1624**
  - **Rack Fanpack – digital I/O**

Glenn Horton-Smith, KSU