eFPGAs for Advanced Detector Readout

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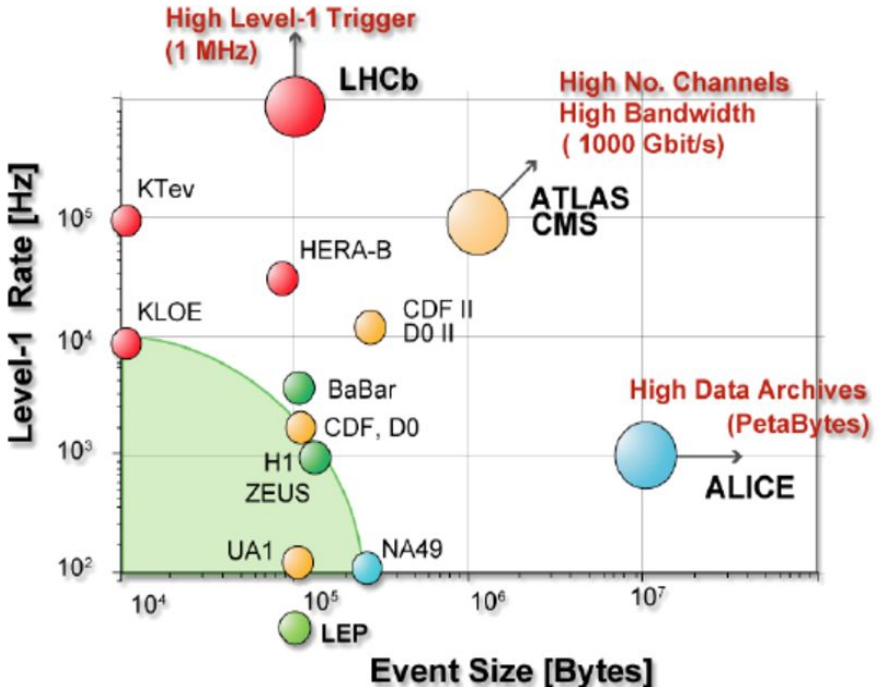
BERKELEY LAB

Motivation from HEP

- Detectors at future energy frontier colliders (EIC, FCC, muC) will need to accommodate a variety of unique challenges:
  - High granularity → *high data rate*
  - Spatial constraints → *low material budget, low power consumption*
  - High radiation dose → *custom front-end electronics design*

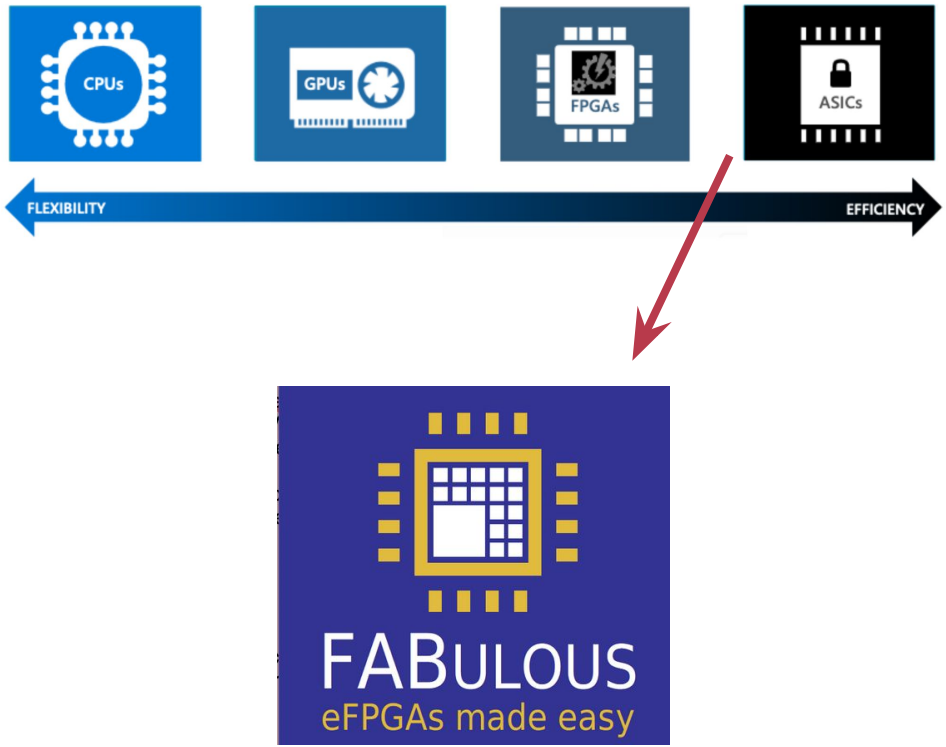
- Transmission of data off the detector is often less efficient than data processing → push data processing close to the front-end

- **Custom AI/ML-based front-end can provide intelligent filtering or featurization of data at-source,** to handle highly granular detectors, high pileup, and/or increased signal efficiency



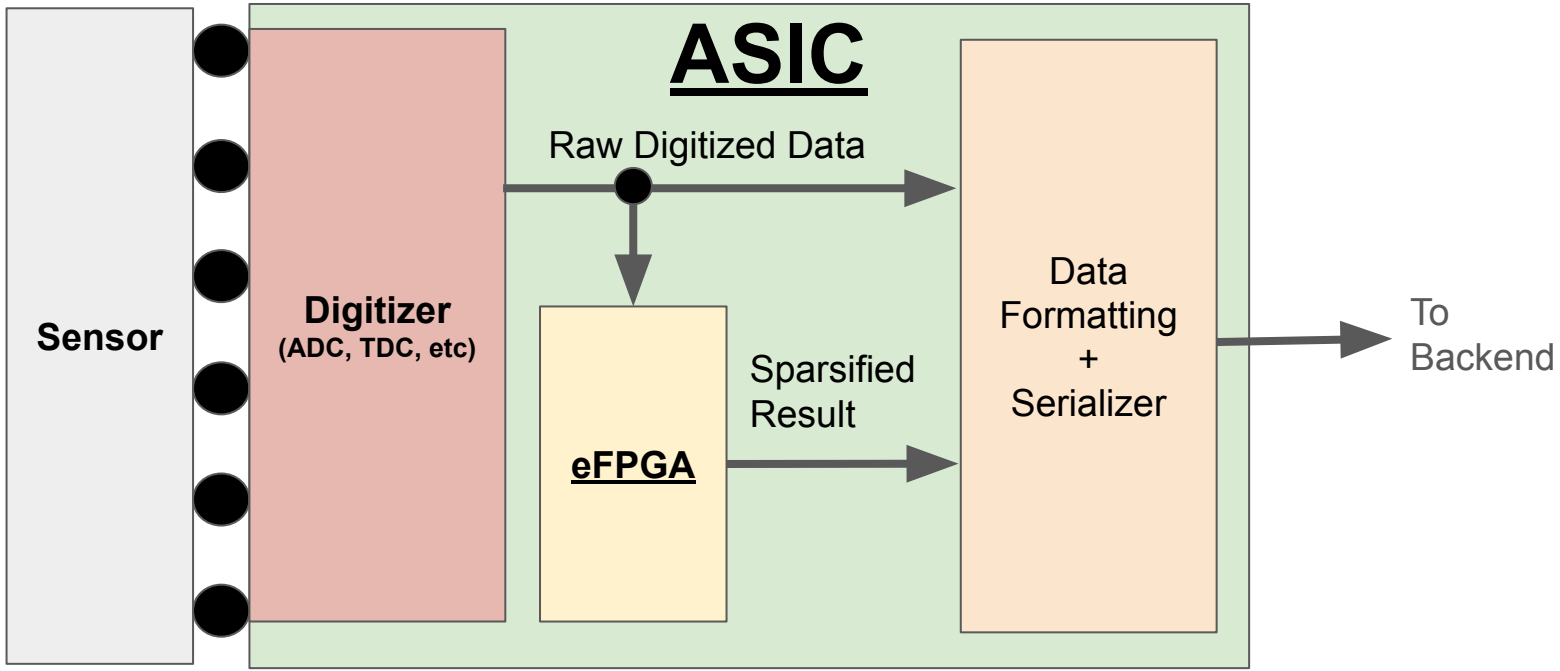
Why eFPGAs for HEP-ML?

- Embedded FPGA (eFPGA) technology can offer reconfigurable logic within an ASIC
  - Low latency to the data after digitization
  - Ease of FPGA configurability on an ASIC: *crucial for dynamic data-taking application*
- Several popular FPGA architectures are over 20+ years old
  - **Original patents have expired**
  - Includes Spartan-3 and Virtex-II FPGAs from AMD/Xilinx
- **→ Open source framework "FABulous" available for eFPGA design**
  - Lowers barrier to entry for chip design



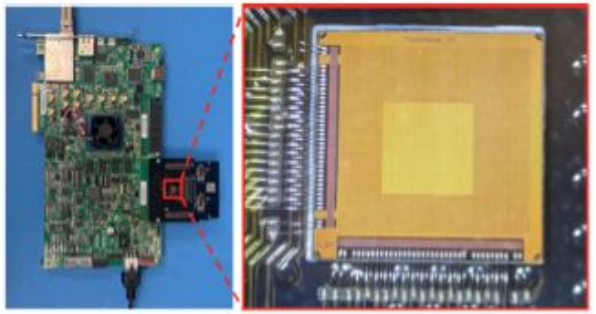
https://fabulous.readthedocs.io/en/latest/

eFPGA in the Front End: Simplified Concept Drawing



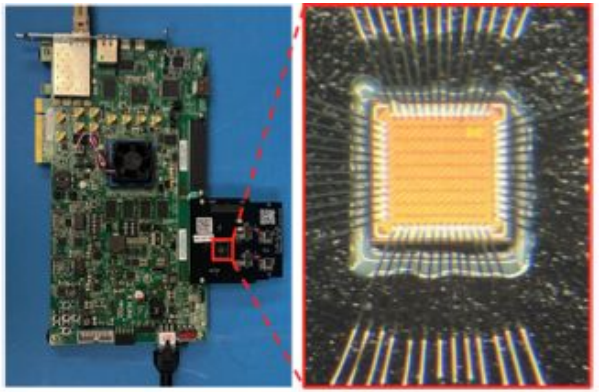
Current eFPGA Prototypes Efforts

- SLAC tapped out two eFPGAs designed with **FABulous** framework
  - 130nm & 28nm:
    - 8 x 8 tiles
    - Small logical capacity (~500 LUTs)
  - 28nm ideal node for harsh radiation environments



130nm CMOS (SLAC)

- LBNL **also** taped out an eFPGA designed with **FABulous** framework
  - 180nm CMOS: 10x16 tiles



28nm CMOS (SLAC)

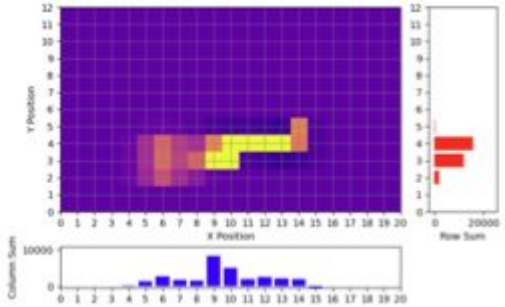
Physics Test Case #1: Smart Pixel Readout

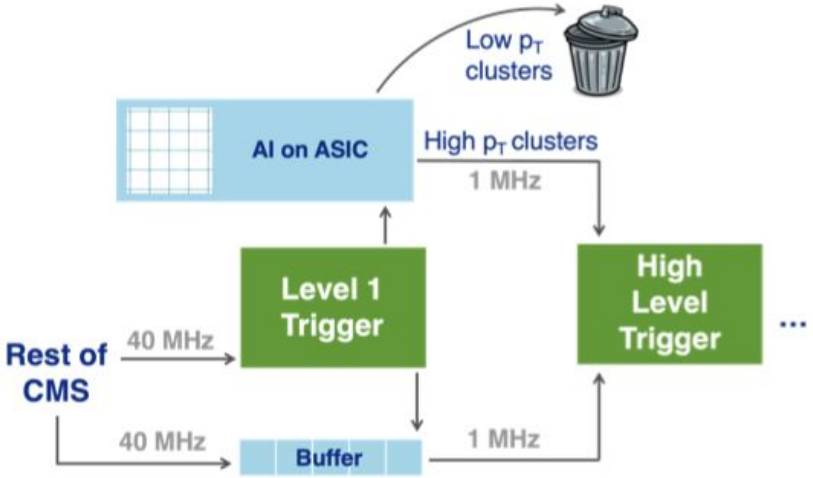
- eFPGAs for at-source inference in low-level pixel sensor data
  - Using Fermilab “smart pixel” dataset
  - Train ML model to classify high-pT from pileup tracks at source, and compress to run in eFPGA

- **In Feb. 2024 achieved first proof-of-concept configuration of toy eFPGA with track classifier Boosted Decision Tree (BDT) with 100% accuracy to quantized software result!**
  - Only ~few % background rejection: need to scale up to realistic logical capacity

- *JINST paper in preparation with 130nm/28nm designs and proof-of-concept ML*

“Smart pixels with data reduction at source”

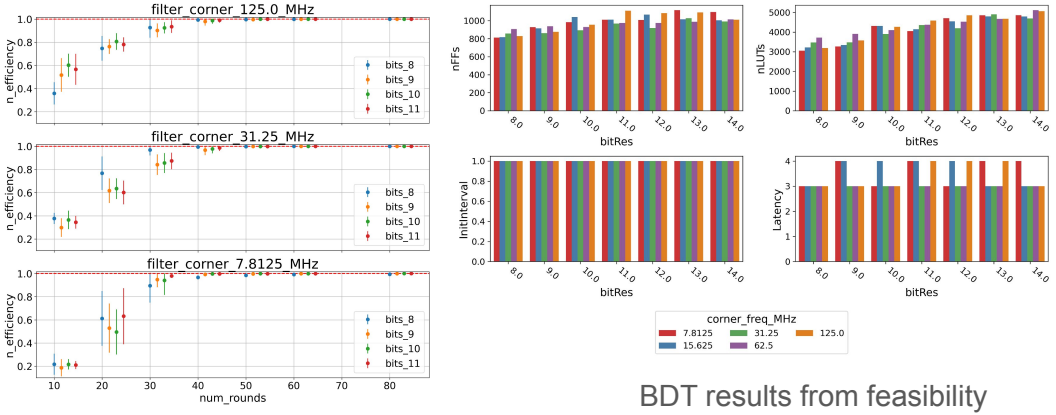




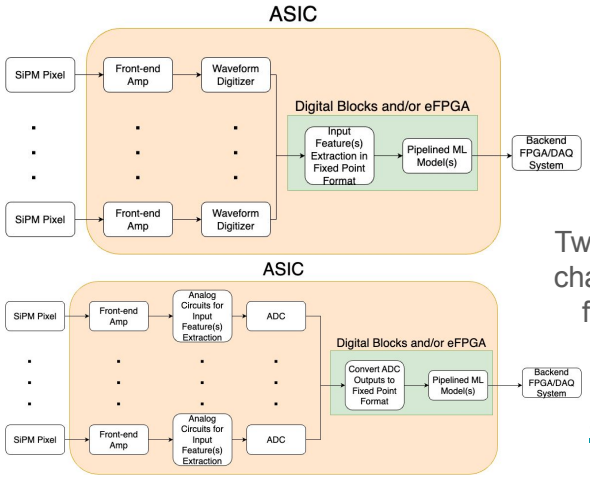
Physics Test Case #2: Classification in Scintillator Emission

- ASICs integrated with required analog blocks (front-ends, ADCs, TDCs, etc) and eFPGA for real-time, AI/ML aided triggering decisions

- Feasibility study conducted for n/g discrimination with sparse BDT/fcNN models
  - Currently working on demonstrator of full signal chain w/ model deployment on eFPGA test chip
  - *JINST paper in preparation*



BDT results from feasibility study; right figure assumes number of boosting rounds = 50



Two possible signal chains; top used for feasibility study

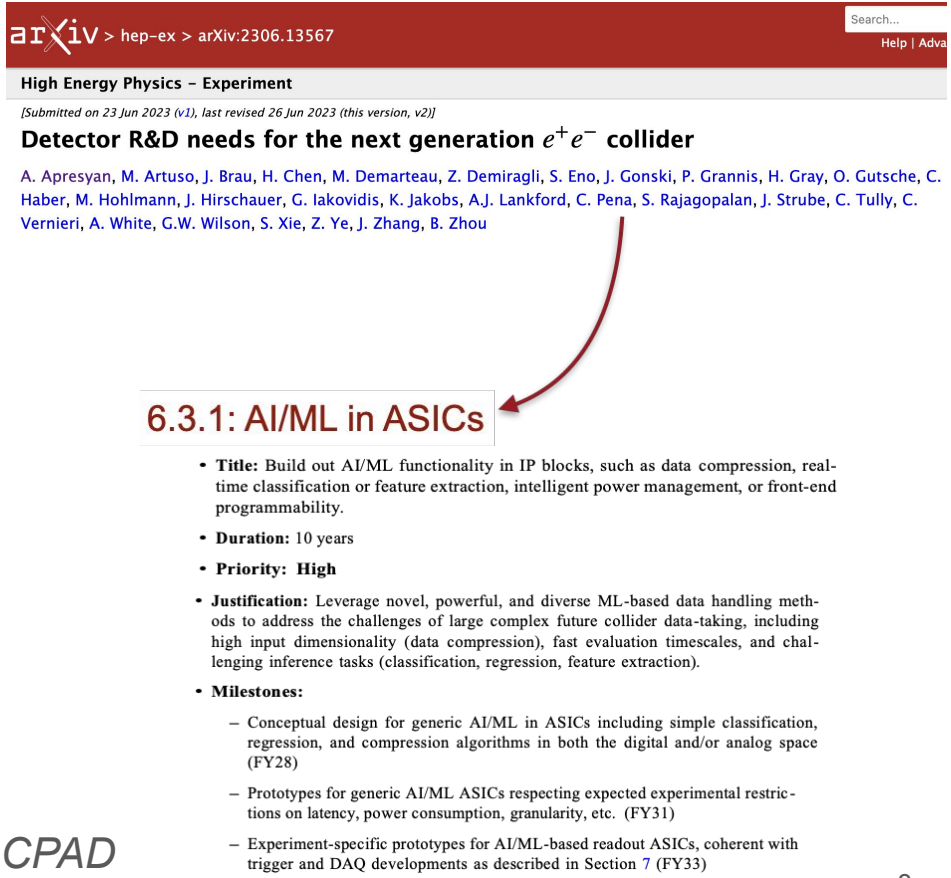
Vision for Work Package

- Increased intelligence in data processing is a key priority of the DOE Basic Research Needs (BRN) [1] and US budget exercise for future Higgs factory[2306.13567]

- **Wide scope for potential university participation**: lower the barrier to entry for ASIC design and engage/train US microelectronics workforce
  - Conversations with university partners ongoing (Hawaii, UPenn)

- Considerable synergy with MAPS, precision timing, 4D tracking and calorimetry, and other AI/ML in microelectronics

➔ *Envision potential to merge with other AI/ML-electronics topics (RDC5, others) for CPAD proposal towards university detector R&D FOA*



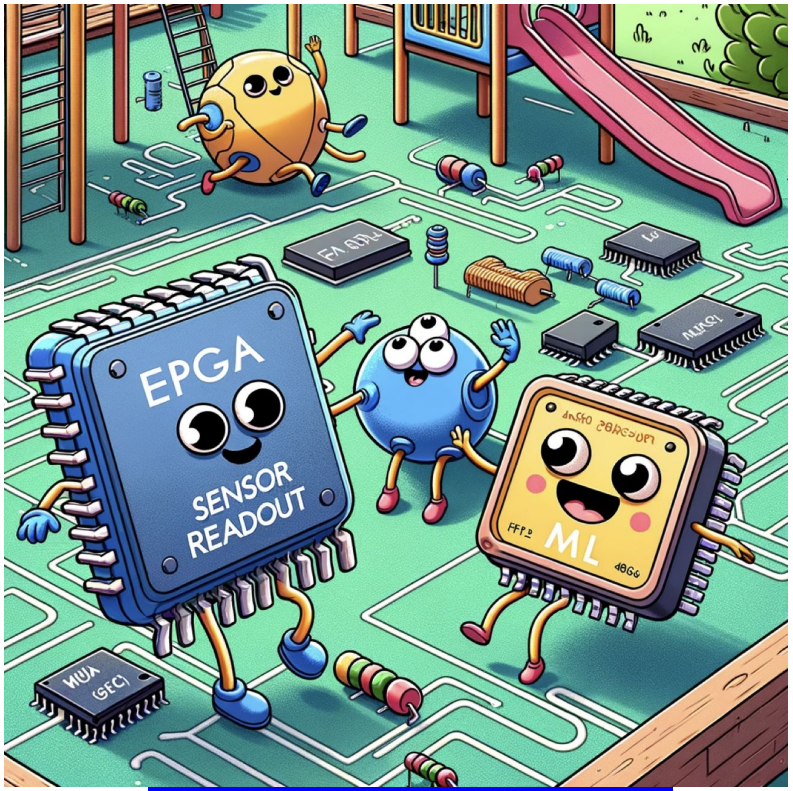
Work Package Objectives

1. Organize a set of **physics targets** for eFPGA use and provide community access to development datasets.
2. Build out the **FABulous open source framework with common IP blocks:**
    a. Optimization for extreme environments such as high radiation or cryogenic temperature
    b. Optimized for higher logic cell density compared to digital auto placement/routing
3. Make available a library of **eFPGA IP blocks**, to enable broad adoption of eFPGA technology and design capability across US labs/universities.
4. Incorporate future collider detector specifications, understand context for eFPGAs in future detector design, and promote **eFPGAs as a viable readout option for detector concepts in the 5-10 year timescale**.

What's next?

- Next steps: co-design of higher-performance 28nm eFPGA for variety of pixel readout tasks (SLAC)

- Happy for more collaborators!



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