Fermilab U.S. DEPARTMENT OF ENERGY Office of Science

RDC4 - Fermilab ASIC R&D Ideas

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RDC4 – Fermilab R&D and work packages ideas

Covered in this talk:

Smart Pixels
- Expanding the **Smart Pixels Collaboration**
- AI in pixel, including digital/analog/beyond CMOS
- NSF POSE Award to support HLS4ML and make it widely available to community (Northwestern, UIC, Arizona State, Fermilab)
- AI on edge, including fully reconfigurable on eFPGA
  - (Northwestern+Columbia+Fermilab funding for 3Y to develop design methodology for eFPGAs)
- AI chiplets
- Distributed AI communications across chips

3D (Chicago 3D Chips Codesign Community)
- MPW, MP-NDAs, access to new 3D tools, Assembly Design Kits (ADKs)

CMOS sensors codesign (Tower, Global Foundries, SkyWater)
- MAPS
- LGAD
- SPADs (cryoSPAD development with GF 55nm for DUNE)
- Also interested in SiC for MAPS

SiPh

Not covered in this talk:

PDK and IPs for extreme environments
- cryo + radiation
- cryo probe station and hosting
- given current 22FDX cryomodels to GF to build upon
- 22FDX, GF28HV, coordinating with CERN for TSMC28

Superconducting Electronics
- JJ – JPA/TWPA – SNSPD

Verification
- currently working with UVM and Cocotb
- further development of formal verification for SEU tolerant design.
- infrastructure for verification IP sharing

Additionally, we are also interested in:
- **IP development in 28nm** (e.g. **fast timing**)
  - e.g. 3D LGAD Front End for 3D LGADs
  - ps TDC currently being tested with LGAD and SNSPD
- **wireless transmission**

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Smart Pixel Detectors:

- **AI in pixel**, including digital/analog/beyond CMOS
- Expanding the **Smart Pixel Collaboration** (FNAL, John Hopkins, UIC, UChicago, Northwestern, Purdue, Kansans State Uni, ORNL, Sandia)
- NSF POSE Award to support HLS4ML and make it widely available to the community (Northwestern, UIC and UIUC, Arizona State, Fermilab) *An Open Source Ecosystem for Collaborative Rapid Design of Edge AI Hardware Accelerators for Integrated Data Analysis and Discovery*
- **AI on edge**, including fully reconfigurable on eFPGA: Northwestern+Columbia+Fermilab funding for 3Y to develop design methodology for eFPGAs
- AI chiplets/custom accelerators
- Distributed AI communications across chips: photonics AI

Large collaboration and ecosystem, good candidate for a university-led initiative

Pixel detector R&D effort for “Phase III”

Applications

HL-LHC Phase III upgrade R&D

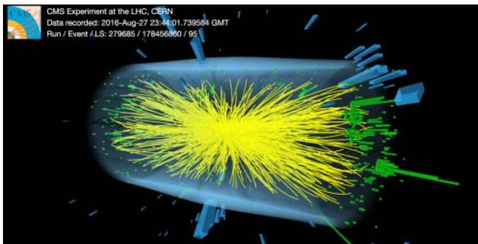
- 28nm process node
- 4x pixel size reduction
- 2x improve threshold detection
- 40x faster sampling rate
- 1W/cm^2

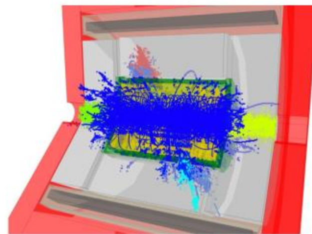
Future colliders

- Smart pixels with data reduction at source: possible applications for linear e+e- colliders

Xray sources (e.g. Ptychography)

- In-pixel AI for lossy data compression at source for X-ray detectors

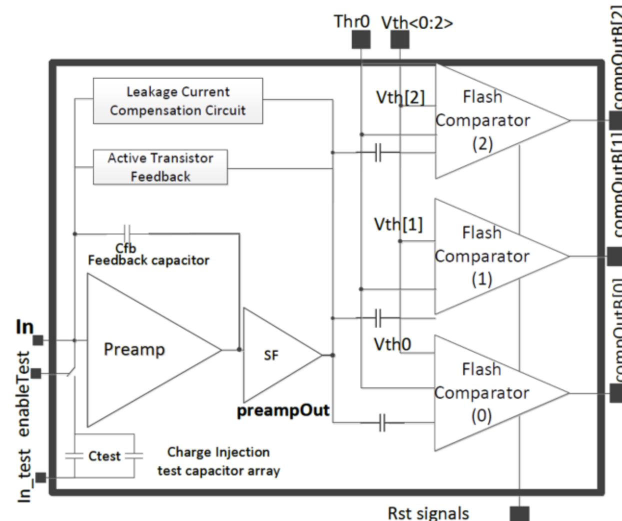




CMS & Future colliders (hh, ee, uu)

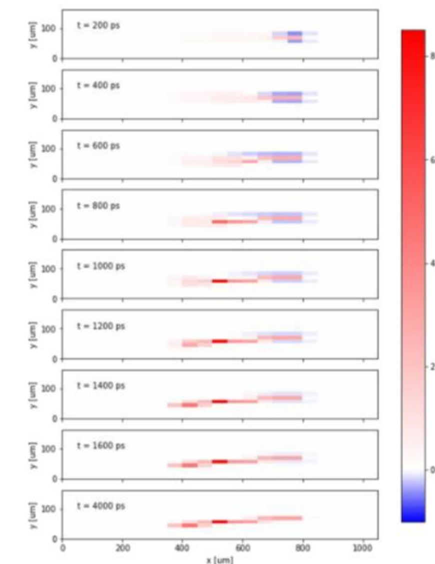
ROIC Implementation

- Low power, low noise preamplifier with a leakage compensation
- A low power 40MSPS synchronous comparator architecture with auto-zero capability to create an in-pixel ADC
- On chip data reduction capability using AI/ML techniques



Smart Pixel dataset

- Open Access simulated dataset of silicon pixel clusters produced by charged particles (pions), where the particle kinematics are taken from fitted tracks in CMS Run 2 data.
- Morris Swartz, & Jennet Dickinson. (2024). Smart pixel dataset (Version 3) [Data set]. Zenodo. https://doi.org/10.5281/zenodo.10783560



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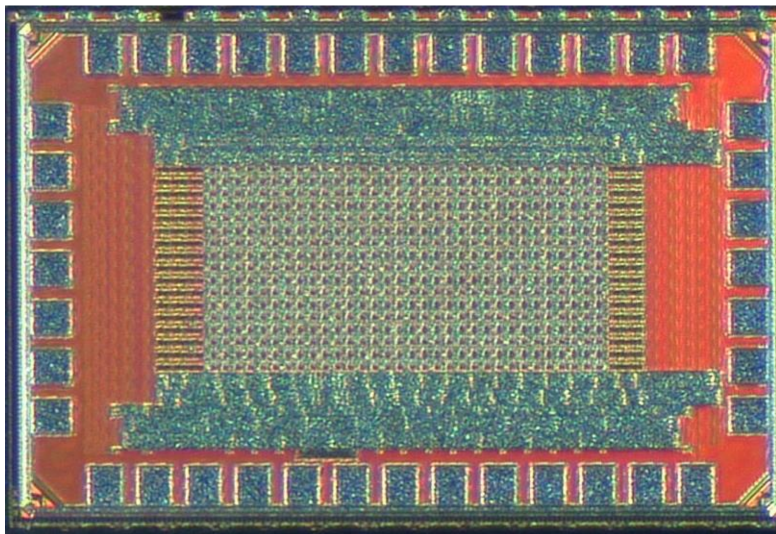
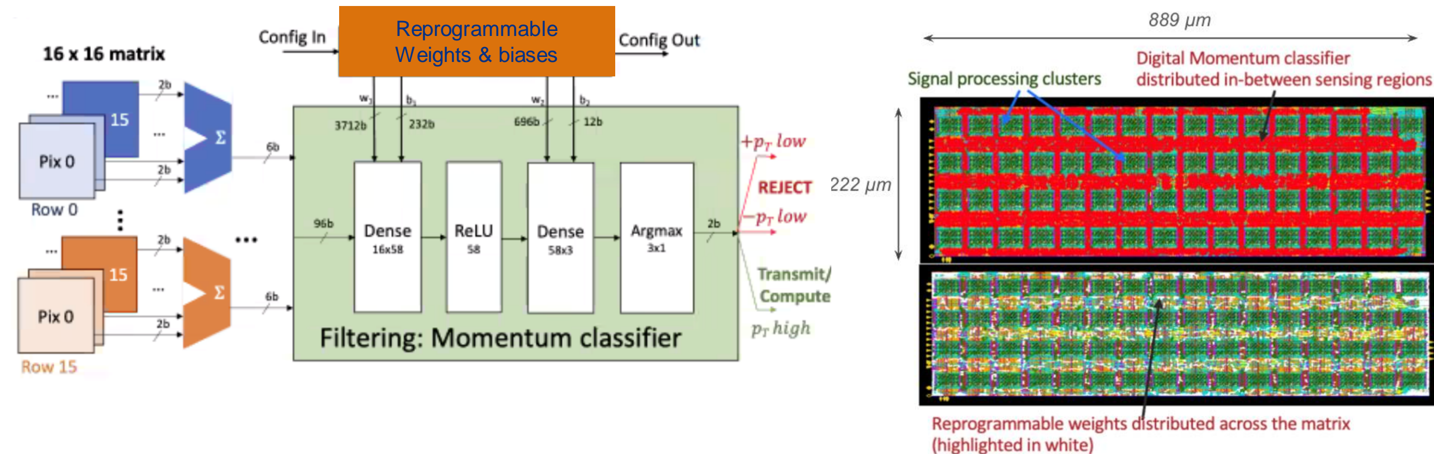
Ongoing Effort for “Phase III” pixel replacement

First Prototype Implementation:

- Analog frontend without ML/AI backend
- TSMC HPC+ 28nm
- Array of 16x32 pixels
- Pixel size: 25μm x 25μm
- ASIC size: 1.5mm^2



Second Prototype Implementation:



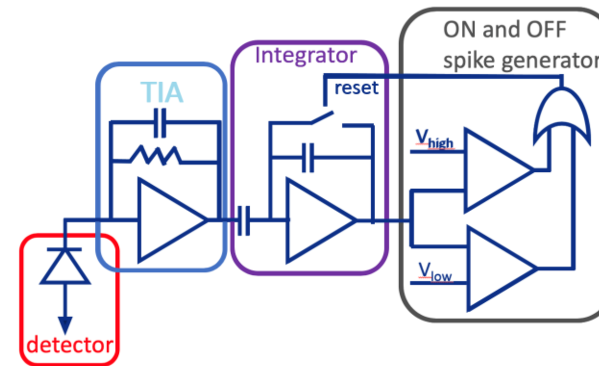
- **Co-Design** development with analog frontend pixels tightly connected to a fully combinatorial digital classifier
- 300uW of power for 256 pixels
- ~1uW/pixel to ensure our goal of 1W/cm2
- Classifier allows to reject 75% of the clusters
- Reducing power required for data transfer

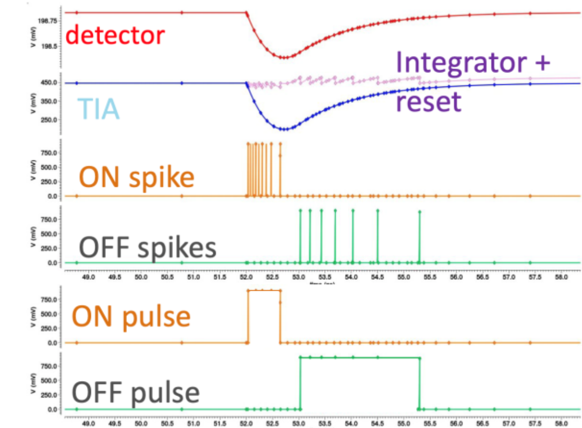
Future Effort

(1) Neuromorphic Solution

- Event-driven Front-End Architecture
- Spiking Neural Network (SNN) backend

Algorithm -> Digital -> Analog

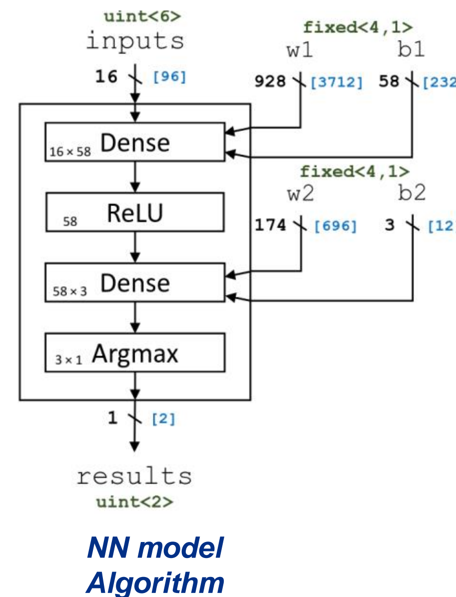




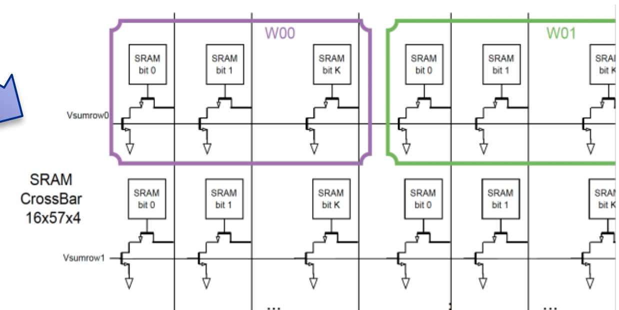
- Pulse shape encoded in spike train
- Ultra-fast signal processing ~ 100ps
- Digital processing – power constraints
- Analog processing – device constraints (speed)

(2) Analog AI Back-End:

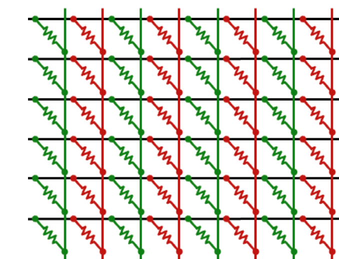
- Implement analog classifier counterpart for a cluster of pixels
- Develop ROIC prototypes:
  - SRAM based solution
  - Floating Gate based solution
  - Beyond CMOS ReRAM based solution



NN model Algorithm



Analog NN model with SRAM



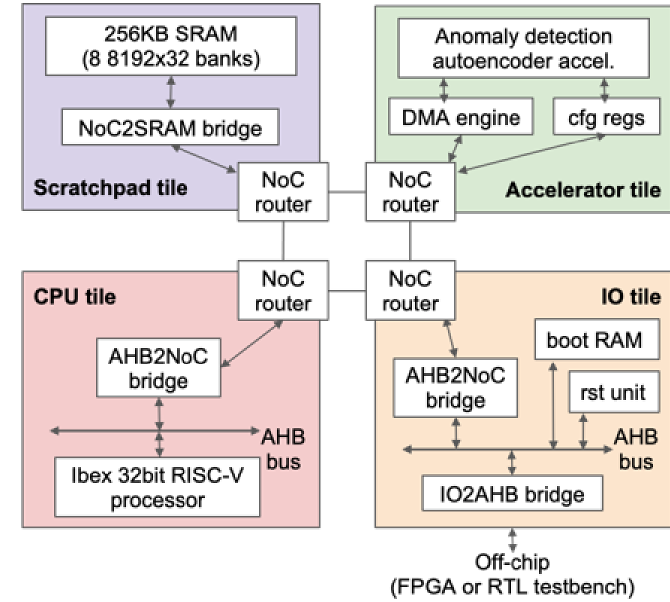
Analog NN model with ReRAM

Reconfigurable Edge AI – with eFPGAs

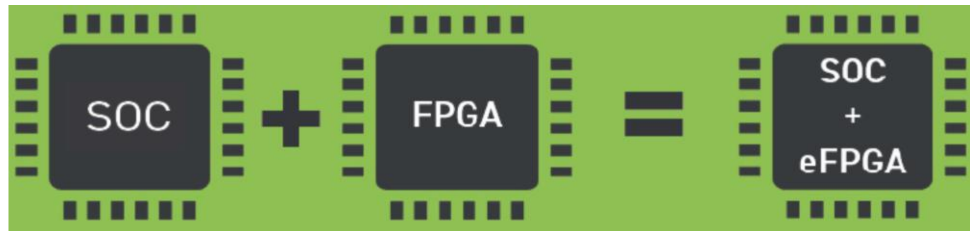
- Collaboration with Columbia U. & Northwestern U.
- Edge AI: Combining two established open-source platforms (ESP and HLS4ML) into a new system-level design flow to build and program a System on chip

  In the modular tile-based architecture, we integrated a low-power 32-bit RISC-V microcontroller (Ibex), 200KB SRAM-based memory, and a neural-network accelerator for anomaly detection utilizing a network-on-chip.

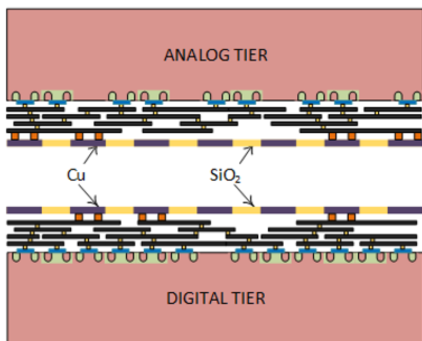
- Embedding FPGAs on detector: Radhard/ cryogenic eFPGA on-chip – with Flex Logix (22nm / 28nm).
- Establishing design flow (with ESP) and investigating extreme environment performance



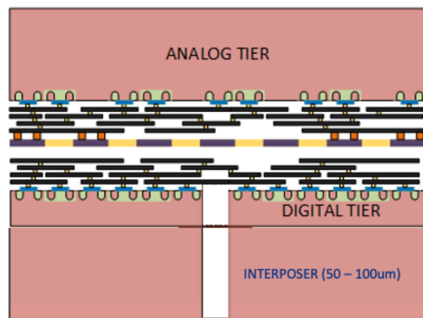
TSMC 28nm eFPGA dev board from FlexLogix



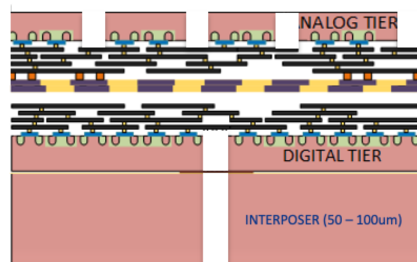
Establishing Chicago 3D Chips Codesign Community C 3D C^3



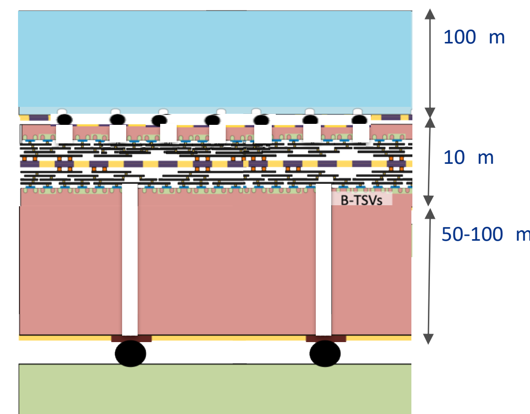
a. Face-2-Face wafer bonding



b. B-TSV insertion and bond to TSV interposer wafer



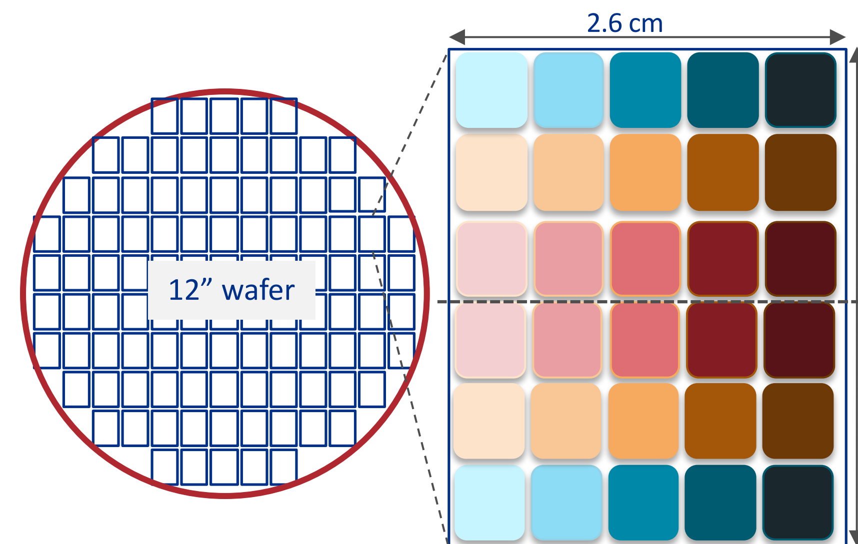
c. Thinned down top side and B-TSV insertion



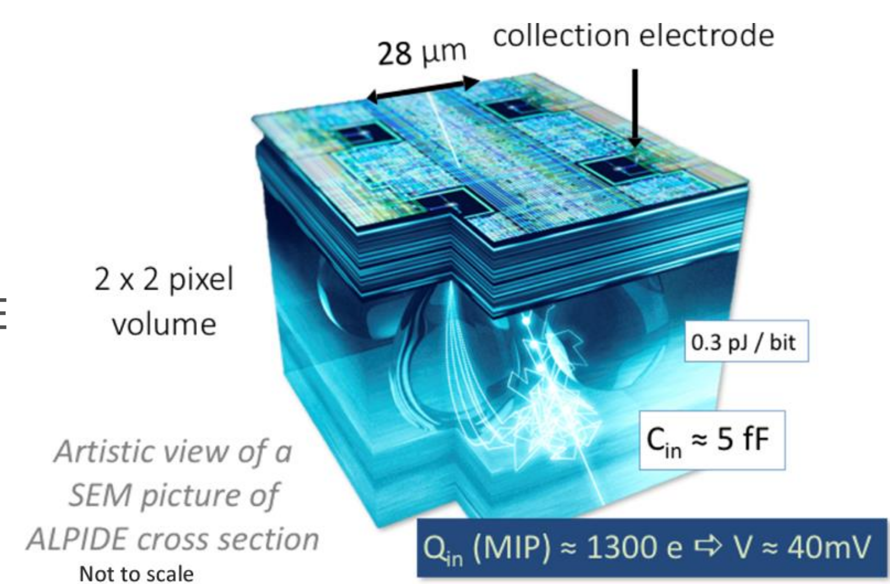
3D sensor system

Fermilab,
Oak Ridge,
UMN,
ASU,
Northwestern,
U.Chicago,
UIC,
UIUC,
Purdue,
Cornell Tech,
DESY,
SLAC

- CREATING A COMMUNITY and RELEVANT PARTNERSHIPS
- Create open source ADK (Assembly Design Kits) and distribute to consortium members. Membership agreement is almost ready
- Fermilab assembles MPW work with (IMEC, MUSE and others)
- Currently have a multi party NDA with more than 80 institutions for HEP chips (IMEC-TSMC-CERN-Fermilab-others)
- 1st run: Low cost – same as the cost of silicon; 65 nm; several national labs and university groups have expressed interest and actively working on designs



Sensor Co-design with SkyWater



GOALS

- Enable US manufactured sensor capability for HEP experiments
- Optimize the process to enable various types of sensors ubiquitously used in HE (MAPS, MAPS with timing, Digital SPADs, LGADs, CMOS LGADs)
- Co-design sensor and readout electronics
- Standardize chip format and pad frame to enable high throughput testing
- Enable the broad adoption of the development across HEP community

PROGRESS

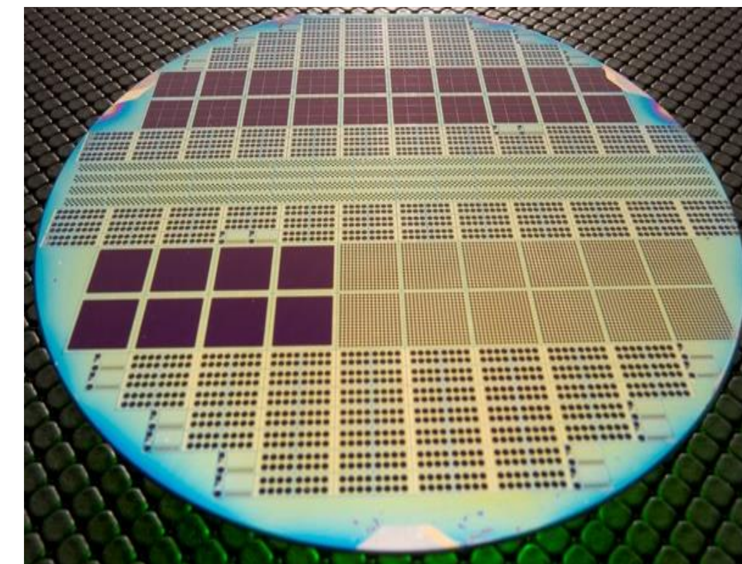
PARTNER with **SKYWATER TECHNOLOGIES**. Multi party NDA with **LBNL. ANL** has confirmed participation

Strong academic support from **UC, UIC, Purdue, NU, UIUC**, for device simulation and testing

Engineering run with various designs on a high resistivity wafer. Secured partial funding from JTFI award

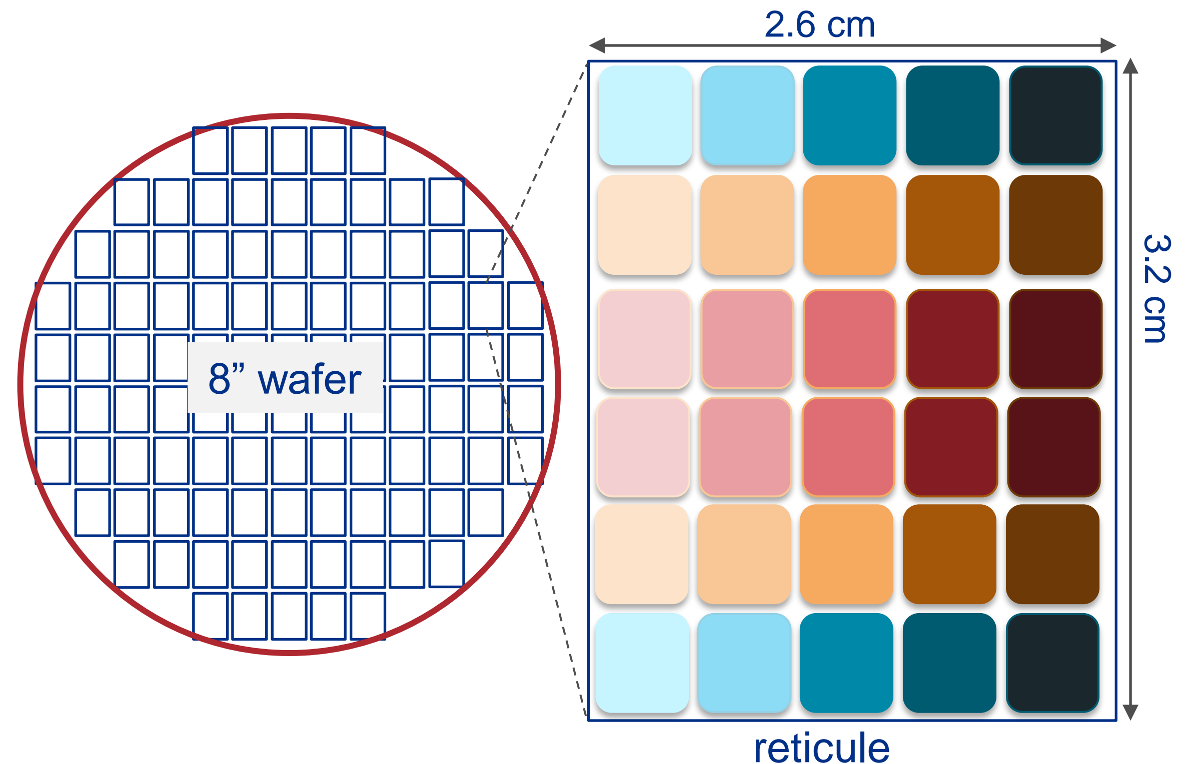
High-throughput testing of sensors at Fermilab and other institutions

Regular Monday meetings, Fermilab LDRD started working on TCAD simulations.



Sensor Co-design with SkyWater

- Process details: Epi on bulk CMOS
  - Epi thickness: > 25um
  - Epi resistivity: ~ 1k-Ohm-cm
- Create a HEP specific MPW
- Divide reticle into 24 dies (5 x 5 mm^2)
  - ½ wafer with only sensors
  - ½ wafer with sensors & readout circuits
  - Test dies with single transistors
- Sensors: would require process splits for optimization



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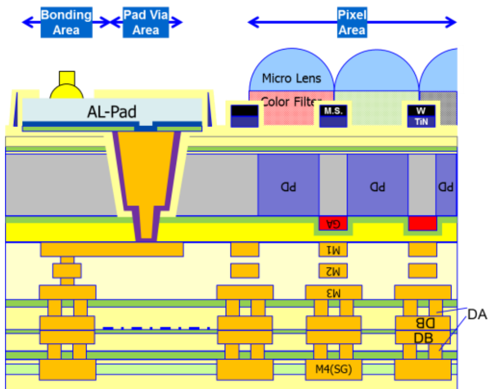
Other Sensor + Readout Co-Design Activities

Tower Semiconductor (3D LGADs)

- Create **LGADs** in 12" CMOS wafers which can be 3D integrated (hybrid bonding) with readout circuits in 28 nm
- Large area, low power sensor+readout IC with ~50um pixel
- Fast time tagging (~10ps precision)
- Secured funding through DOE Accelerate

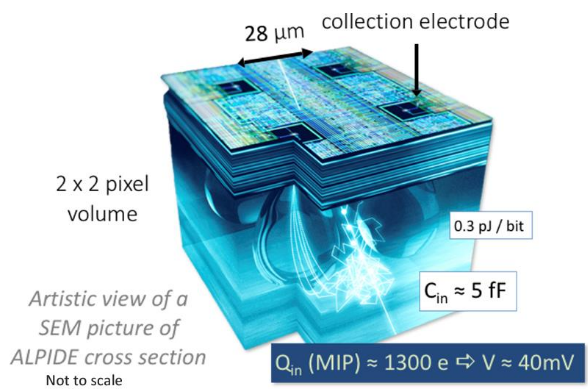


MIT LL - SiSeRO

- Skipper-in-CMOS: co-developed novel ultra-low noise sensors with Tower Semiconductor 180 nm CIS process
- Testing at Fermilab of more than 400 devices will help determine structures with highest Quantum efficiency

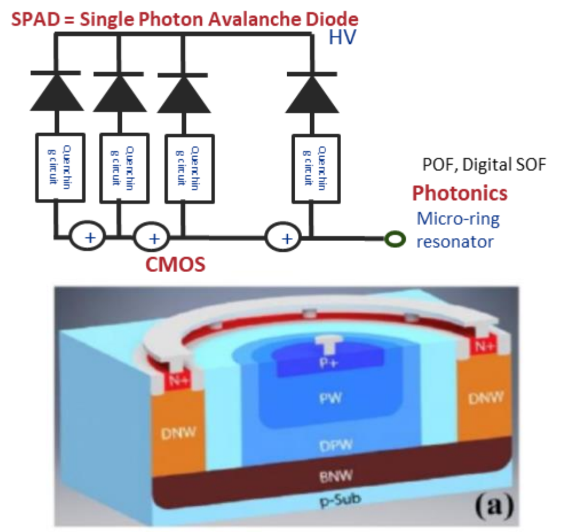
SkyWater

- Enable US manufactured sensor capability for HEP experiments
- Optimize the process to enable various types of sensors ubiquitously used in HEP (MAPS, MAPS with timing, Digital SPADs, LGADs, CMOS LGADs)
- Multi party NDA with LBL, ANL. Strong academic support from UC, UIC, Purdue U., NU, UIUC, for device simulation and testing.



Global Foundries

- Development of Cryo Digital SiPM (77K) for DUNE photo detector (eventually down to 3K)
- Focused on cryo Digital SiPM (SPAD integrated in CMOS process)
- Integrated photonics for power delivery and data transfer



Cryo PDK development with Foundry support

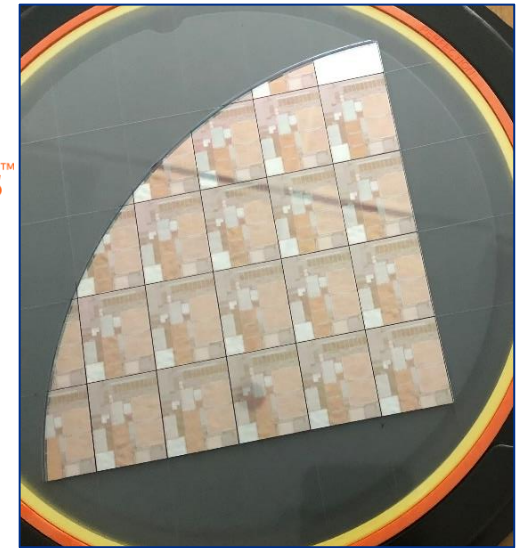
GF 22FDX: cryoPDK (BSIM-IMG) for 4K provided to GF for future enhancement and distribution (protected)

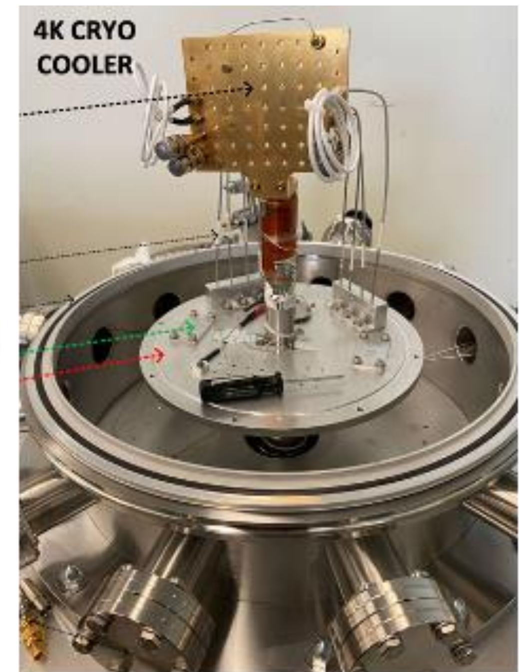
SiGe 9HP: collaboration with Northwestern

GF 28HV: collaboration with GF

TSMC 28 HPC+: coordinating with DRD 7

Skywater 130: coordinating with UTA

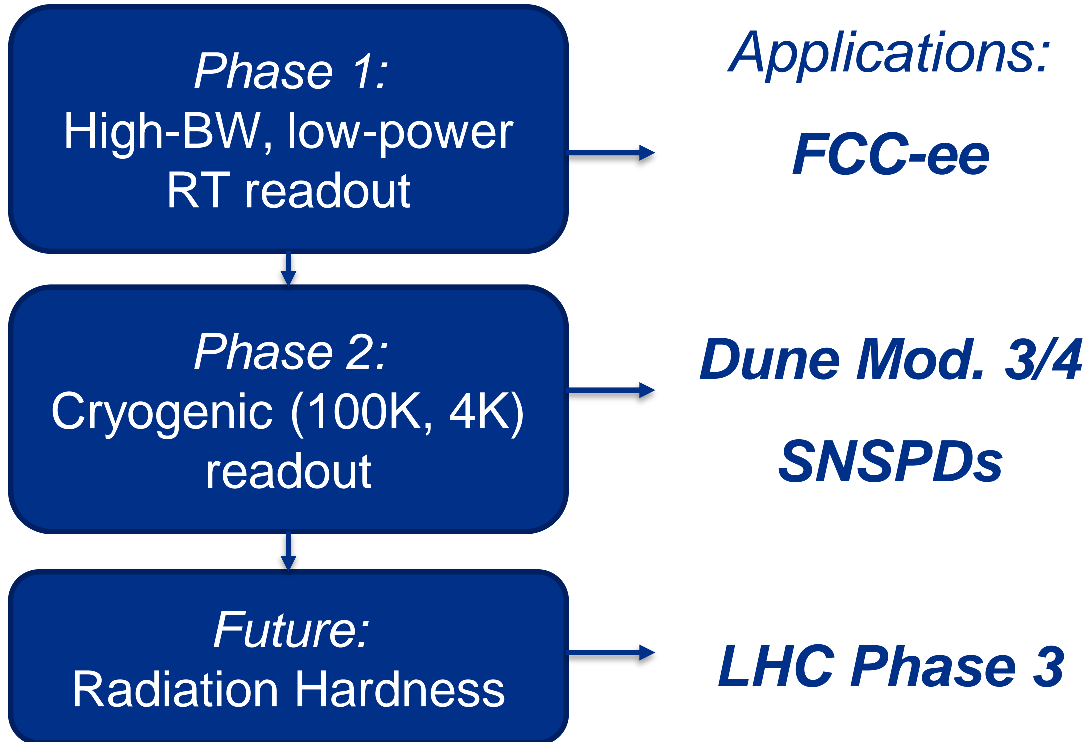


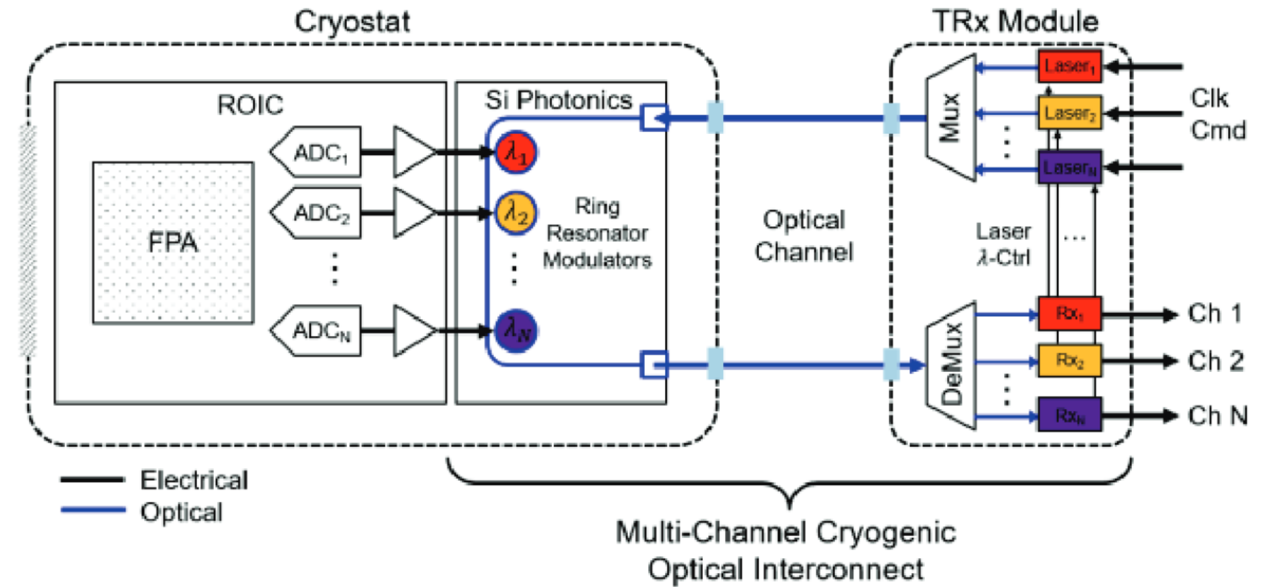


Silicon Photonics: Developing Expertise in a Critical Technology for Future Detectors

100x bandwidth, **100~1000x** lower heat load,
10~100x channel density, EMI/cross-talk immunity.

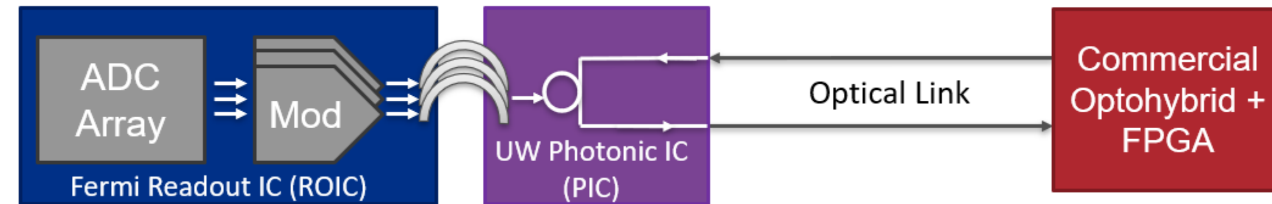
In collaboration with U.Washington





Conceptual schematic of a scalable cryogenic readout architecture based on silicon photonics [1]

Phase 1 Prototype Block Diagram



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Silicon Photonics in the SPROCKET3 Tapeout