Updates on DAT & RTS at BNL

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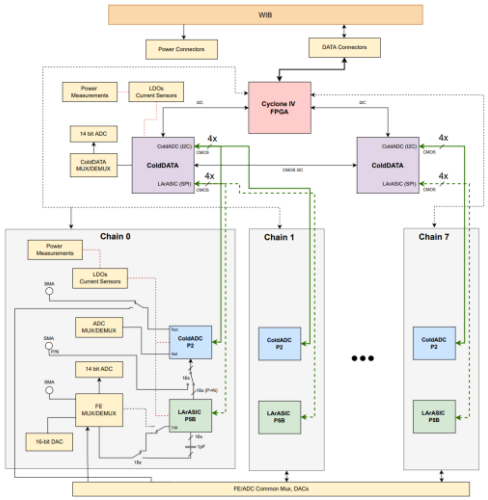
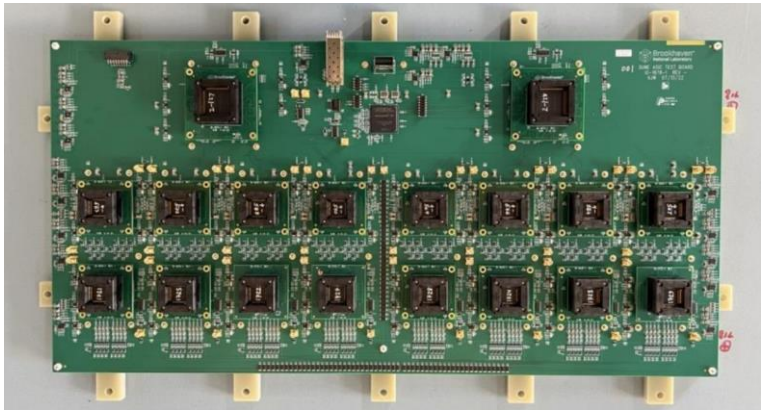
04/12/2024

Hardware: DUNE ASIC Test Board (DAT)

- DUNE ASIC Test (DAT) Board
  - Unified ASIC test board for LArASIC, ColdADC and COLDATA QC
    - Compatible power and data interface with WIB. It acts as exactly same as a FEMB to WIB
    - Can perform QC testing for 8x LArASIC, 8x ColdADC and 2x COLDATA at both RT and LN2 with MSU new RTS
    - Aim for DUNE-FD1 & FD2 ASIC QC carried out in several test sites
  - A single big board solution with ASIC socket mezzanines
    - ASIC socket suffers mechanical degradation through thermal cycling
    - More commercial semiconductor devices have been identified for cryogenic operation
      - Such as Analog MUX: SN74LV4051, Power Monitoring Chip: INA226, I2C Bridge device: PCA9306, DAC: AD5675ARUZ





DAT Revision List

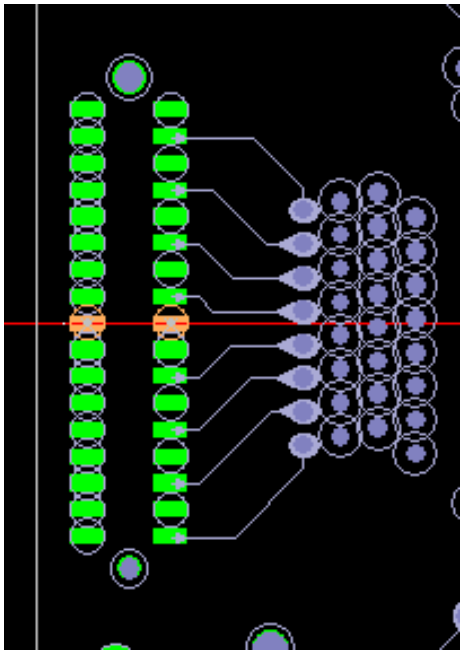
- BOM Update
  - Re-assign some resistors and capacitors with correct values
  - Add a 100 Ohm at each regulator output/input/bias to expedite the power cycling
  - Keep SMA footprint but DNI
- Schematics Issues
  - Few FPGA IOs were assigned with conflict
  - Few FPGA DIFF IOs missed external termination resistors
- Add clock fanout buffer for SCL/SDA between COLDATA and ColdADCs
- **Connect COLDATA PLL lock signal to FPGA IO**
- Remap FE calibration scheme
  - **Calibrate one FE channel at a time per board if needed**
- Remap ColdADC test scheme
  - **Each ColdADC channel can be tested independently**
- Add a SE-to-DIFF buffer on DAT for external signal from WIB
- Keep SFP cage inside the board outline
- **Add circuit for COLDATA EFUSE programming**

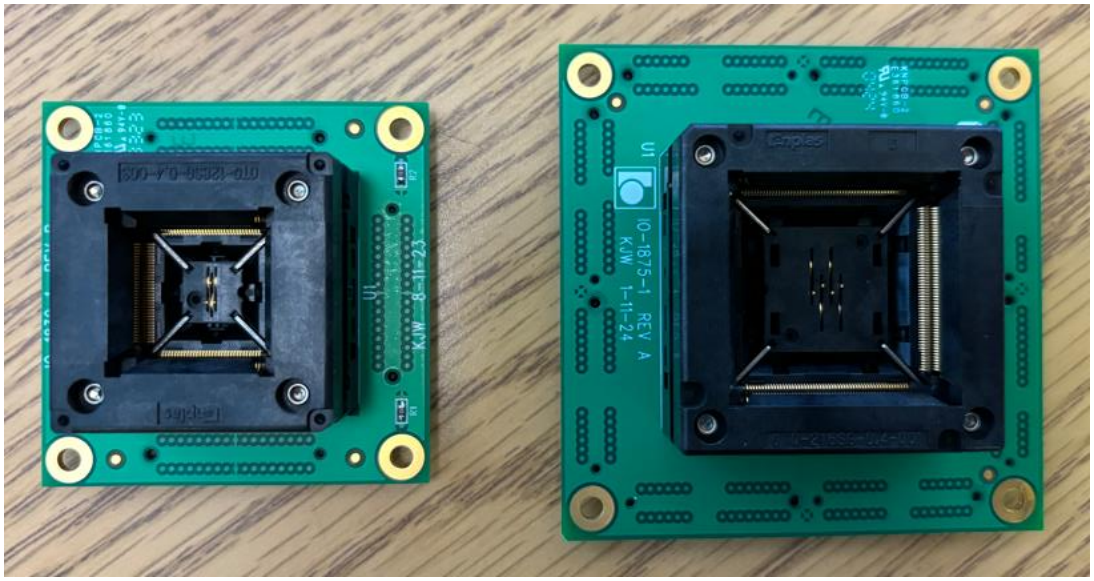
DAT Fabrication and Assembly Status

- Received 8 pieces of revised DAT PCB boards on 04/08/2024
  - Ordered 10 pieces, 2 pieces are under fabrication
- Ship DAT kit to assembly house on 04/09/2024
  - BNL purchased materials and components
    - Enough parts for >10 boards
  - Assembly lead time: 4 weeks
    - Expected to get assembled boards back in early May

Socket Mezzanines Status

- Socket ordered and received
  - COLDATA: OTQ-216SG-0.4-001, 20 pieces
  - LArASIC/ColdADC: OTQ-128SG-0.4-003, 190 pieces
- Improve reliability of socket mezzanines





Inner traces, Via in pad with tear drop, enlarge pad size

LArASIC QC Status on DAT

Test Items

```
(base) PS D:\Github\BNL_CE_WIB_SW_QC_main> python .\DAT_LArASIC_QC_quick_ana.py
Analyze all test items? (Y/N) : n
  QC task list
 0: Initilization checkout
 1: FE power consumption measurement
 2: FE response measurement checkout
 3: FE monitoring measurement
 4: FE power cycling measurement
 5: FE noise measurement
 61: FE calibration measurement (ASIC-DAC)
 62: FE calibration measurement (DAT-DAC)
 63: FE calibration measurement (Direct-Input)
 7: FE delay run
 8: FE cali-cap measurement
Please input a number (0, 1, 2, 3, 4, 5, 61, 62, 63, 8) for one test item:
```

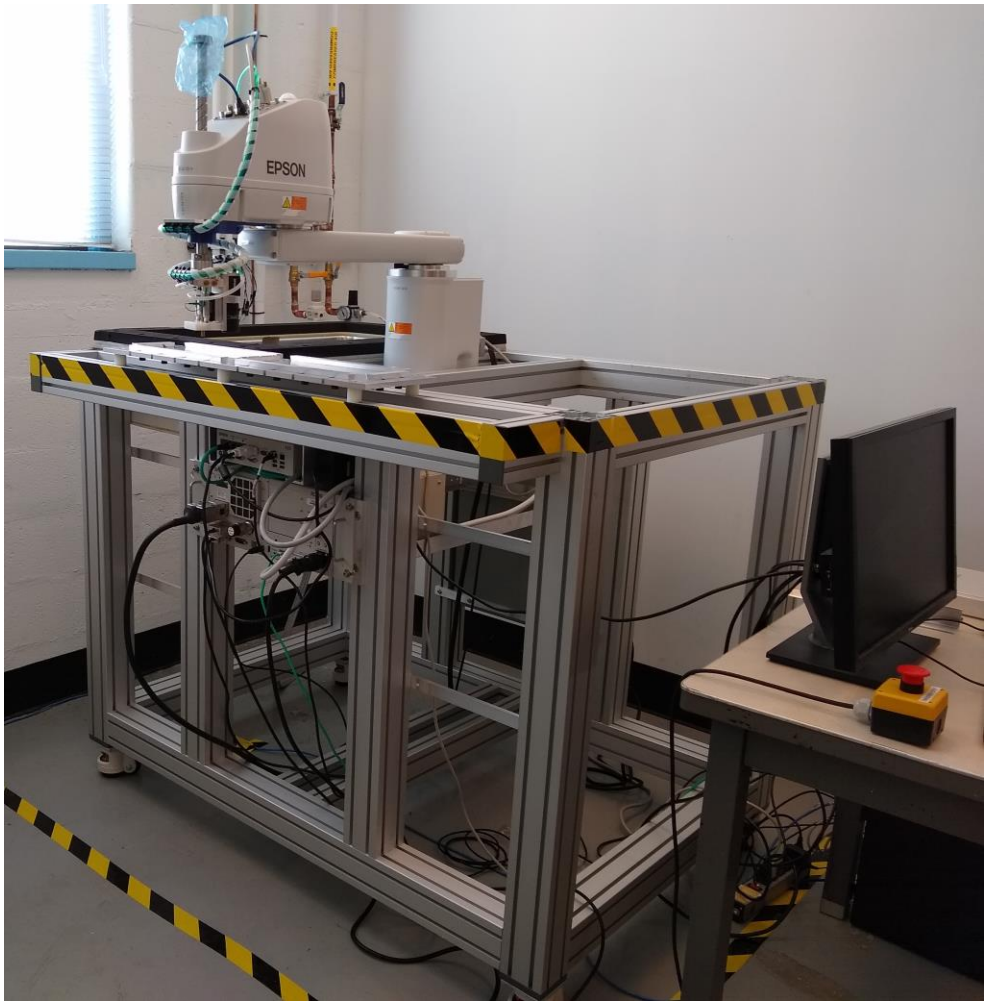
Raw data

```
~/dune_ce/ce_ana/test nitish@nitish
(ce_venv) ❯ ll ../data/FE_001000001_001000002_001000003_001000004_00100
total 707M
-rw-rw-r-- 1 nitish  41M Nov  6 13:38 QC_CALI_ASICDAC.bin
-rw-rw-r-- 1 nitish 151M Nov  6 13:38 QC_CALI_DATDAC.bin
-rw-rw-r-- 1 nitish  51M Nov  6 13:38 QC_CALI_DIRECT.bin
-rw-rw-r-- 1 nitish 161M Nov  6 13:38 QC_Cap_Meas.bin
-rw-rw-r-- 1 nitish 8.6M Nov  6 13:38 QC_CHKRES.bin
-rw-rw-r-- 1 nitish  81M Nov  6 13:38 QC_DLY_RUN.bin
-rw-rw-r-- 1 nitish 1.1M Nov  6 13:38 QC_INIT_CHK.bin
-rw-rw-r-- 1 nitish  15K Nov  6 13:38 QC_MON.bin
-rw-rw-r-- 1 nitish 3.1M Nov  6 13:38 QC_PWR.bin
-rw-rw-r-- 1 nitish 4.1M Nov  6 13:38 QC_PWR_CYCLE.bin
-rw-rw-r-- 1 nitish 211M Nov  6 13:38 QC_RMS.bin
```

- Jesse from LSU (Hanyu's group) visited BNL on 02/26-03/08
  - LSU (Hanyu's group) has done ~3,000 LArASIC QC warm testing based on Dual-DUT test board
  - Got familiar with LArASIC QC based on DAT board
  - Got training to be a local contact to oversee LArASIC QC
- **~1,500 LArASIC chips are tested at warm based on DAT board**
  - Mainly done by SBU students, very positive feedback
- **QC report and database (require further discussion)**
  - Analysis script to generate full QC report is being developed (SBU student: Rado)
  - Strategy for data storage
    - NFS for local raw data storage
  - Define key parameters for hardware database (Same requests for ColdADC and COLDATA QC)
    - Save test result in Json file?
    - Martin (LSU) , Karla (BNL): Interface to hardware database

RTS Update

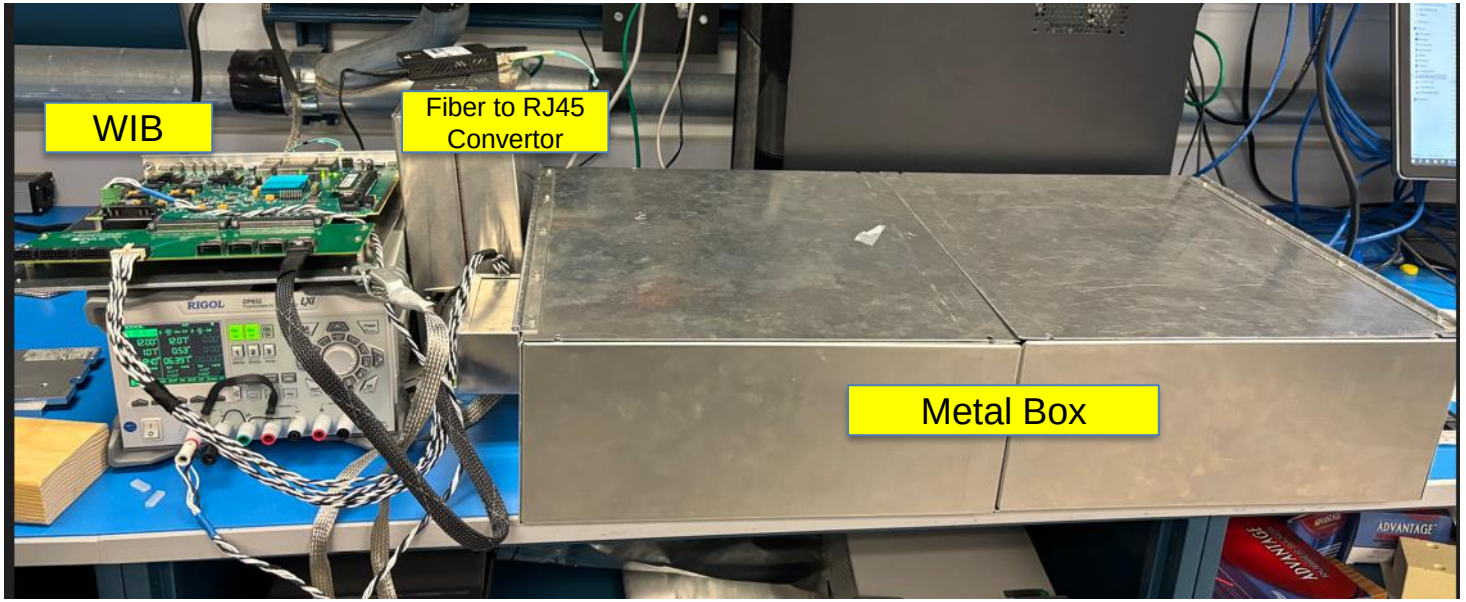
- Update from Volodya on 04/11
  - Augie completed the last installation step. The RTS is connected to the building compressed air line, **all components received from MSU are installed** (the vacuum control box, the arm hand with a camera, the upfacing camera, the image processor). Carl installed the dummy DAT board with sockets (no electronics). I am documenting all the changes and hope to **send the documentation to safety** later today. Hope that the review process will take much less time than the first review. Hope that early next week we will **get approval from safety and can start exercising the chip loading/unloading into the sockets on the DAT board**. The last thing we need from MSU is the light for the downfacing camera.

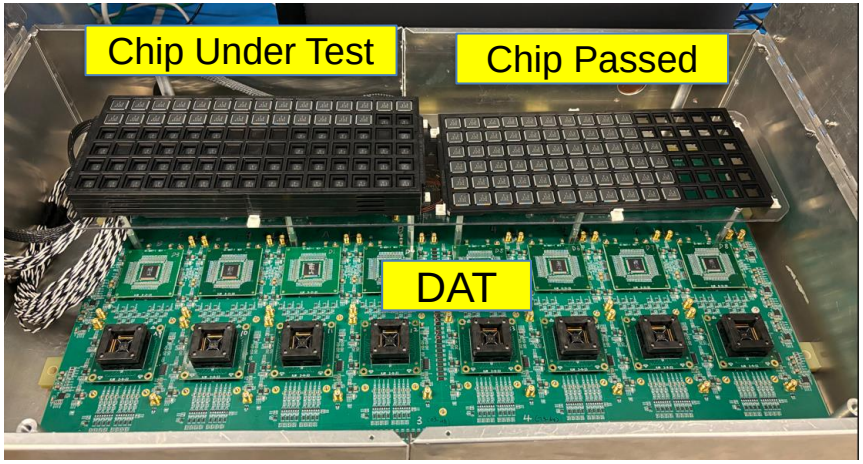


DAT Setup to be distributed

- **BNL provides each DAT setup (no RTS version)**
  - A DUNE WIB with a WIB adapter board (miniSAS version)
    - Installed on a WIB support metal plate
  - 1 pieces of 12V WIB power cable
  - 1 set of 2.5m cold power cable and miniSAS cable
  - 1 DAT board with different configurations
    - LArASIC QC: 10x 128-pin socket mezzanines, 8x ColdADC chip mezzanines, 2x COLDATA chip mezzanines
    - ColdADC QC: 8x LArASIC chip mezzanines, 10x 128-pin socket mezzanines, 2x COLDATA chip mezzanine
    - ColdADC QC: 8x LArASIC chip mezzanines, 8x ColdADC chip mezzanines, 3x 128-pin socket mezzanines
  - 2 pieces of ESD-safe vacuum pens
  - 1 set of fiber to RJ45 convertor
  - 1 metal 30x20x8 inch shield box to hold DAT board
    - Open-up lid with support
  - A setup instruction
    - including rules for grounding, isolation and ESD protection
- **Test Site provides**
  - 12V, >4A DC low noise power supply
  - ESD-safe Bench-top
  - A RJ45 port connected to a local server
    - With NFS set up

Current DAT Test Stand at BNL





DAT Distribution Draft Plan

- Setup is expected to be distributed in the coming months
  - Phase I: initial setup
  - Phase II: 5 more DAT-1A (revised) board
  - Phase III: RTS in use

	Phase I	Phase II	Phase III (RTS)
LArASIC	BNL QC: 1 DAT-1	BNL QC: 1 DAT-1	BNL RTS QC: 2 DAT-1A
	BNL R&D: 1 DAT-1A	BNL R&D: 1 DAT-1A	BNL Support: 1 DAT-1A
	LSU QC: 1 DAT-1	LSU QC: 1 DAT-1A	LSU QC: 1 DAT-1A
	BNL RTS: 1 DAT-1A	BNL RTS: 1 DAT-1A	Spare: 2 DAT-1
ColdADC	LBNL: 1 DAT-1A	LBNL RTS: 1 DAT-1A	LBNL RTS: 2 DAT-1A
	? : 1 DAT-1A	? : 1 DAT-1A	? : 1 DAT-1A
		? : 1 DAT-1A	? : 1 DAT-1A
COLDATA	Fermilab: 1 DAT-1A	Fermilab RTS: 1 DAT-1A	Fermilab RTS: 2 DAT-1A
		? : 1 DAT-1A	? : 1 DAT-1A

Note: the distribution will also be affected by the availability of DUNE WIB boards

QC Related topics

- QC activities in all sites will be monitored and led by the TPC electronics consortium
  - Maintain central repo for the testing software
  - Each site admin updates the controlled system deployment in coordination with local operators
- All test sites share use the same hardware setup and the same QC procedure
  - All ASICs to have a unique identifier on the package, COLDATA chips will also have E-fuses burnt during the QC process
  - Plan on testing all ASICs both at room and cold temperature
    - The cold screening test is not reliable enough for high-yield ASIC chips
    - if the cold yield is high enough, a small portion (5~10%) of ASIC will be tested at cold instead of all chips.
- QC data storage
  - Test result will be uploaded to the central hardware database
  - Raw data and test result will be backed up locally

Summary

- Revised DAT boards are being assembled
  - 5 pieces
  - Expected to distribute DAT standalone setup in the coming months
- Warm LArASIC QC based on DAT has started
  - Over 1,500 chips have been tested
- ColdADC QC test procedure and scripts are being finalized
  - Jillian’s talk
- COLDATA QC test procedure and scripts is being developed
- BNL RTS makes progress
- Plan for DAT hardware setup distribution