DEEP UNDERGROUND NEUTRINO EXPERIMENT

Brookhaven National Laboratory

U.S. DEPARTMENT OF ENERGY

ColdADC QC test development

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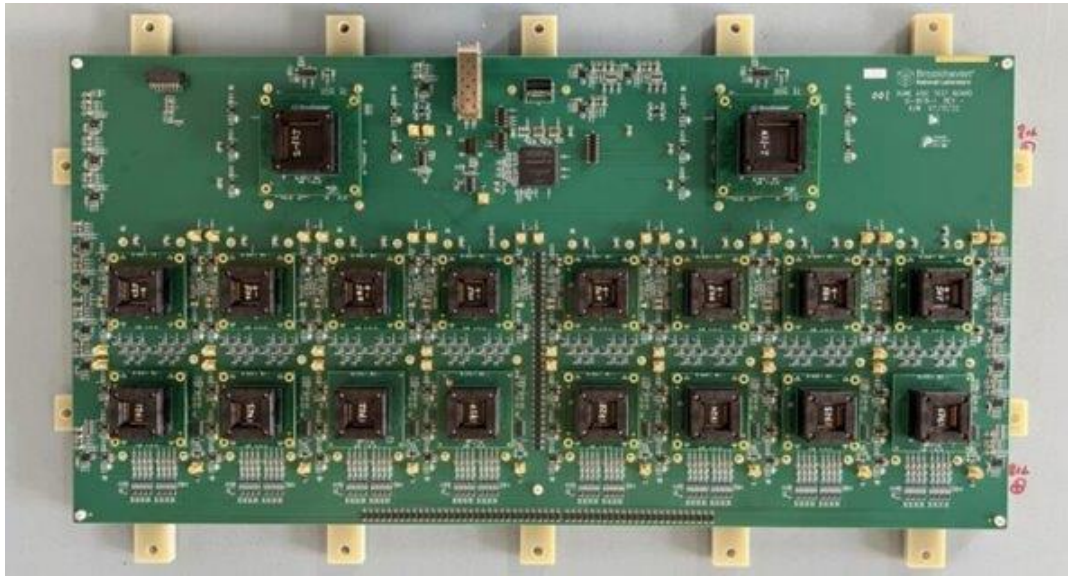
Outline

- ColdADC QC requirements
- Test script overview
- To-do list

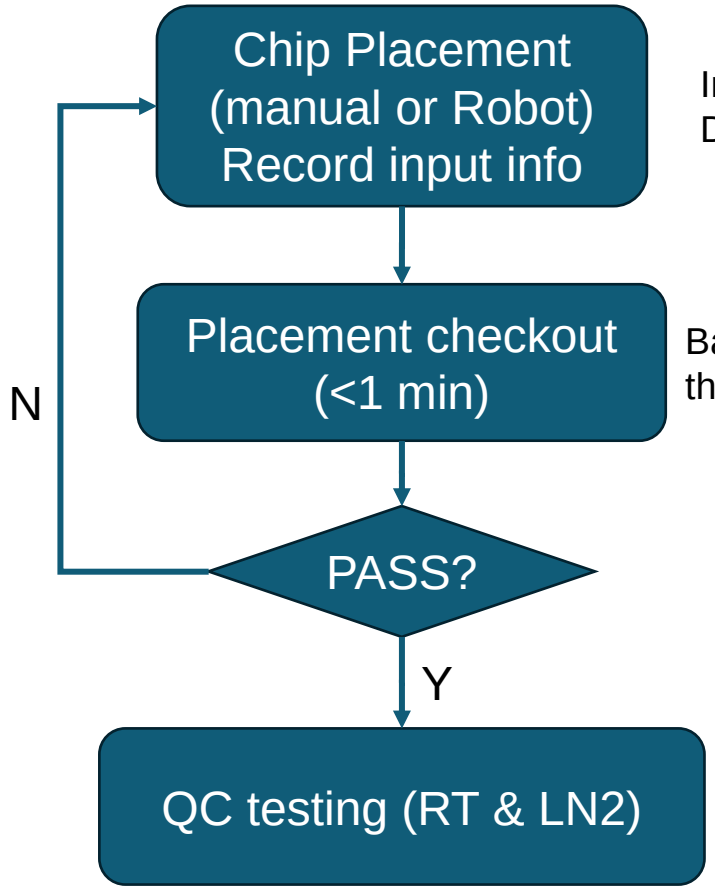


ColdADC QC requirements

- Requirements:
  - Sampling frequency ~2 MHz
  - Number of ADC bits: ≥ 12

- Specifications:
  - Crosstalk: < 1%
  - Differential Nonlinearity (DNL): Absolute value < 1 LSB
  - Integral Nonlinearity (INL): < 1 LSB
  - Equivalent Number of Bits (ENOB) > 10.3
  - Overflow protection: When input signal exceeds the upper or lower ADC range, the output should be fixed at the maximum or minimum value.

ColdADC QC Procedure and Test Items based on DAT



Input info: Date, Time, Location, Tester,
DAT SN, Socket SN, Chip ID, and etc.

Basic functionality checkout to assure any chip is aligned in the socket, no short, no open pin

- Power cycle at least 5 times with different configs
- Test I2C communication (Write/read registers)
- Check power-on reset (verify default register values)
- Measure reference voltages
- Measure ring oscillator frequency
- Perform auto calibration; check weights
- Measure open channel noise (new DAT)
- Measure DNL/INL (slow ramp or sine wave input)
- Check overflow protection
- Measure ENOB (optional)

Verified doable on DAT

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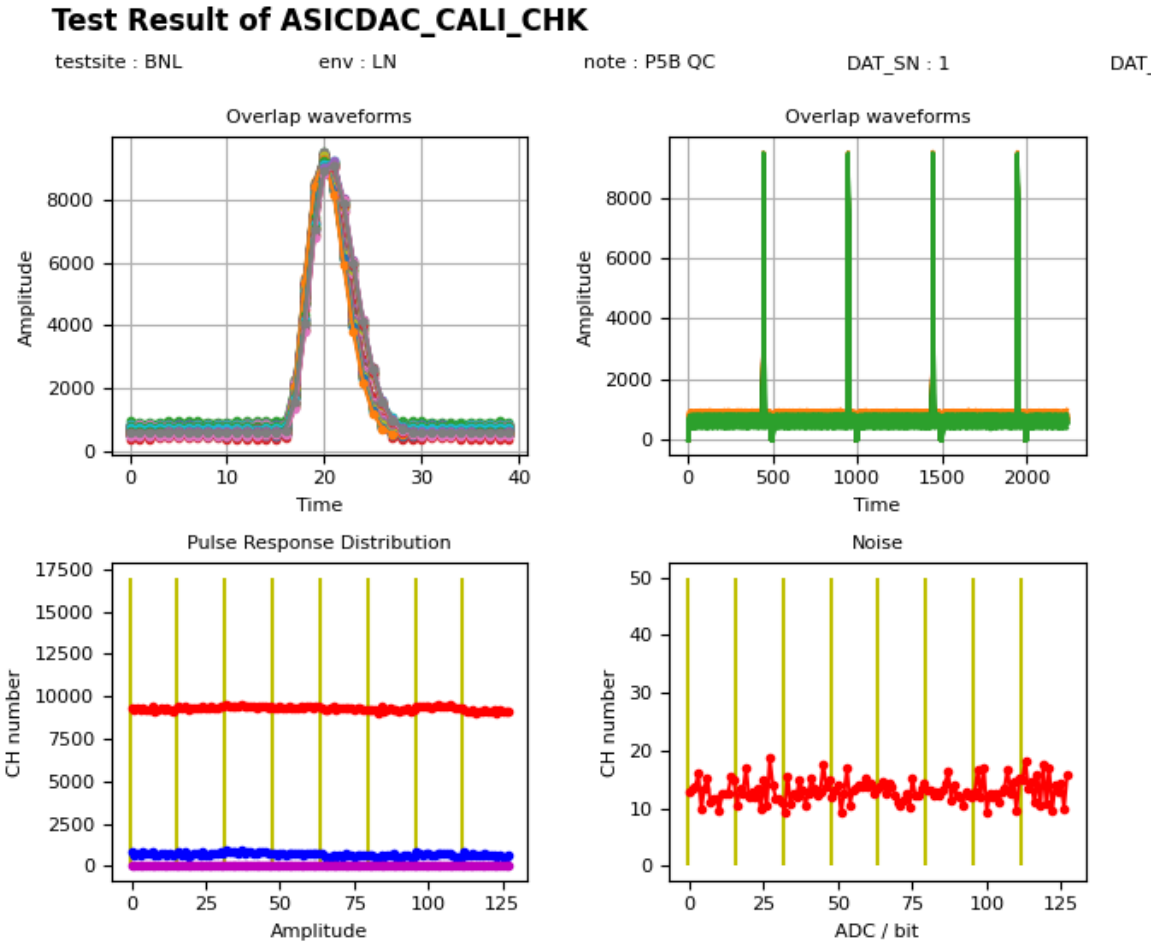
Initialization checkout

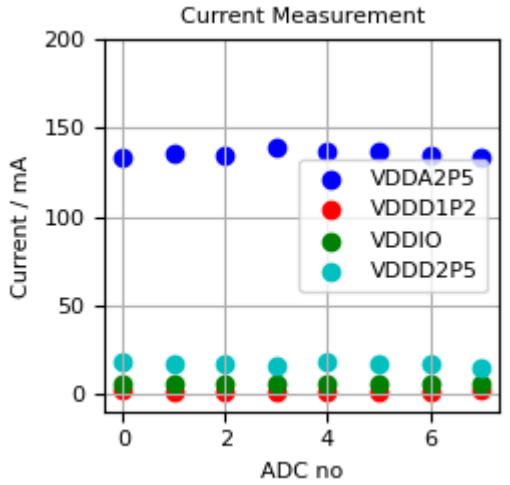
- Largely similar to current LArASIC initialization checkout
- Ensures chips are placed correctly and rules out nonfunctioning chips
- Checks power consumption, reference voltages, and readout from LArASIC (pulse shape, noise)



Data capture time: 1 minute

Power cycling measurement

- Power cycling is recommended for cold testing to screen out chips with potential (rare) start-up issue
  - Keep this test item in warm testing as well to make sure both warm/cold test follow the same testing procedure
- Checks if current draw changes accordingly under different input buffer settings
  - SDC on or bypassed
  - DB on or bypassed
  - Input signal treated as SE or DIFF



Current draw with SDC and DB off.

Data capture time: 3 minutes

I²C communication checkout

- Checks that registers have default values at powerup
- General I²C communication is necessarily verified during configuration for other tests

Register	Control Name	Description	Bits	Default = 0xFF
15 0x8F	**ibuff0_ctrl[7:0]**	200 µA nominal current source for input buffer. Current is 2 µA (257 – i_buff0_ctrl).	[7:0]	0xFF

Register	Control Name	Description	Bits	Default = 0xFF
16 0x90	**ibuff1_ctrl[7:0]**	200 µA nominal current source for input buffer. Current is 2 µA (257 – i_buff0_ctrl).	[7:0]	0xFF

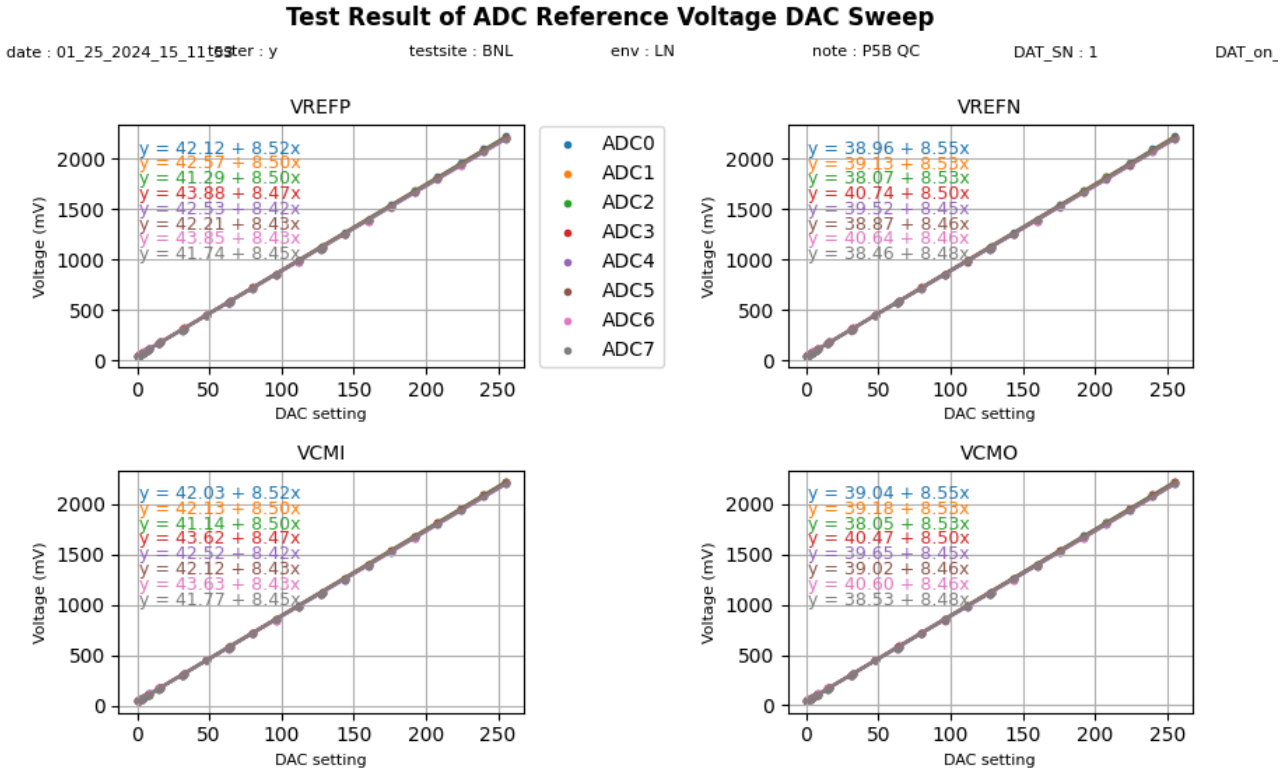
Register	Control Name	Description	Bits	Default = 0xFF
17 0x91	**i_vdac_0_ctrl[7:0]**	200 µA nominal current source for VDAC. Current is 2 µA (257 – i_vdac_0_ctrl).	[7:0]	0xFF

Register	Control Name	Description	Bits	Default = 0xFF
18 0x92	**i_vdac_1_ctrl[7:0]**	200 µA nominal current source for VDAC. Current is 2 µA (257 – i_vdac_1_ctrl).	[7:0]	0xFF

Data capture time: 1 minute

Reference voltage measurement

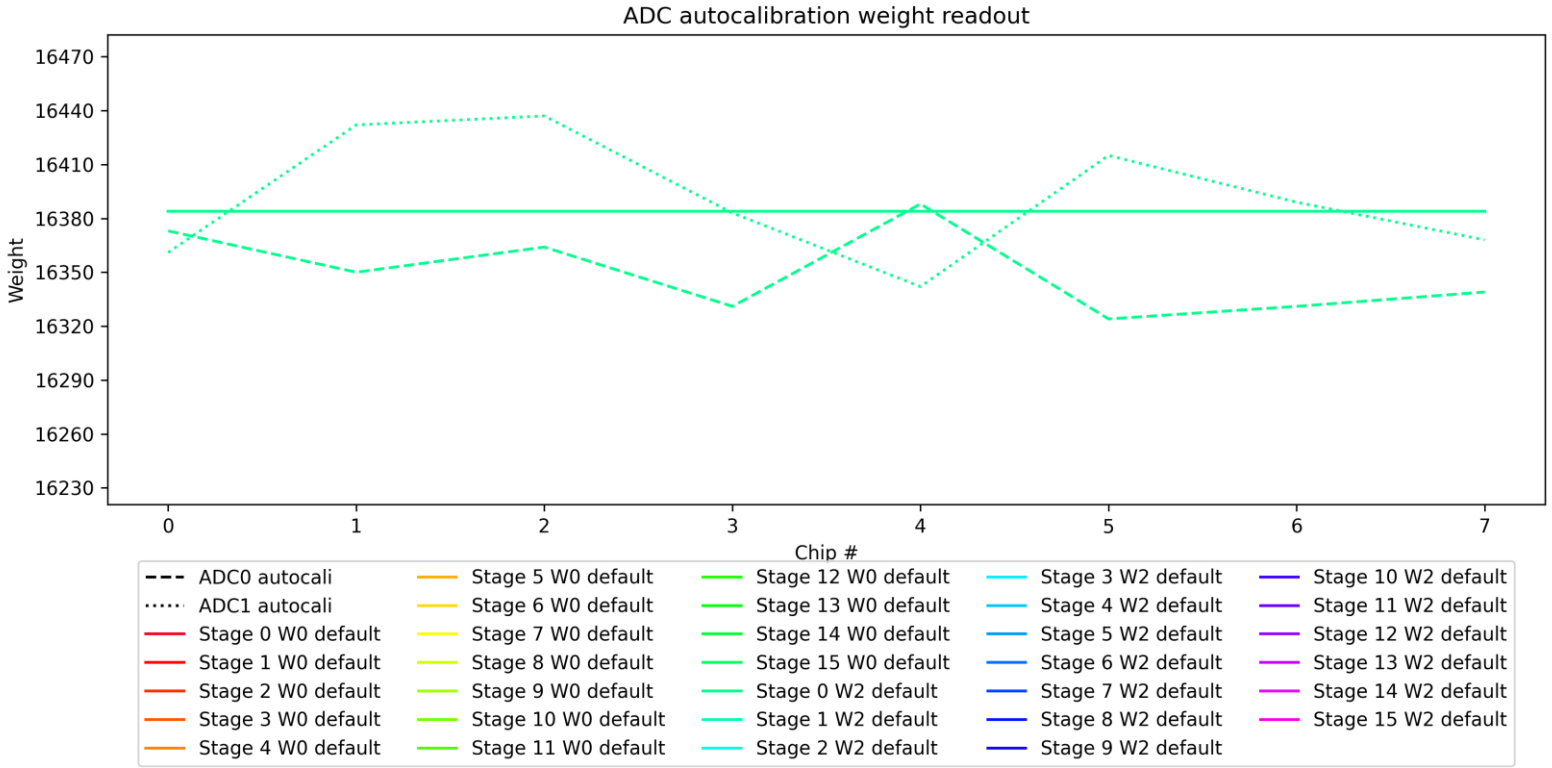
- Check current monitors and default reference voltages
- Evaluate linearity of reference voltage DACs



Data capture time: 3 minutes 40 seconds

Autocalibration check

- Run ColdADC autocalibration and readout the autocali weights subsequently stored in its memory



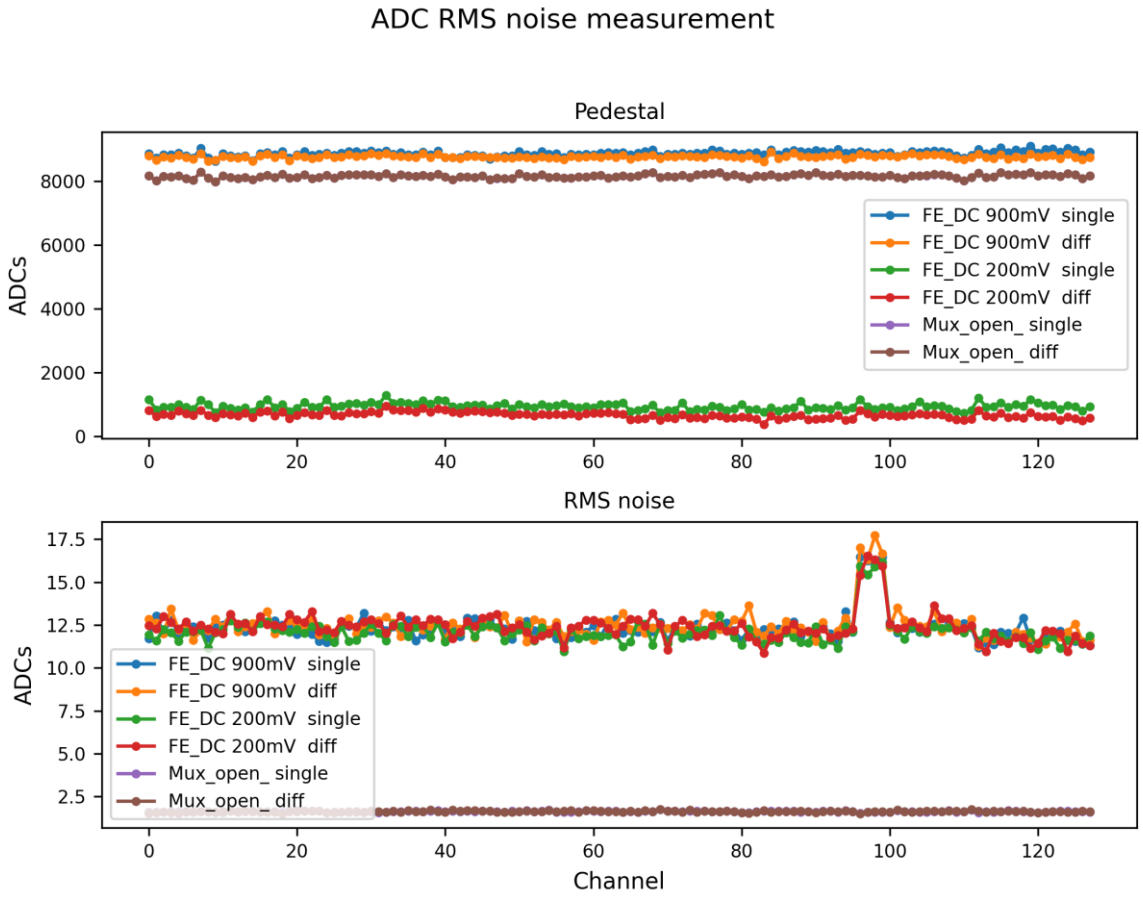
ADC Stage	W0	W2	ADC Stage	W0	W2
0	0xC000	0x4000	7	0xFF80	0x0080
1	0xE000	0x2000	8	0xFFC0	0x0040
2	0xF000	0x1000	9	0xFFE0	0x0020
3	0xF800	0x0800	10	0xFFF0	0x0010
4	0xFC00	0x0400	11	0xFFF8	0x0008
5	0xFE00	0x0200	12	0xFFFC	0x0004
6	0xFF00	0x0100	13	0xFFFE	0x0002
			14	0xFFFF	0x0001

Table 11: Default ADC pipeline stage weights.

Data capture time: 2 seconds

Open channel noise measurement

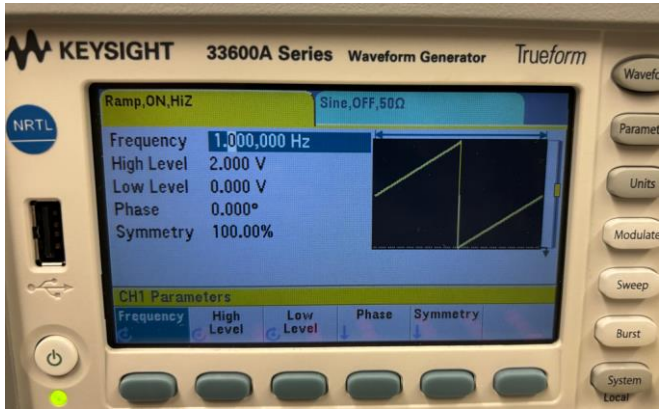
- Measure open channel RMS with single and differential buffer setting
- Original DAT does not allow channels to be completely disconnected from everything else (this is fixed in the upcoming revision)
  - Measure DC from LArASIC at 900 mV and 200 mV baselines
  - Measure open channel noise via mux input (channel X of each ASIC are tied together)



Data capture time: 30 seconds

Differential/integral nonlinearity (DNL/INL) measurement

- Looking for INL/DNL, missing codes
- Want ~100 samples/code → ≥1,638,400 continuous samples
- Sweep with a ramp (or a sine wave) from external waveform generator
  - Sampling rate of 2MHz & 100 samples/code → sweep period of 1 second



Sweep voltage across entire range of ColdADC

↓

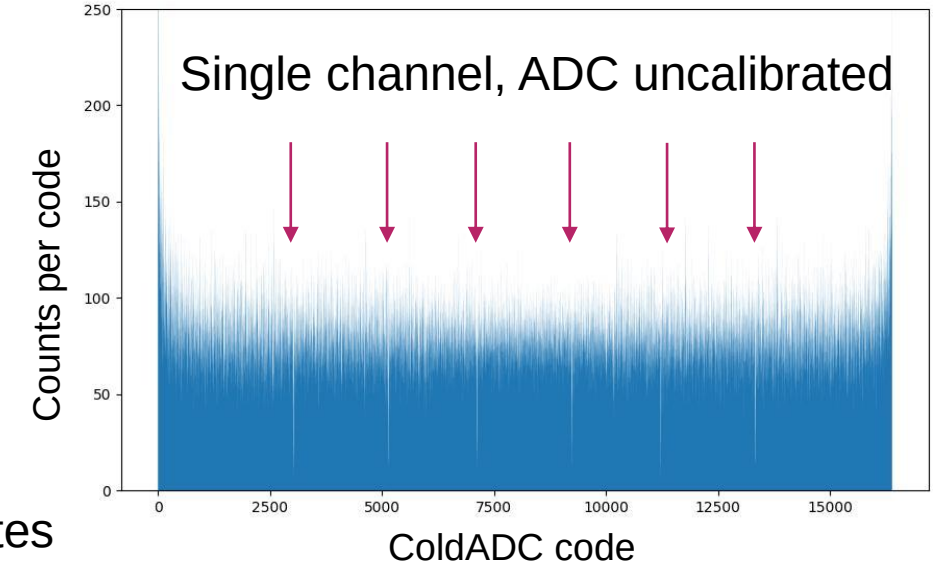
Read out ColdADC data

↓

Count # of samples per code per channel

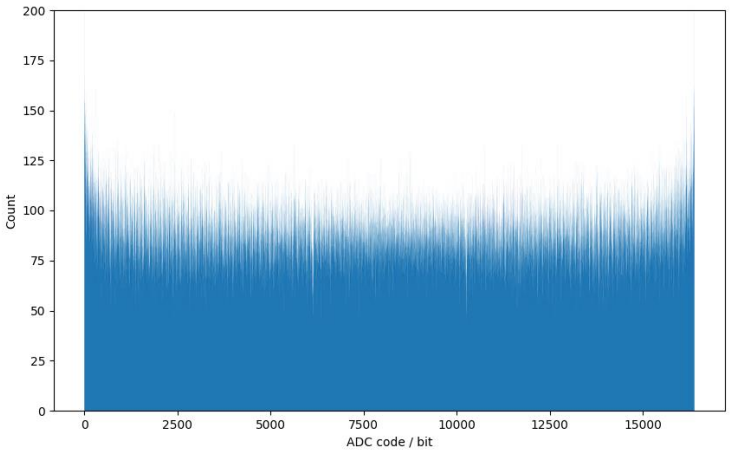
↓

Normalization → INL/DNL (ongoing)



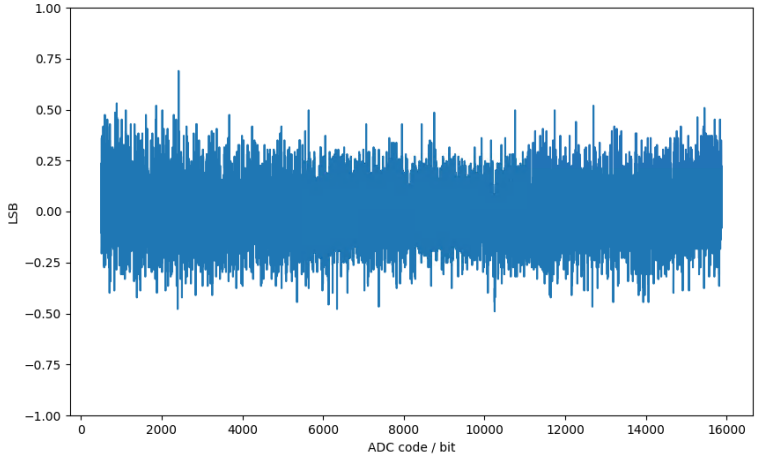
Data capture time: 3 minutes

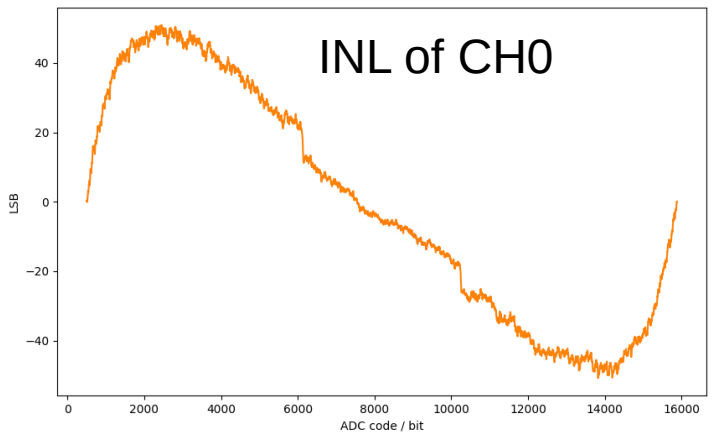
DNL/INL measurement - Normalization (preliminary, w/ ColdADC calibrated)



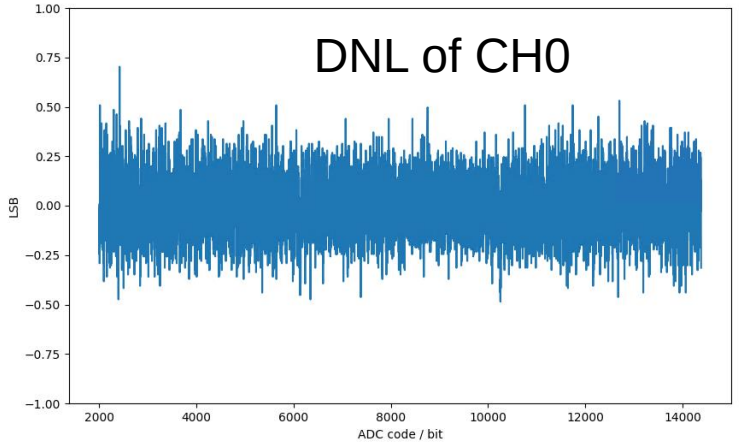
Histogram result of CH0

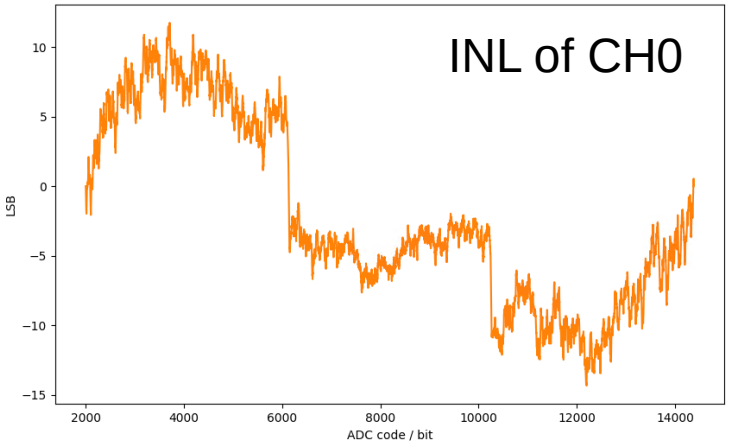
Note: Ramp signal is applied to all 128 channels simultaneously.





ADC code [500,15884]



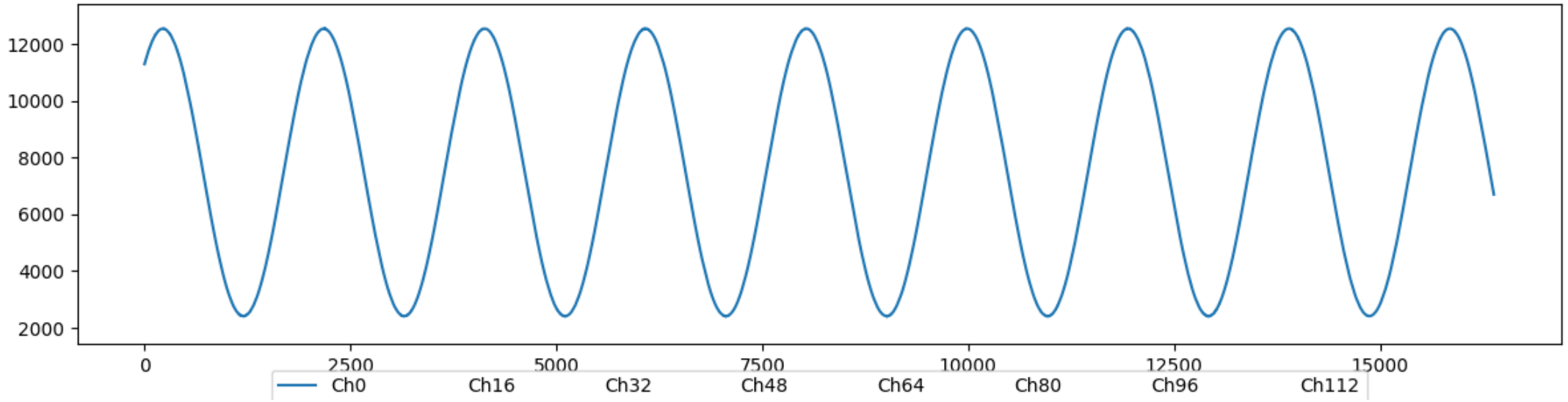


ADC code [2000,14384]

Data capture time: 3 minutes

Effective number of bits (ENOB) measurement

- Inject a sine wave into the ColdADC inputs
- Use WIB single-channel buffer firmware to capture 16,384 continuous samples of each channel (consecutively)



Note: Performance of ENOB testing is under development

Data capture time: 4 seconds

Ring oscillator frequency readout

- Read out ColdADC ring oscillator frequencies as have been measured in DAT firmware

Example readout at room temp:
ADC0: 15.285402 MHz
ADC1: 15.321691 MHz
ADC2: 15.200986 MHz
ADC3: 15.831096 MHz
ADC4: 15.486661 MHz
ADC5: 15.517424 MHz
ADC6: 15.897482 MHz
ADC7: 15.565368 MHz

Process Corner	-200 C	27 C
Slow-Slow	18.4 MHz	16.1 MHz
Typical-Typical	24.2 MHz	18.9 MHz
Fast-Fast	34.9 MHz	22.5 MHz

Table 6: Oscillation Frequency

Data capture time: 2 seconds

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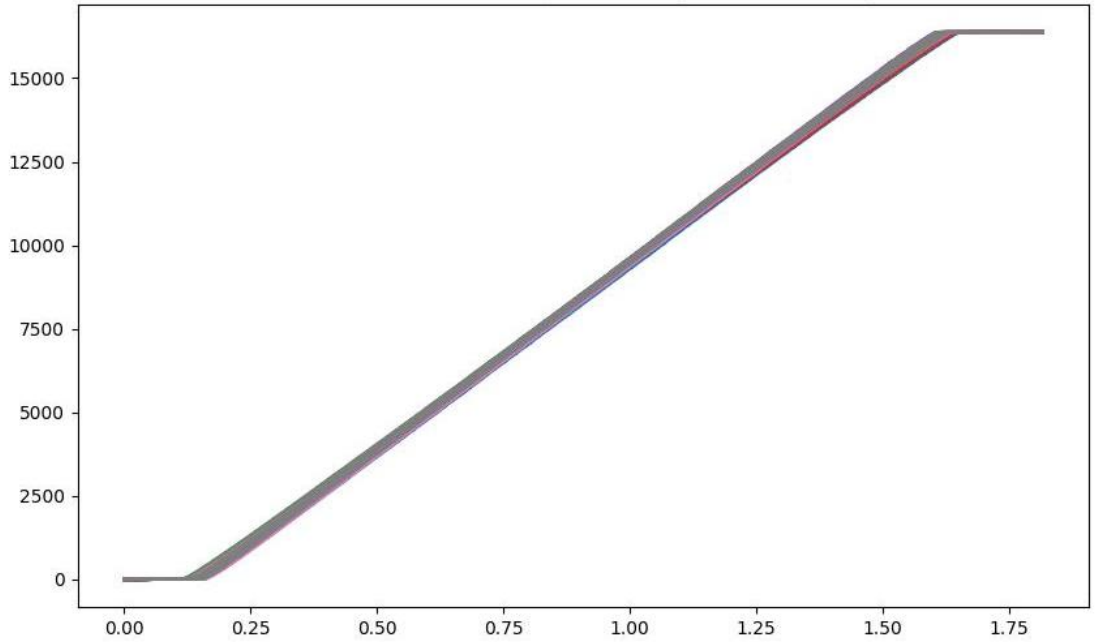
Gain and overflow test

- Inject a 200 Hz ramp waveform (0-2.0V) into the ColdADC inputs
- Use WIB single-channel buffer firmware to capture 16,384 continuous samples of each channel (consecutively)



Further analysis is undergoing to extract some ADC performance metrics, such as DC offset, range of input, overflow

Data capture time: 3 seconds

To-do list

1. Verify and finalize QC scripts
- Script is being verified on the original DAT board.
- Revised DAT board is expected to deliver optimized hardware performance

2. Update DAT FPGA FW for the revised DAT board

3. Complete analysis scripts for QC data
- Generate QC report for each ASIC
- Build pass/fail criteria

4. Database
- Export readable format (json file) for hardware database

5. QC data backup

…= Total data taking time of ~12.35 minutes

Summary

- Data taking QC scripts for ColdADC based on DAT board is basically complete
  - To be verified with small batch of ColdADC chips
- Scripts for data analysis are to be finalized