

# Pixel Detectors in a Muon Collider Environment

Inaugural US Muon Collider Community Meeting  
Aug 08 2024

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# Introduction



- Requirements of **muon collider environment are clearly unique** and can not simply build on LHC (and similar) experience
- We all know the culprit: **beam induced background (BIB)**
- Tracking detector and primarily the innermost layers will have nearly all of their **technical requirements driven by BIB**
- Goal of this talk:
  - Highlight differences of HL-LHC and MuC environment from **Pixel detector perspective**
  - No solutions to many questions, but will try to **highlight aspects that are very different to HL-LHC** and therefore require more R&D
  - Will try to point out how the MuC environment will require **co-design of detector hardware and simulation**
  - Exciting new R&D domains, how can we get started? -> **4D Pixel detector demonstrator**
- Will focus on front-end readout chip design (somewhat biased towards ATLAS, but fundamental design is identical/similar for CMS) as it typically builds the backbone of the tracking detector system



# Primer: State-of-the-art Pixel Detectors

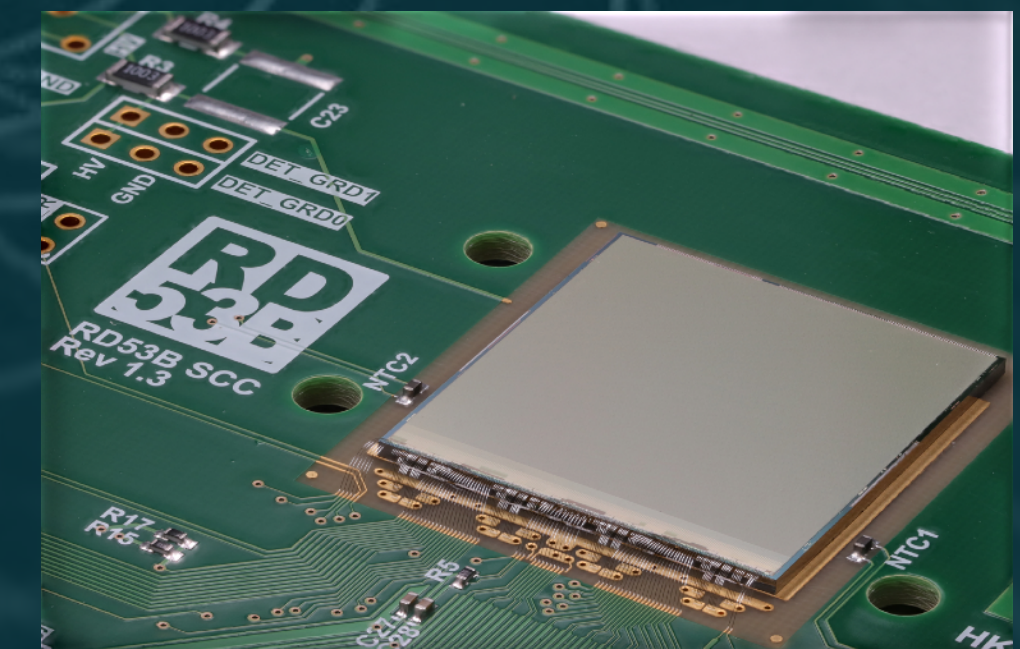
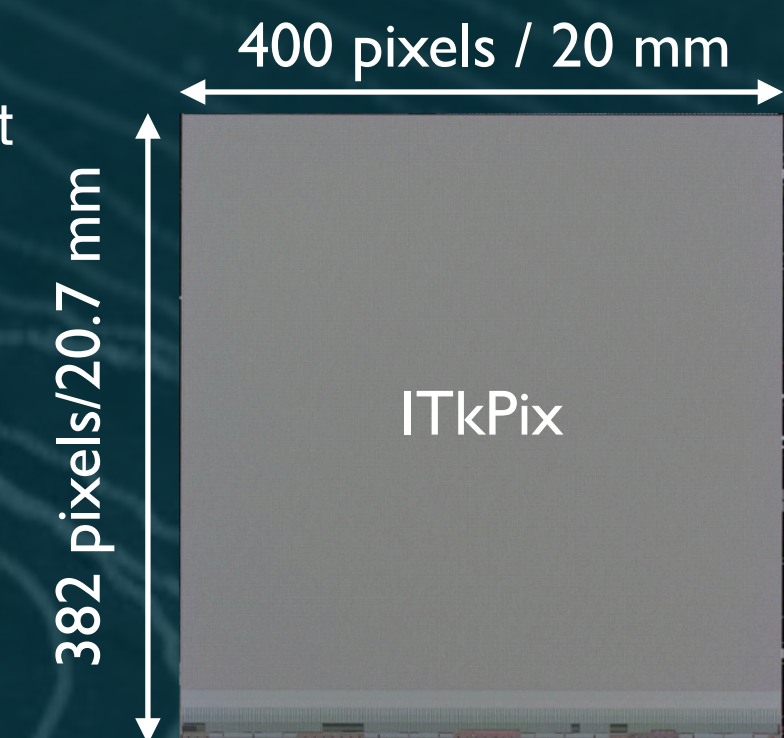


- For the ATLAS and CMS HL-LHC Pixel detector upgrades the RD53 collaboration was formed and tasked with designing and testing the Pixel detector readout chips
- Great idea to form a **cross-collaboration R&D group!**
- On average **20 FTE** engineering and scientist effort required to fulfill the task!
- Task **so complicated that design was delayed nevertheless** (~2 years) and had to deny collaborations advanced features (e.g. ROI readout)
- Design **specs well known at start** as extrapolation from LHC environment and primary drivers were increase in multiplicity, granularity, and radiation tolerance

## ITkPix Readout Chip:

- Designed by RD53 Collaboration in 65nm CMOS
- Same design library has been used for CMS readout chip

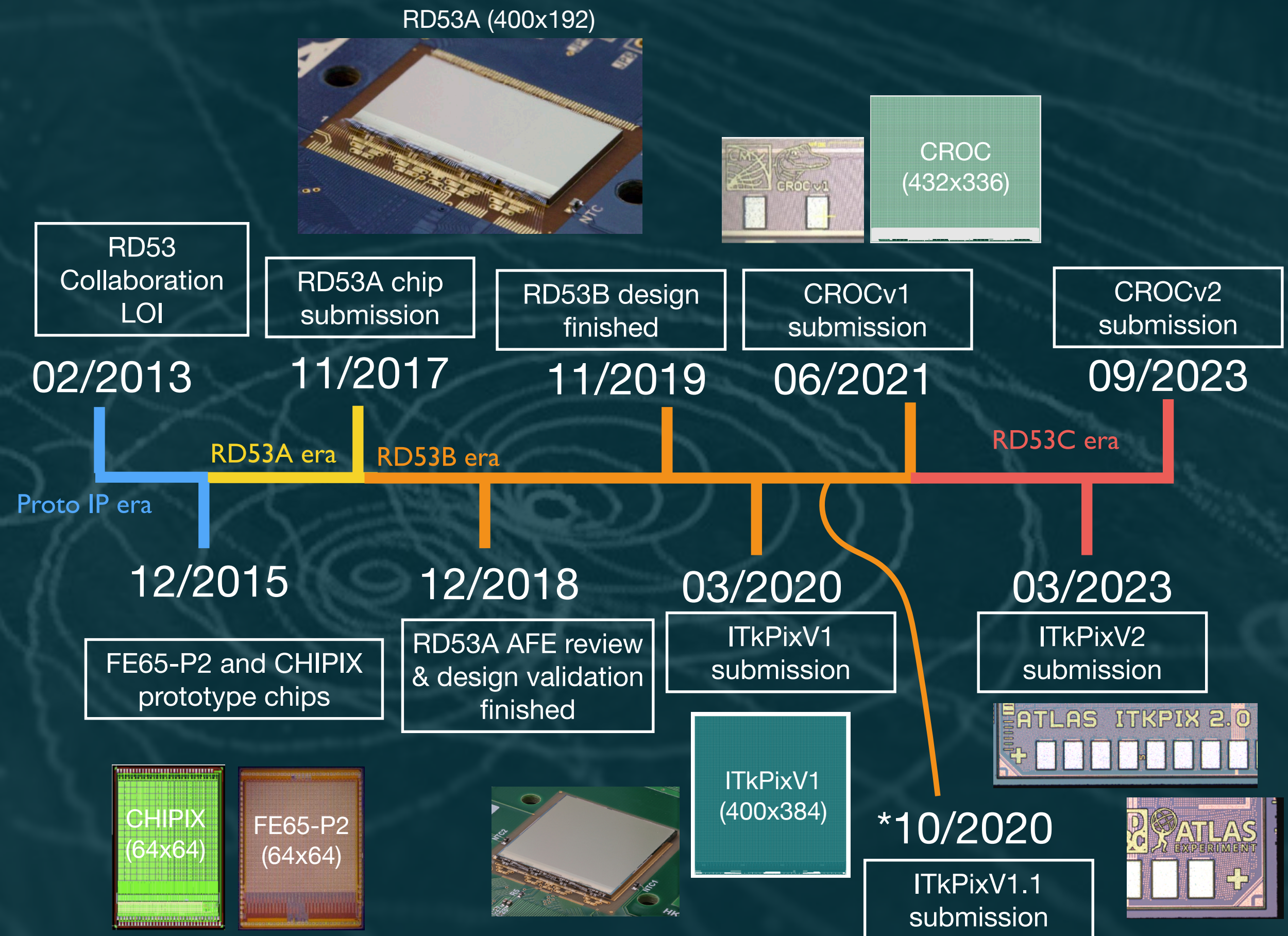
Parameter	Value
Technology	65nm
Max. hit rate	3.5 GHz/cm <sup>2</sup>
Trigger Rate	1MHz
Trigger Latency	12.5us
Pixel size (chip)	50um x 50um
Pixel array	400x384
Chip dimension	20mm x 21mm
Detector Capacitance	<100fF
Detector Leakage	<10nA
Min. threshold	<1000e
Radiation Tolerance	1Grad @ -10C
SEE Tolerance	<100Hz/chip
Power	<1W/cm <sup>2</sup>
Readout data rate	1-4 links @ 1.28Gbps
Temp. Range	-40C to +40C





# Readout Chip Design Time

- Full design cycle took **10 years** to arrive at Production Chip
- Specification/Requirements did not change in a significant way from their definition at the start
- E.g. analog front-end architecture did not change since early prototypes in 2015, memory architecture nearly identical to ATLAS Phase 1 upgrade
- Final chip architecture finalized with “RD53B”, **another 4 years necessary to fix all bugs** and other issues found
- Chip verification relies on well defined set of requirements and how the chip will be operated -> tough to figure out a-priori
- **In-silicon testing** as close as possible to final operational conditions is **vital!**
- But chip submissions are costly (\$\$ and time spent on final assembly and not design)





# Lessons Learned

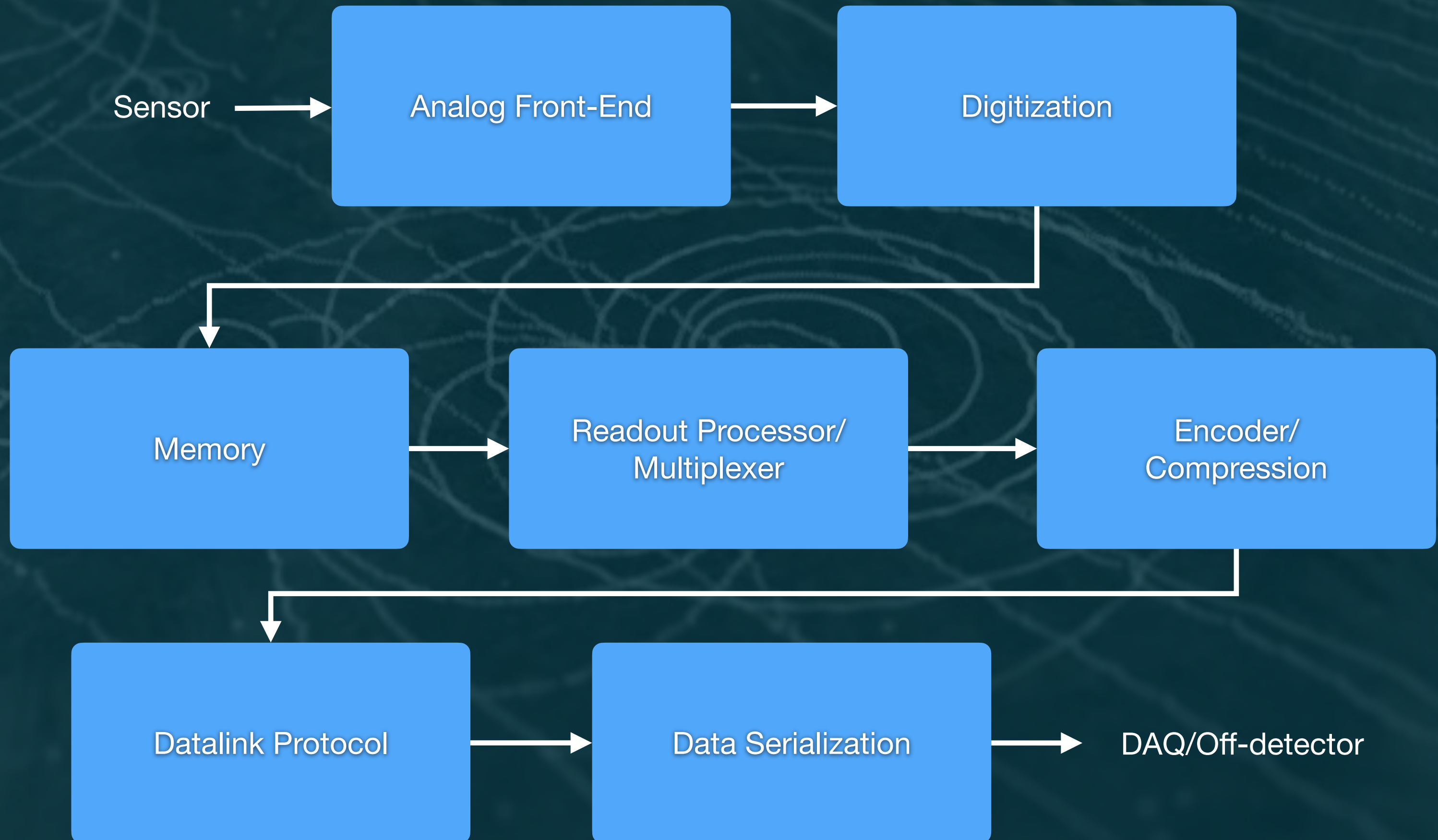


- It's "easy" to make a prototype to demonstrate specific features, it's **really hard** to **combine all features** and **proof they will work reliably**
- RD53 spent around 4-5 years **not "designing" but rather understanding what has been designed** and making sure it works as any issues found at a later stage will have massive impact on detector production schedule
- **Even small and easy to fix bugs, can lead to massive delays** as the process of synthesis, place and route and time closure is not automatic but heavily relies on (expert) human guidance
- The more **feature complete early prototypes** are the higher the chance to find systematic issues early
- Long design time requires **designers/experts to be available for a long time**
  - Expert personnel leaving the collaboration or moving on to other projects had massive impact on design time
  - Either need to build this into the schedule (how to anticipate?) or need to **create a sustainable design model**



# Information Flow in Pixel Detectors

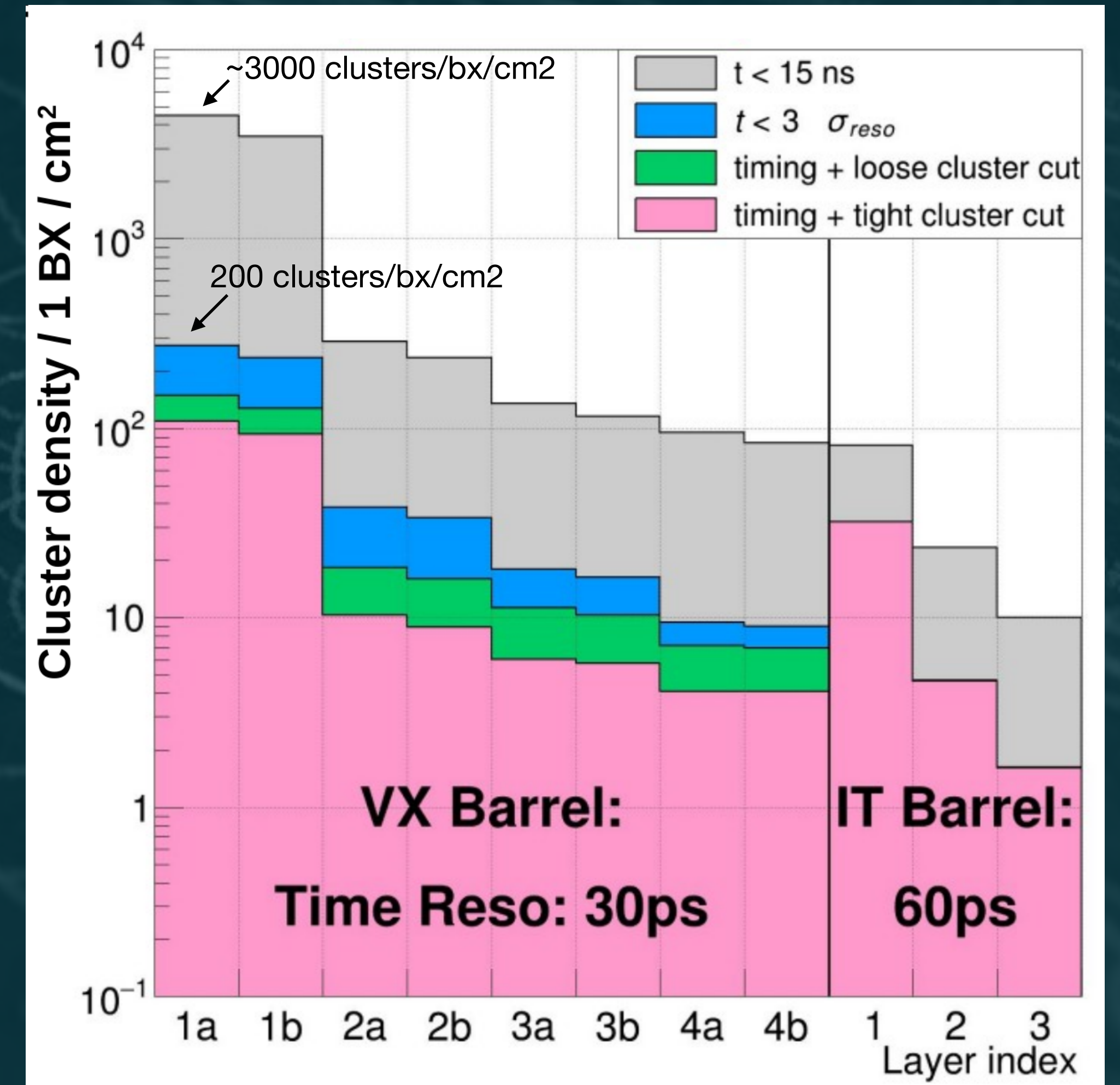
- Charged particle deposits energy in sensor, traditionally by excitation of electrons
- Analog front-end contains pre-amplifier and discrimination
- Digitization converts analog quantity (charge, time of arrival) in digital domain
- Hit information needs to be saved for some time, until readout processor retrieves hit data and combines it with all other hits from event
- Varying amount of compression is applied
- Data is contained in a link layer protocol and serialized
- DAQ has to undo serialization and compression





# Hit Rates

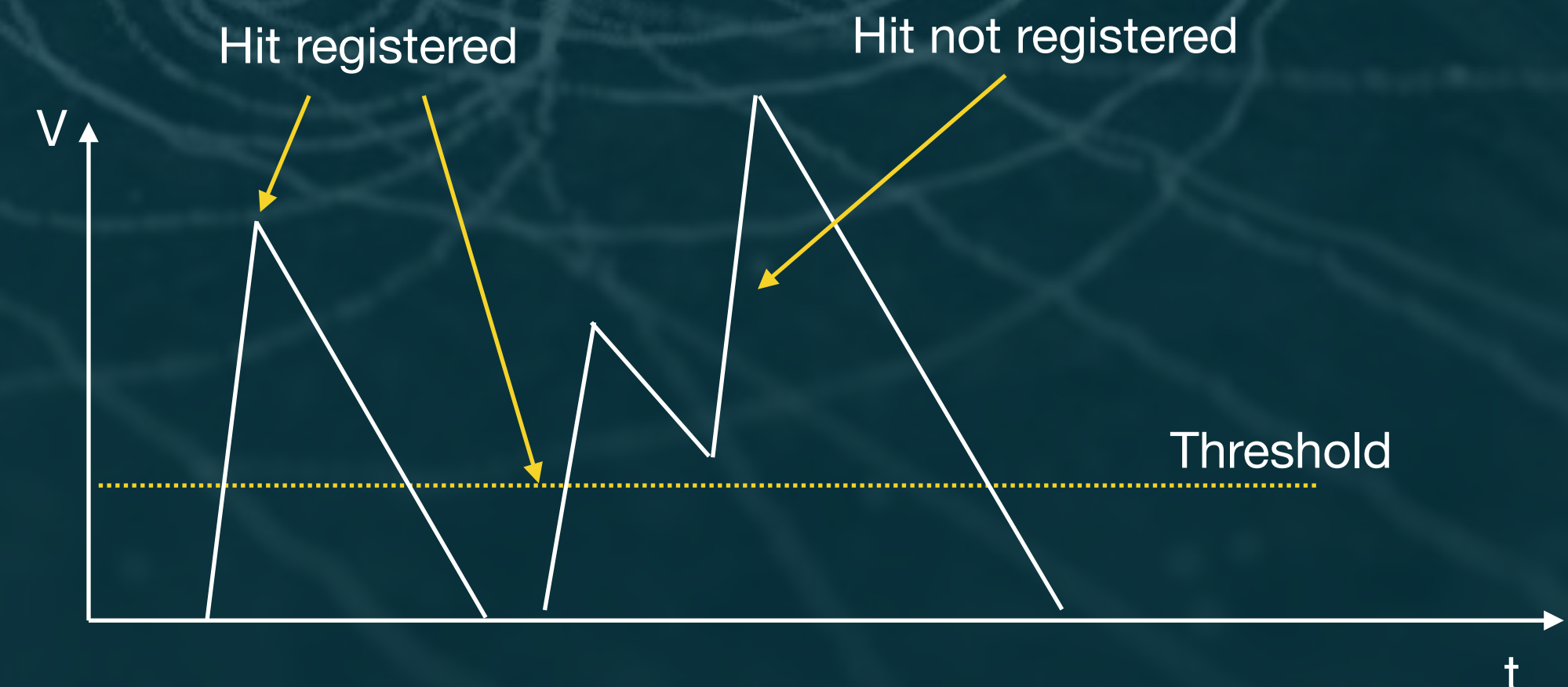
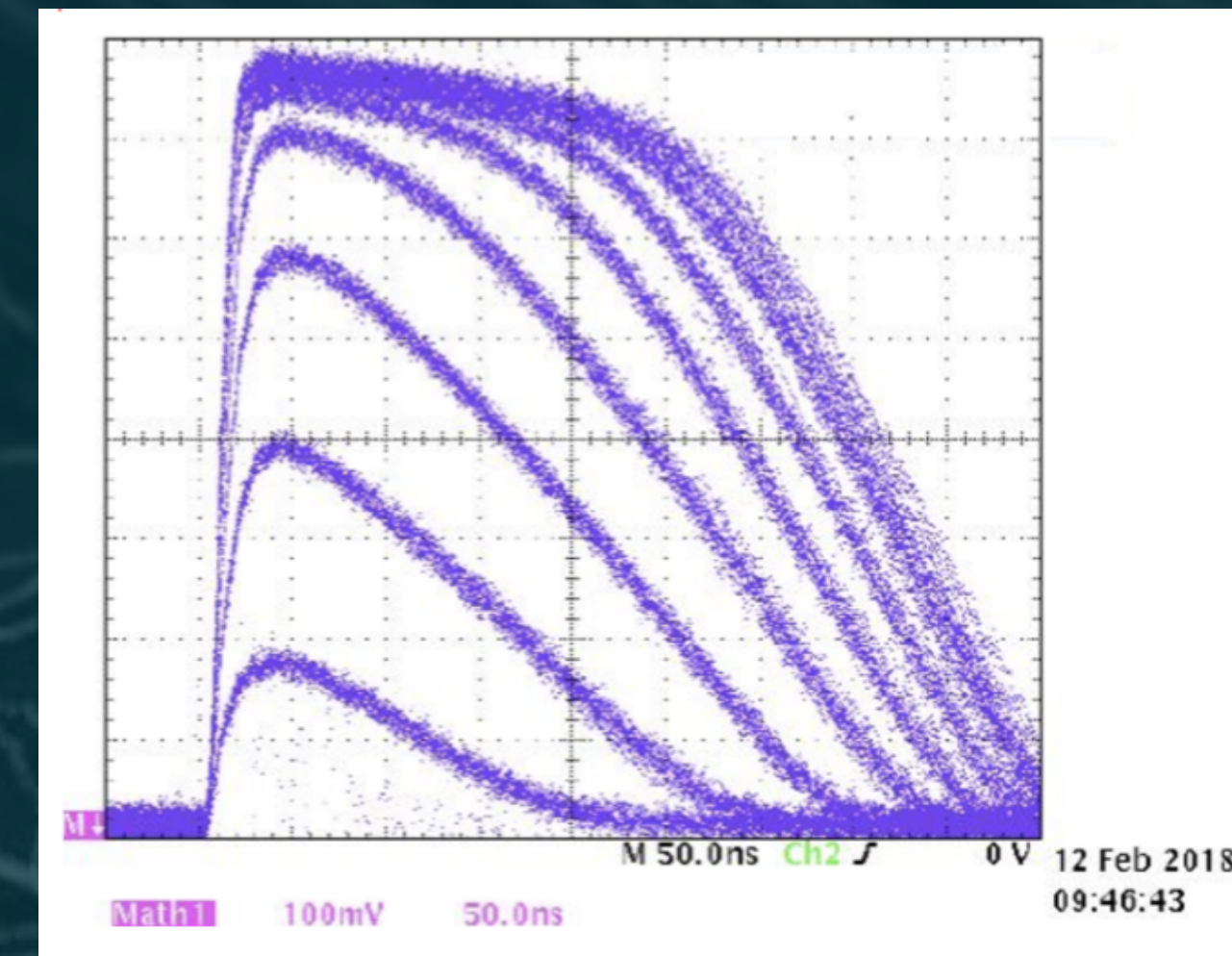
- In HL-LHC conditions hit rate is 3GHz/cm<sup>2</sup> (innermost layer)
- This translates to 75 hits per bunch crossing (25ns)
- For a 50um by 50um pixel detector that results in 0.2% occupancy
- Average return to baseline is around 150ns (6 bunch crossings) -> 1.2% of channels “busy” at any given time
- MuC conditions rather different
  - 3000 clusters/bx/cm<sup>2</sup> (bunch crossing = 10us), average cluster size ~12 (dominated by BIB) -> **36k hits -> 3.6GHz/cm<sup>2</sup>**
  - But should actually consider all 36k hits occur within 15ns!
  - For a 25um by 25um pixel detector that results in **22% occupancy!!**
  - Assuming we can ignore everything except **90ps around t<sub>0</sub>** -> 200 clusters/bx/cm<sup>2</sup> -> 2.4k hits -> **1.5% occupancy**
  - Timing cuts are applied after processing, detector “sees” all hits!
  - Close interaction with detector simulation required!





# In-Pixel Pileup

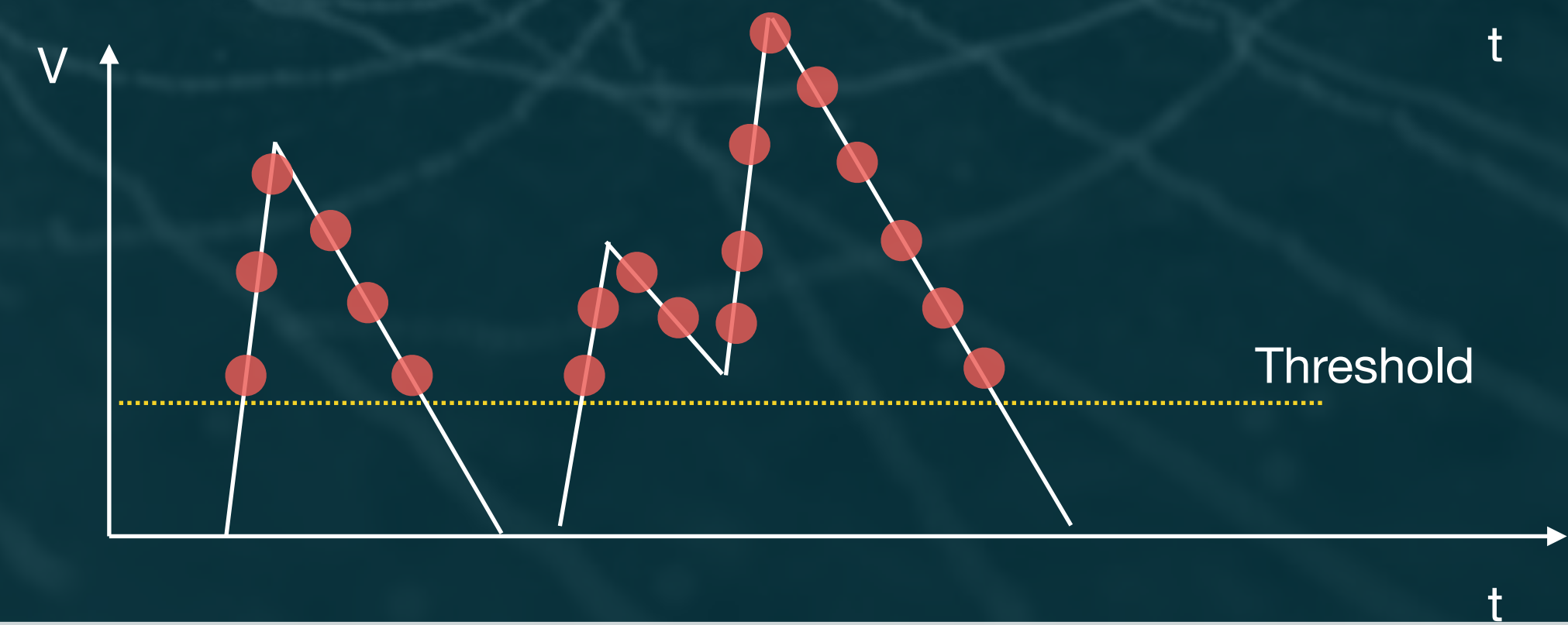
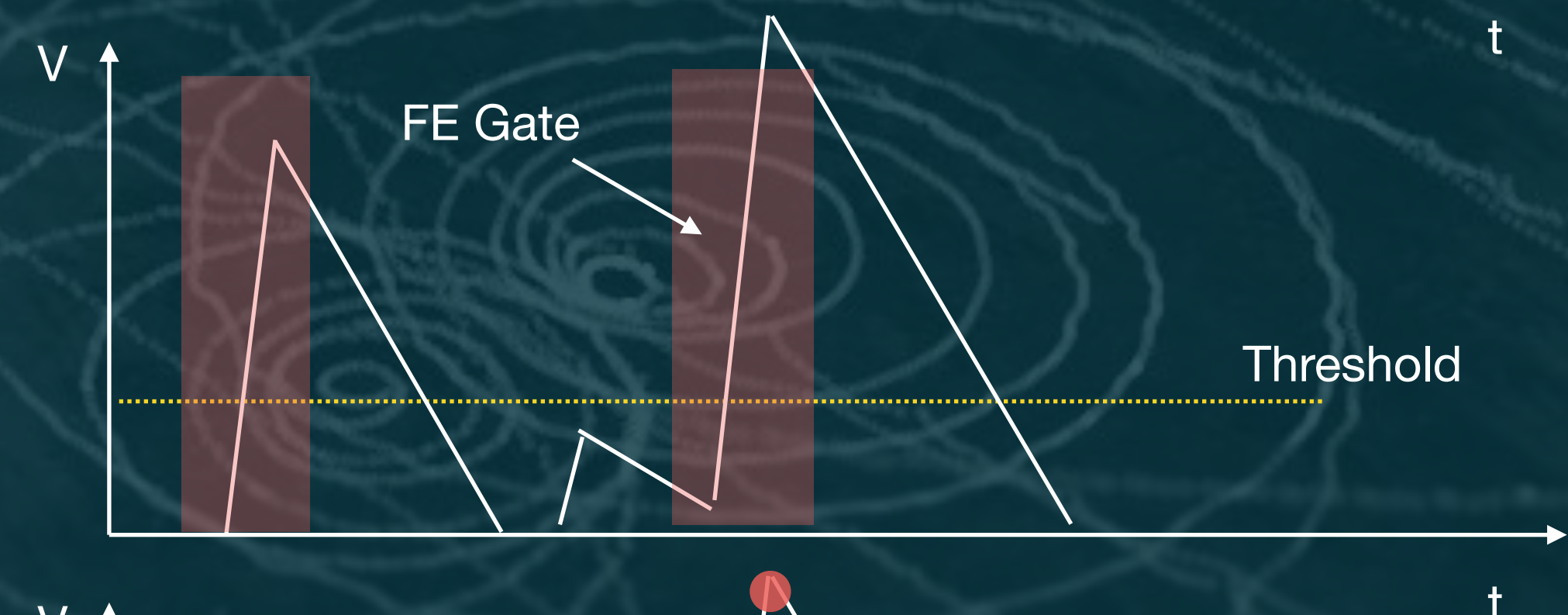
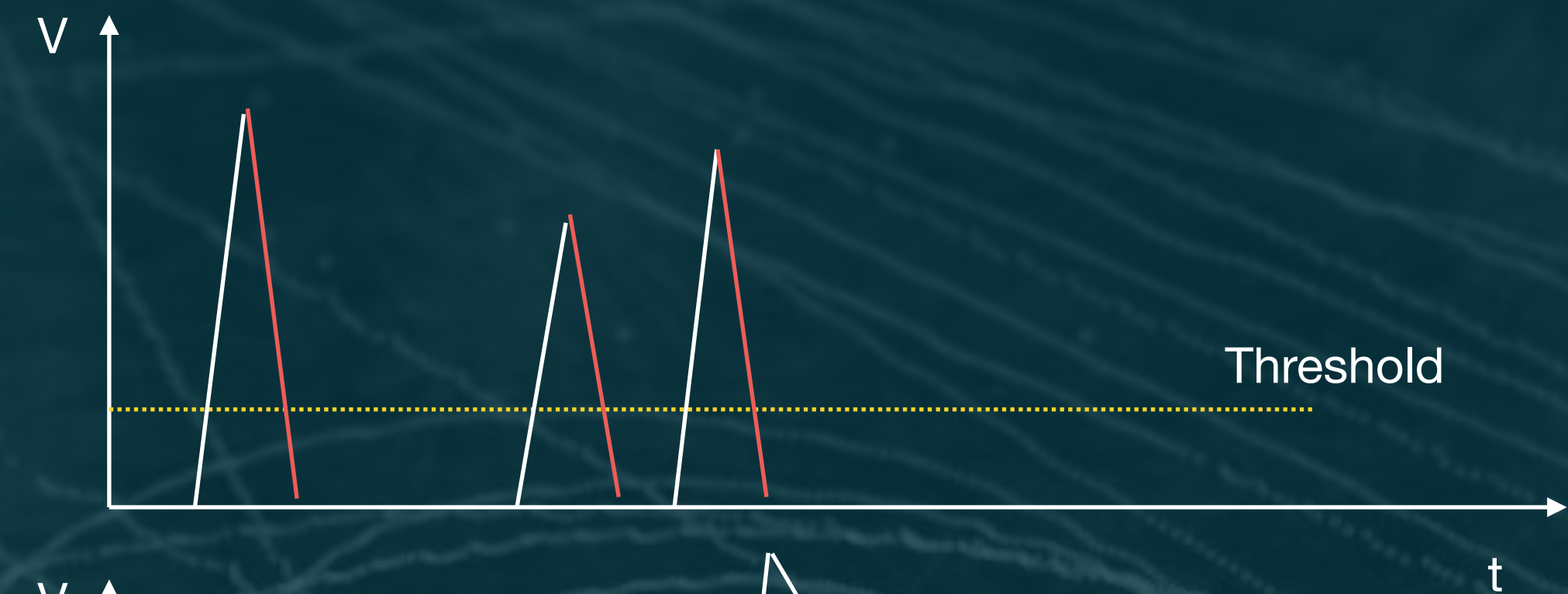
- For HL-LHC readout chip have to consider **return to baseline of signal**
- Constant reset front-end architecture allows Time-over-Threshold (ToT) to be proportional to charge. ToT counted with main 40MHz clock (25ns resolution)
- Hits are registered when they pass above threshold, hits that occur in a pixel that has not returned below threshold are lost. This is called **“in-pixel pileup”**
- While timing cuts in MuC conditions cut down heavily on overall occupancy, detector still sees all hits
- In-pixel pileup will lead to reduced efficiency and could muddle timing precision we can achieve
- I.e. **MuC conditions need to be accommodated at the earliest readout chip stage!**
- The total amount of energy deposited within a very small time frame might also have adverse affects on sensor efficiency





# In-Pixel Pileup II

- What to do?
  - Natural instinct might be to **make return to baseline faster**
    - 4D pixel detector need very fast front-ends to capture time accurately (fast rise time), this naturally shortens the ToT but not to the degree required to cut down on in-pixel pileup
    - Shorter ToT also requires faster clocks to count ToT (more power) and will likely negatively affect charge resolution
    - Time-of-Arrival (ToA) uses ToT to perform time walk correction -> worse ToT -> worse ToA?
  - Could **“gate” front-end** (e.g. modulate pre-amp bias)
    - Major architectural change compared to the past -> R&D necessary
  - **Change digitization fundamentally?**
    - **Full waveform sampling** -> incredibly demanding in terms of power/ noise/space, but gives all information
    - Increased information density could be processed on-chip with ML techniques -> major advancements in this field in recent decade
      - General issue with ML techniques: **how to reduce risk when ML architecture is fixed in-silicon?**





# Digitization



- ToT method has been proven useful in LHC/HL-LHC environment
  - Enables low power electronics while also delivering analog information about particles that can improve tracking beyond binary hit data and be used in specialized dE/dx analyses
  - Current methodologies simply **add ToA to existing ToT architectures**
  - Might want to take a step back and consider: **what information of the signal waveform is most useful** to discriminate between signal and BIB?
  - Current simulation already performs some level of digitization, fundamentally biases us in evaluating importance of information
  - Start a dedicated campaign between hardware and simulation experts to **understand which features of the sensor signals are most useful in MuC environment**
    - E.g. current effort to explore different sensor thickness to exploit dE/dx difference between signal and BIB
  - Result will guide instrumentation R&D, but critically need to keep iterating to stay close to reality!
- > **Instrumentation R&D/Detector Simulation Co-design!**



# “Triggering” and Timing



- HL-LHC has high repetition rate, so even though hits per bx are much lower, average hit rate is similar to MuC environment (~3 GHz/cm<sup>2</sup>)
- Raw data bandwidth required to transmit everything approx 60 Gbps/cm<sup>2</sup> (120 Gbps with timing information)-> **Need to reduce data amount!**
- **For HL-LHC use triggered readout** at ~1/40 (1MHz) of the original bx rate -> Not suitable to MuC with 100kHz rep rate, **want “streaming” readout** for best physics efficiency
  - Triggering different bunch crossings (in order) is a (relatively) simple task
  - Can we read everything out in on bx? If not need some amount of memory!
- Need timing cuts to cut down on hit multiplicity ... **on chip picosecond level timing cuts?**
  - Side effect: don't need to transmit ToA off detector with large dynamic range
  - Assuming **90ps timing cut data rate is approx 5Gbps/cm<sup>2</sup>** -> manageable! (Factor ~5 difference to HL-LHC)
  - How to accommodate time-walk? On-chip time walk correction?
- Are on-chip timing cuts to this level realistic (or what R&D needs to be done to get there)?

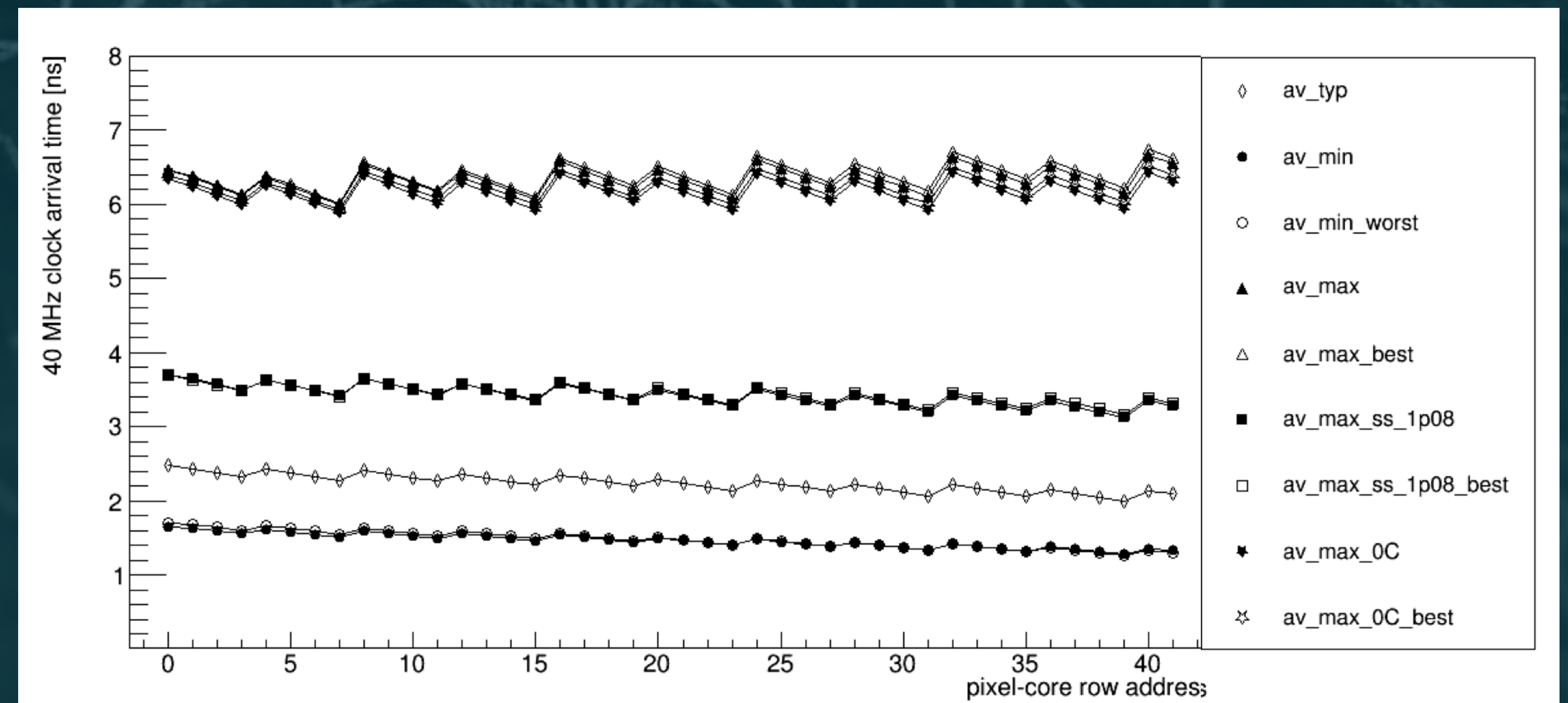
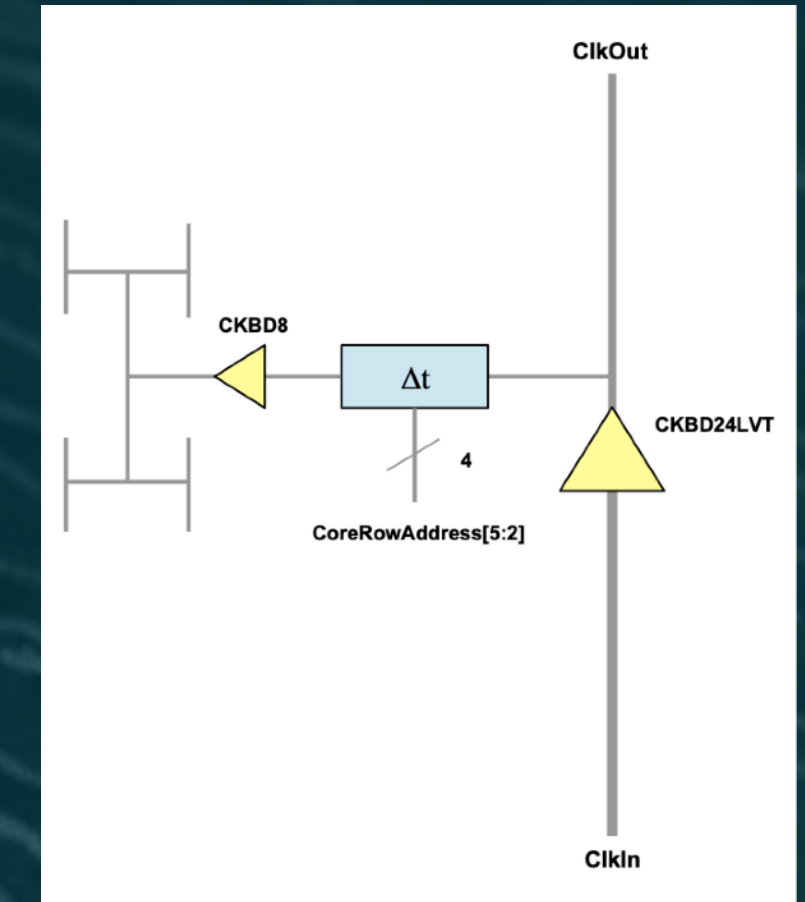


# On-chip Timing



- How to achieve **10 picosecond level synchronization** on-chip?
- Cannot use typical clock distribution trees due to pixel column architecture
- RD53 type chips synchronize the 40MHz clock across all pixels via custom delays to the 100ps level
- Critically also needs to be applied to calibration signals!
- **Delay cells highly dependent on environmental conditions:** temperature, radiation, powering, process corners
- Is it possible to push this down further?
- Do the tools allow us to do this routinely during final chip layout assembly?

- 115 ps RMS in TYP corner
- 95 ps RMS in MIN corner
- 166 ps RMS in MAX corner

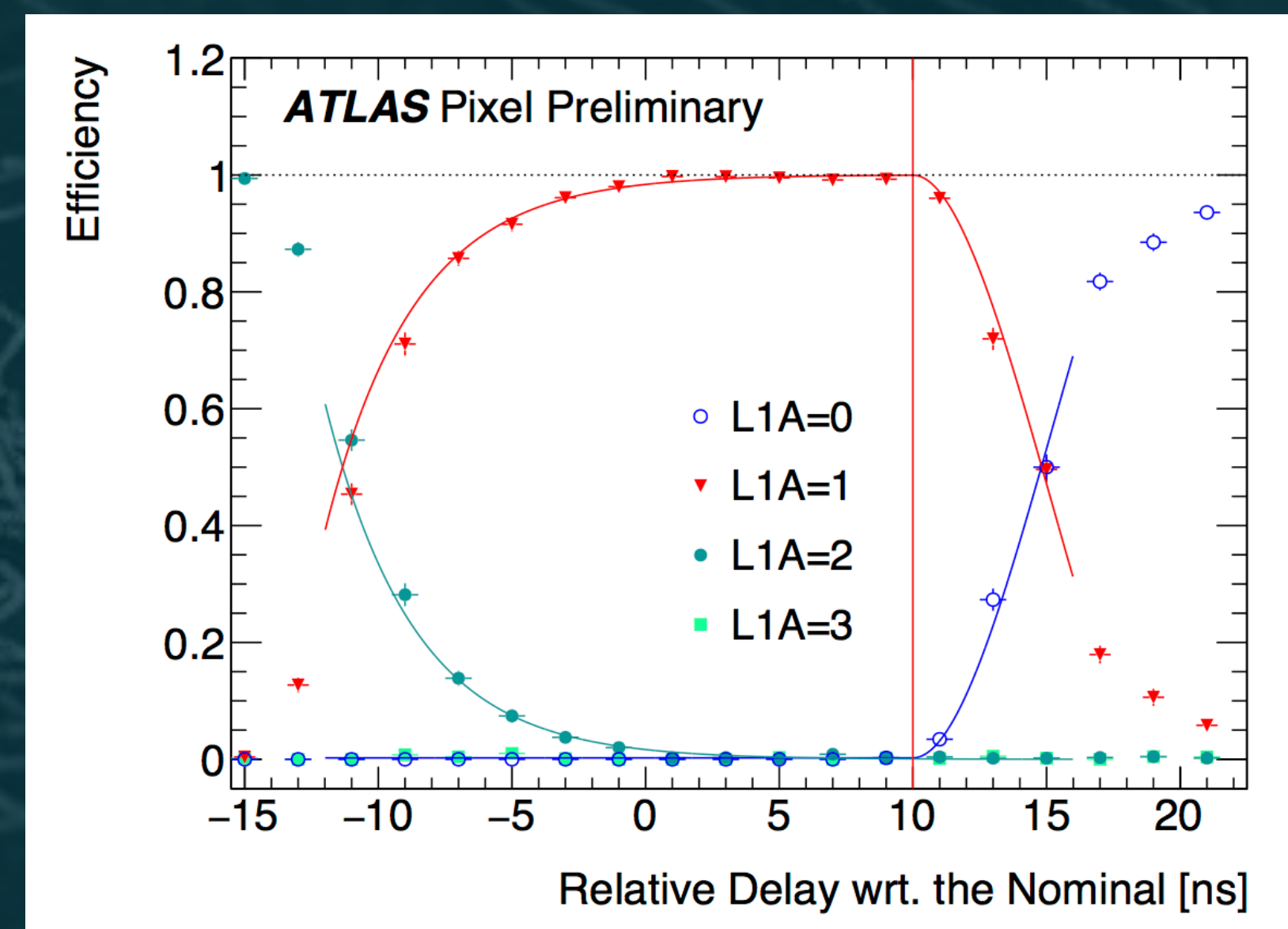




# System Synchronization



- Current **detectors timed in with collision events** by accommodating varying clock skew of each detector element with local delays
- Is this still possible at the MuC?
- Generally speaking though we have been avoiding “global signaling” and try and rely more on “local signaling” to improve reliability during operation
- Example: localized trigger tagging overcomes issue of keeping bx counters synchronized
- Could we **determine  $t_0$  on-chip dynamically**?
  - If we have discriminators other than timing could use those to find timing window: **cluster size/shape, charge, double layer stub angle, ...**
  - Could this be applied even within one chip to reduce on-chip timing constraints?

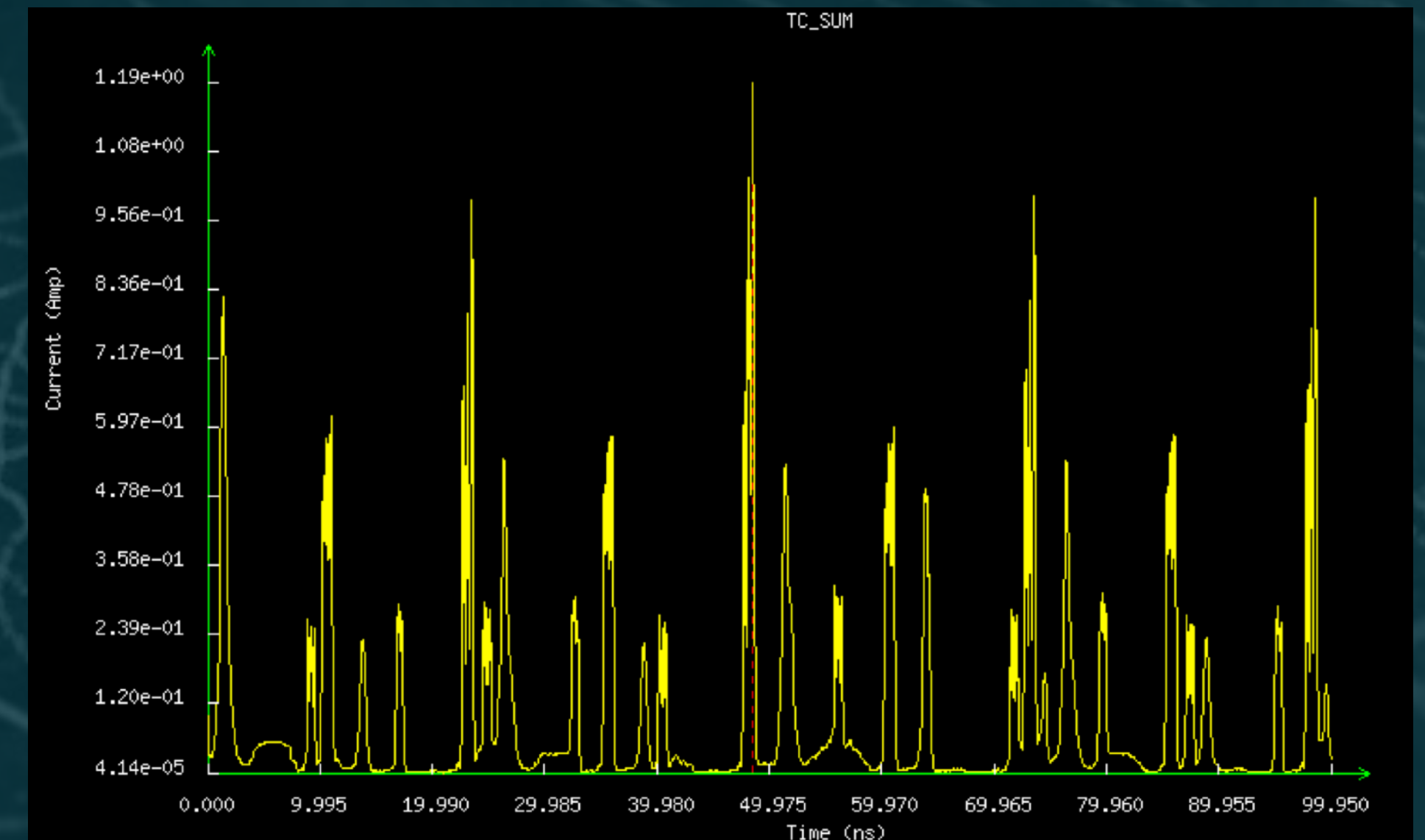




# Timing and Power



- In RD53 chips hit and trigger activity induced **digital current at 3GHz/cm<sup>2</sup> hit rate and 1MHz trigger is 23% of total current (~5uW per pixel)**
- This is by design! **Total power is reduced by only clocking those parts which are actively processing!**
- In MuC environment to reject hits with a timing cut, need to **measure time of ALL hits**
- **Low Power TDC** architecture critical to achieve this!
- For comparison ALTIROC (ATLAS timing layer front-end chip) which delivers 30ps time resolution needs 4mW per channel\*
- Considering 22% occupancy in 15ns window: **activity driven power reduction not sufficient anymore?**
- Cluster timing? Early abort TDC?
- Somehow utilize long “dead” time and stagger measurements?

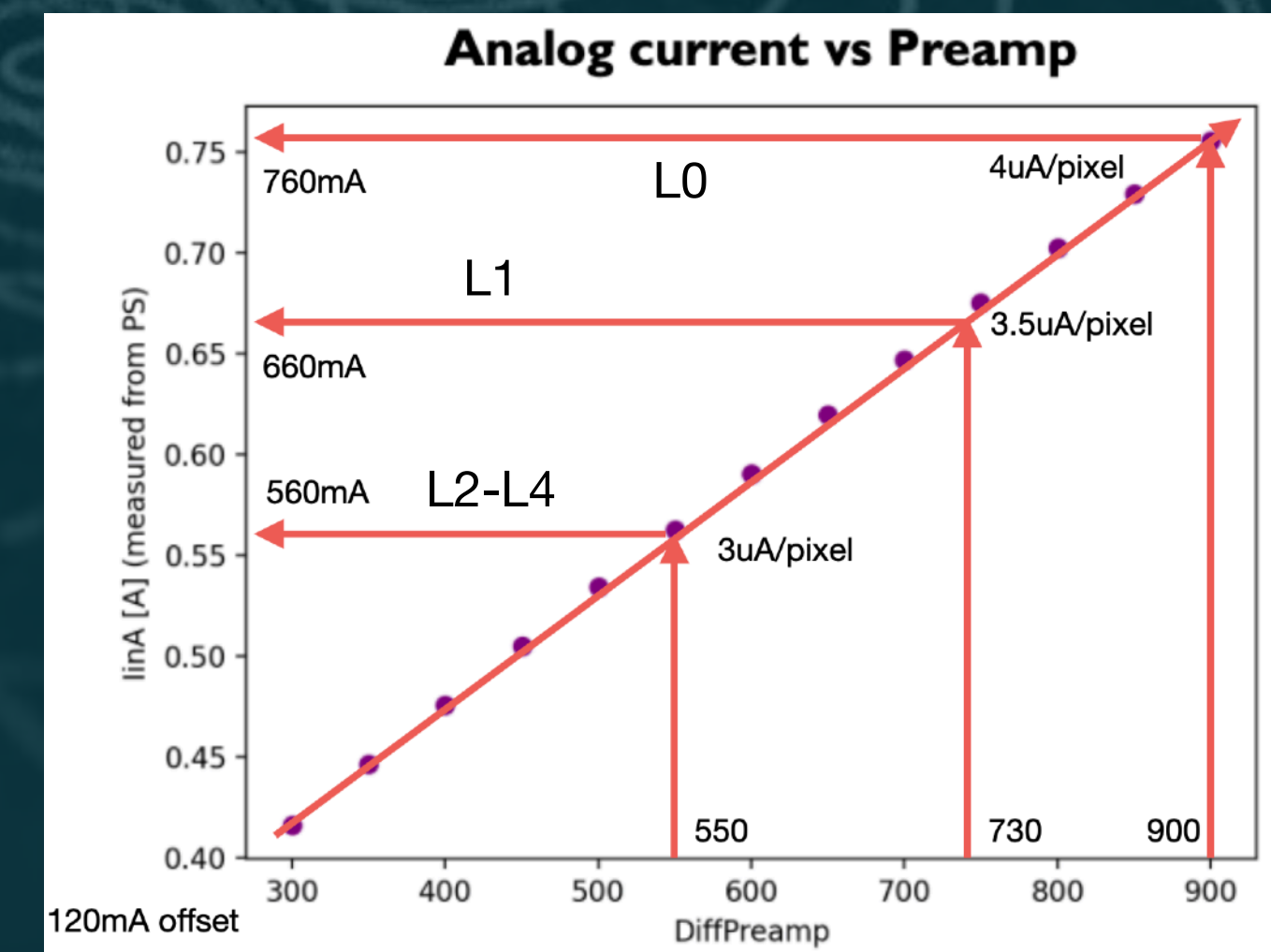
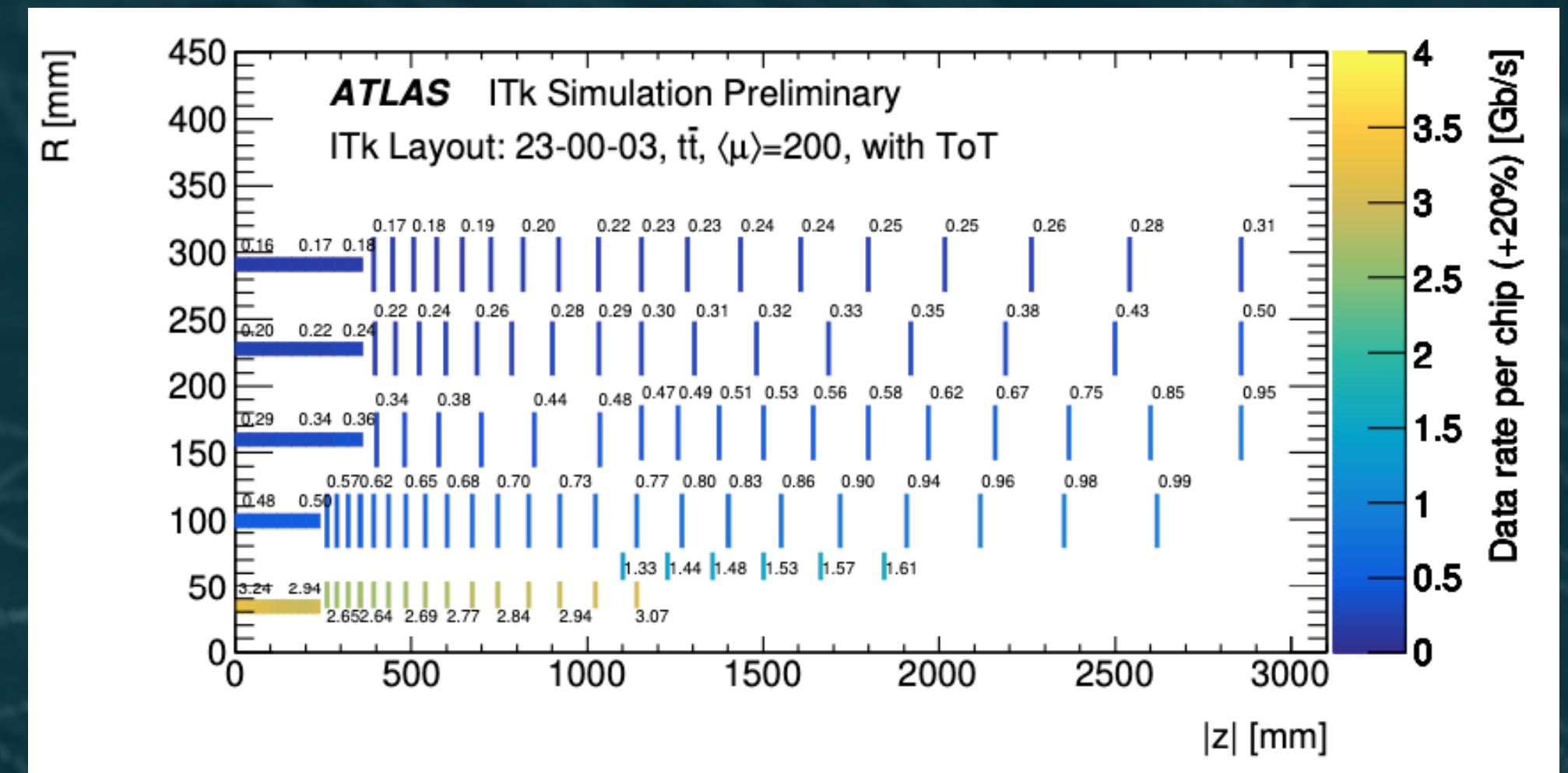


\*not apples to apples comparison



# Data Bandwidth

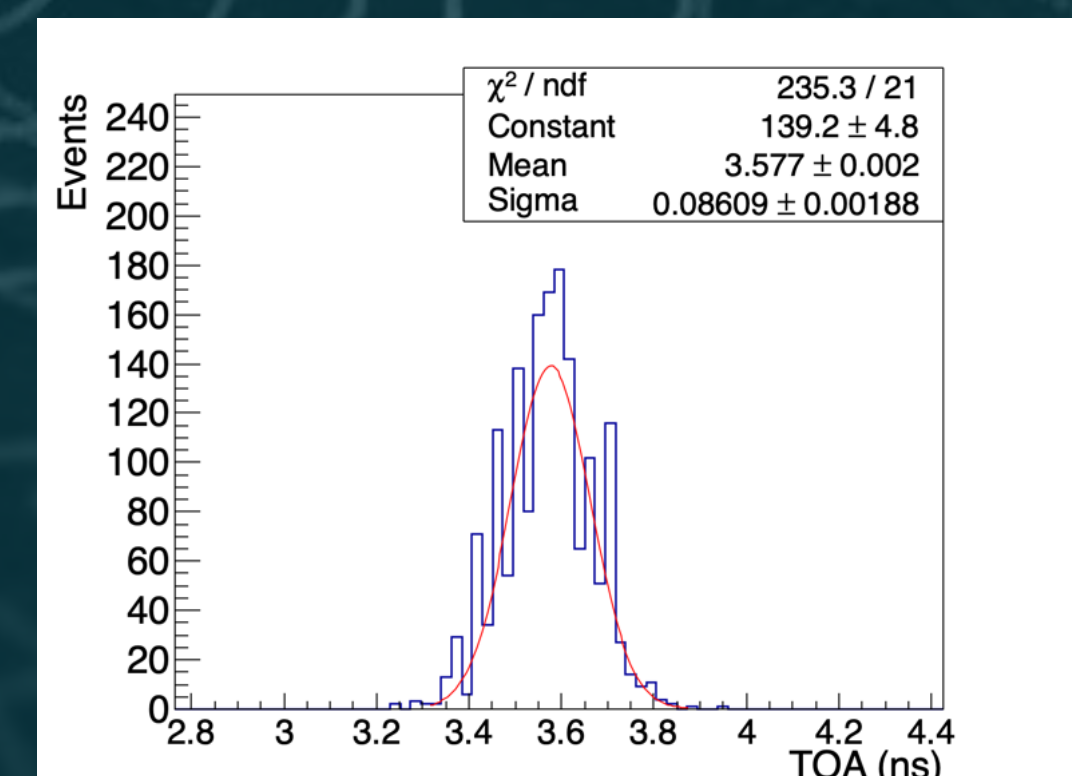
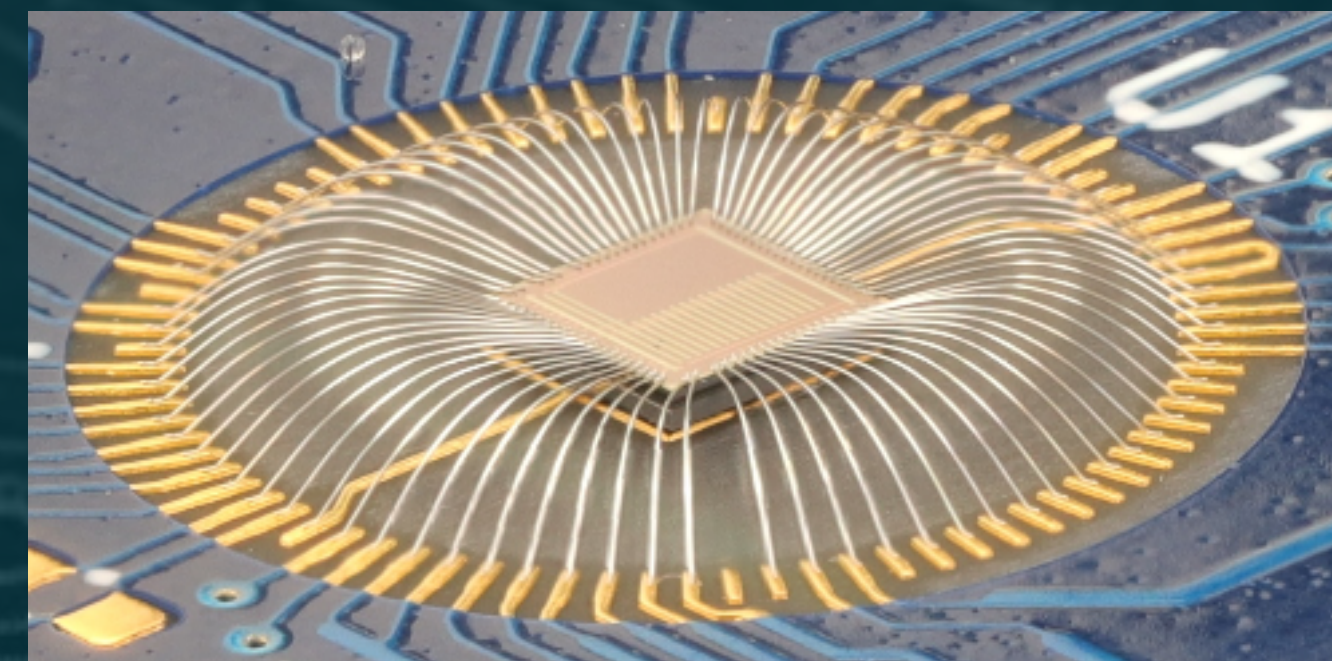
- Vertex detector has to **cover large spectrum in multiplicity**, at HL-LHC already and even more pronounced at MuC
- MuD **Layer 1/2 hit multiplicity ratio factor ~100**
- Innermost layers covers small area and space points are important for vertexing -> worth to splurge on mass wise, can accommodate services for a high data rate, cooling for higher power
- Outer layers cover larger and larger area, sees much lower hit rates and less radiation -> want it to be as light-weight as possible
- Considering the cost and effort to develop pixel readout chip technology, **not practical too have multiple flavors. Scaling needs to be build in from the start!**
- Need to foresee **power scaling** both in analog and digital
- Mass dominated by data services: **on-chip data link aggregation** to efficiently utilize every cable/link





# 4D Pixel Demonstrator

- 4D Pixel detectors are new to us, lots of exciting single component R&D underway already (sensors, ASIC, DAQ, ...)
- There is a possibility to deploy a first 4D Pixel detector as part of ATLAS/CMS “Phase 3” upgrade in LS4/5 (2033/2039)
- A **demonstrator program** that has a defined goal can help drive R&D and coalesce national developments
- See Timespot project by INFN
- Could deliver a **small scale system 4D tracking system** that could be deployed at testbeam facilities and used for future R&D
- Unlikely to have central funding available, need to **communicate and decide on important interfaces between components**, components can be developed in isolation but later need to fit into the system
- Ariel, Simone, and me are **organizing a US 4D Pixel detector workshop** to kick this off for Fall 2024, finalizing details right now, should announce soon
- Please get in touch with us in person while we are all at FNAL if you are interested





# FCC Parallels?

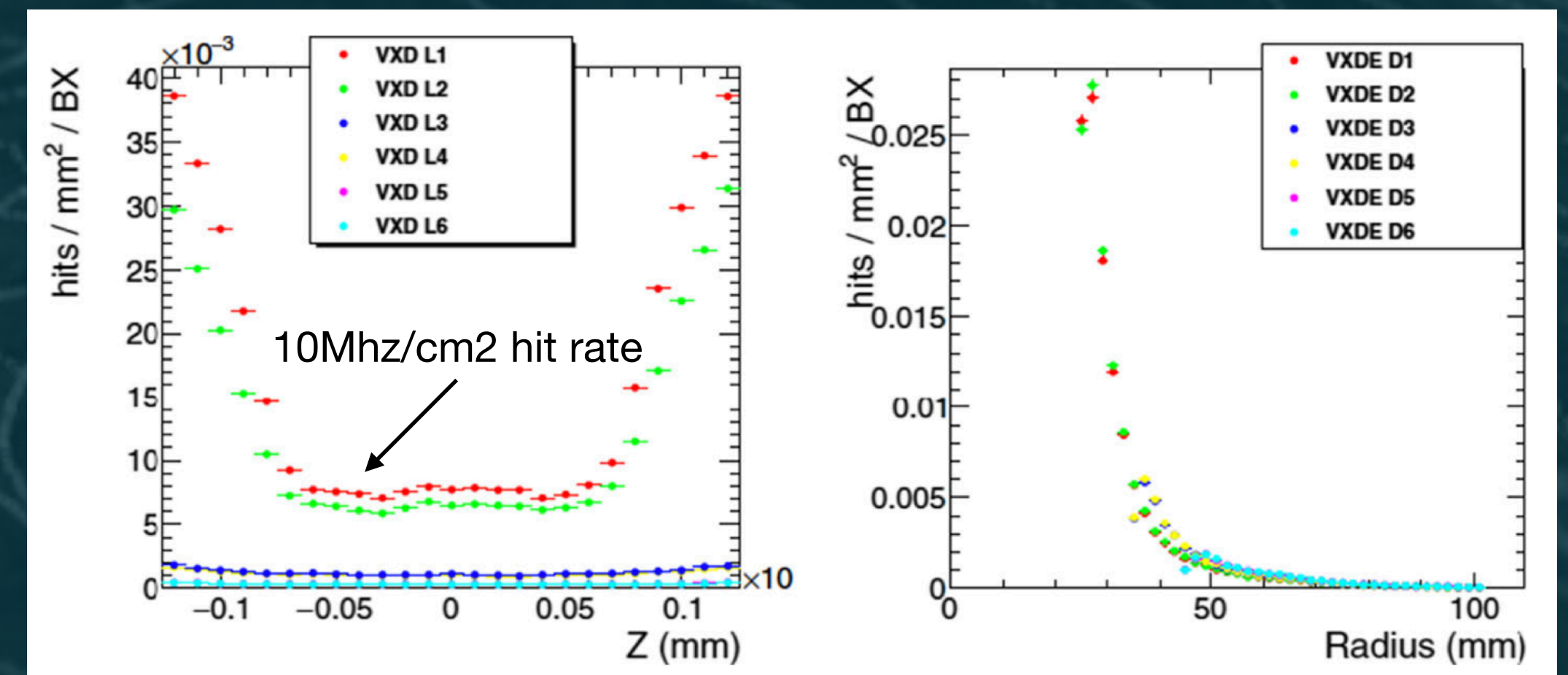


- While FCC-ee environment very different from MuC, should actively **engage in thinking which aspects are transferable**
- Precision timing is a new dimension we are exploring in the detector world, should not exclude that it could lead to **improvements that can also be applied to more classic 3D detectors**

- Sensor technology
- On-chip data processing
- Precision measurement of signal shape
- Local vs. global signaling
- Low power electronics
- ...

- FCC-ee detector will likely have **at least one timing layer** for particle identification through time-of-flight
- MuC environment will **push 4D tracker technology to its extreme**, having explored that domain will help with tracking detectors for any application!

FCC-ee VXD Hit rates





# Conclusion

Hope to have given  
you some food for thought!

- Pixel detector front-end chip design faces many challenges in the MuC environment
- These challenges **require more than just improving on traditional designs**, need to think outside of the box!
- Could lead to paradigm changing developments that could be applied at more than just the MuC
- **Instrumentation and detector simulation should not live in isolation**, let's start the feedback cycle early to not get locked into preconceived notions
- Can we achieve full co-design?
- Let's start a **4D Pixel detector demonstrator project** and coalesce national R&D efforts

