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U.S. DEPARTMENT OF ENERGY

BNL, IO- ASIC Activity

G.W. Deptuch

Contributions: S. Mandal, P. Mukim, N. St. John, D. Górni, A. Iqbal, G. Pinaroli, P. Maj, J. de Melo, S. Hassan, P. Purohit, S. Durando

RDC meeting: 05/08/2024

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Introduction

Expertise

CAD/EDA Tools

Mode of Operation

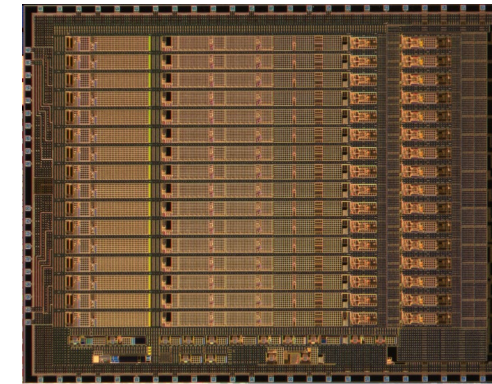
Collaborations

Areas of Activities

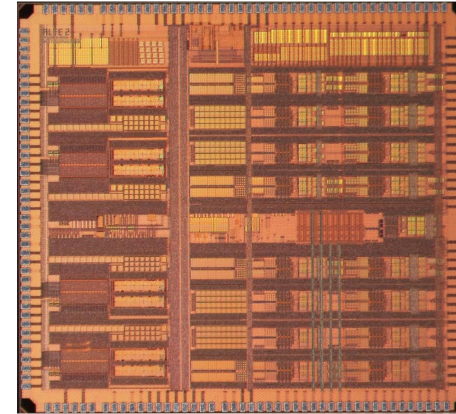
Expertise

Expertise in low-noise, low power, large mixed-signal designs

- 11 full time ASIC designers + test leader
  (8 PhDs + 2 in PhD program, including industrial background)
- profiles satisfying needs of multiple programs (incl. device physics)
- open for hosting guest/visitors and grad/post-grad students
- hand-in-hand with in-house TDAQ, PCB, sensors and other groups

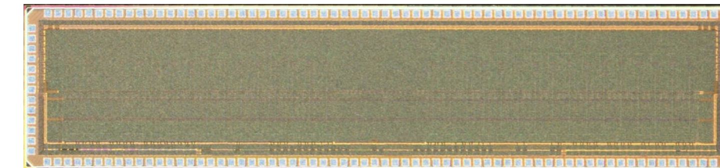


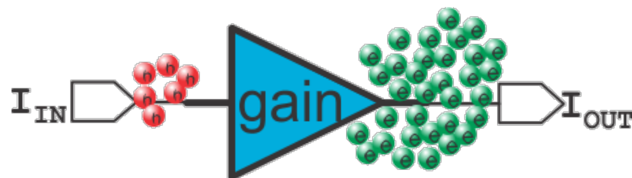
LArASIC_P4 180 nm



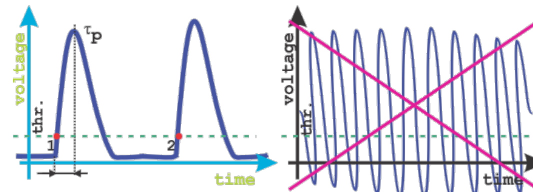
ALFE2 130 nm

AVG_DEV 65 nm

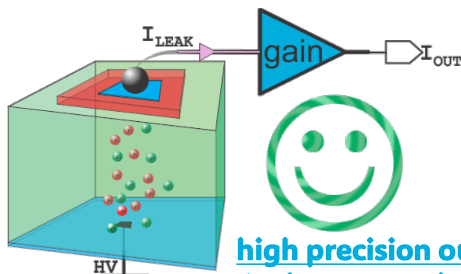




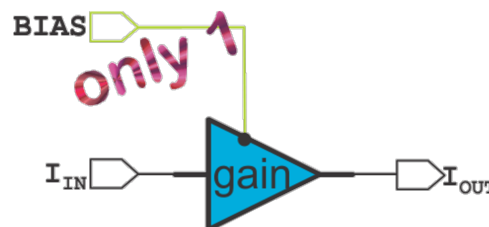
amplifies linearly small input charge (⇨ Low noise)



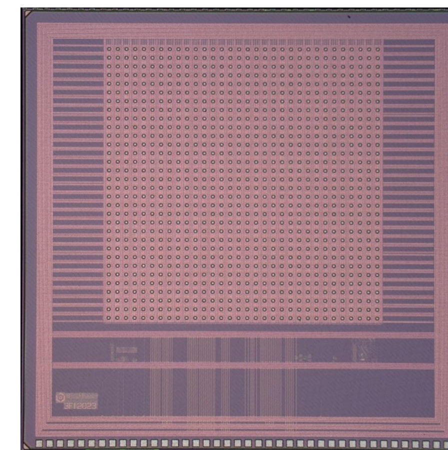
high precision, stable output
(⇨ better resolution)



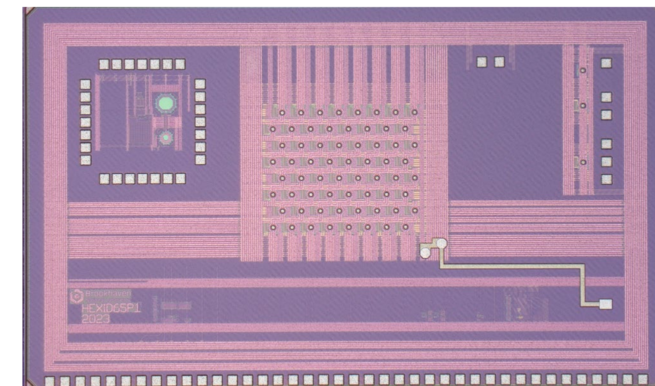
high precision output
(⇨ better resolution)



simple bias (⇨ Low power)



3FI65P1 65 nm

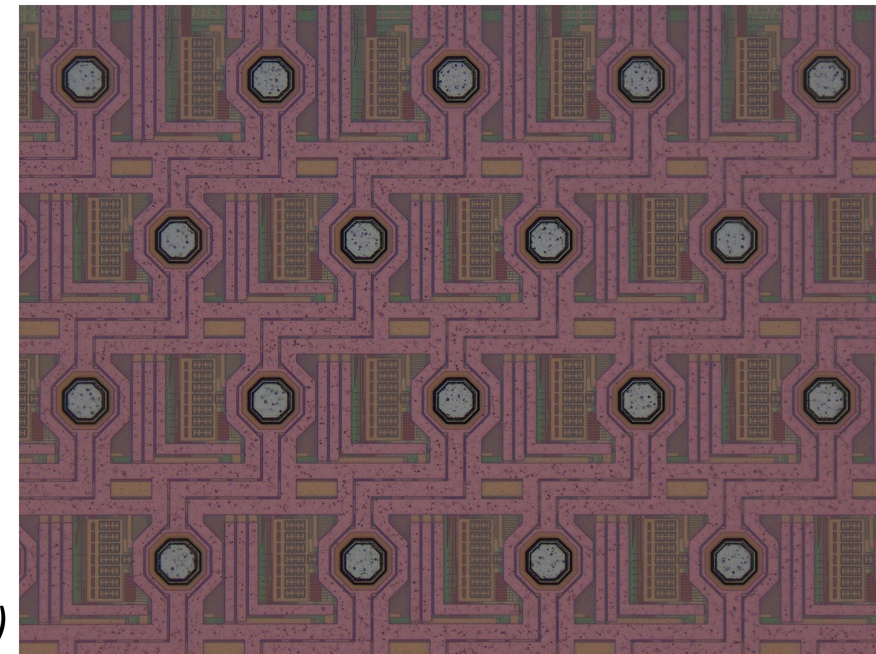


HEXIDP1 65 nm

CAD/EDA Tools

Design tools and methodologies

- industry-standard tools from Cadence, Siemens (Mentor), etc.
  (analog on top or digital on top flows)
  analog: *full custom flow (VSE, VLE, ADE/Spectre, AMS, PVS, XACT3D-PEX)*
  digital RTL2GDS: *functional simulation, logic synthesis, automated P&R, parasitics extraction, static timing analysis, HLS (XCELIUM/GENUS/INNOVUS/QUANTUS QRC/TEMPUS, Catapult/HLS Matlab)*
  library characterization: *custom standard cell libraries for designs for extreme environments: cryogenics, radiation, design for manufacturability and yield*
  verification: *IR drop (VOLTUS/ VOLTUS-fi), functional (SV), physical (PVS, Calibre DRC/ERC/LVS)*
  device modeling: *TCAD, FEM solvers, transistor model parameter extraction (Silvaco ATHENA-ATLAS-VICTORY, Maxwell, UTMOTS4)*
- foundry PDK's: *TSMC CMOS (from 180 nm to 28 nm), GF CMOS and BiCMOS SiGe 130nm, 90nm, 45 SPCLO + specialized processes: monolithic CIS on HR TPSCo, sensors co-design, XFAB High-Voltage bulk and PDSOI (180 nm and 110 nm) etc.*
- access to foundries via: MOSIS, CERN-IMEC Foundry Services, DMEA/TAPO, IMEC and directly
- beyond Silicon: SiC process (ultra rad-hard)



pixel in 65 nm (G. Pinaroli)

Mode of Operation / Collaborations

Fast-developing scales and functionalities of modern μelectronics:

- using established processes (130 nm, 65 nm) for projects ASIC in instruments
- Special place: Monolithic Active Pixel Sensor (dedicated processes)
- reaching for emerging technologies for R&D (28 nm, specialized processes)

Collaborations:

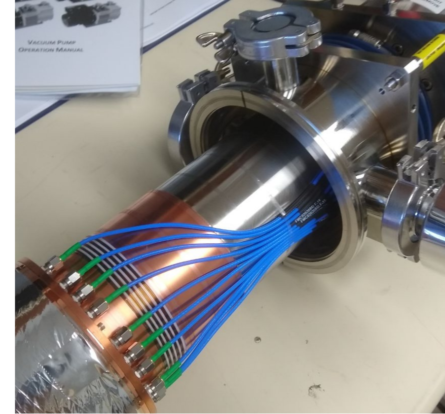
- Universities: SMU, UMich, UPenn, MIT, Georgia Tech, Columbia, USF, UIUC, KU
- National Laboratories: FNAL, LBNL, ORNL, NRL
- Industry: several industrial partners + more collaborators
- International: CERN, RAL, OMEGA, KIT Karlsruhe, AGH Krakow, UBonn

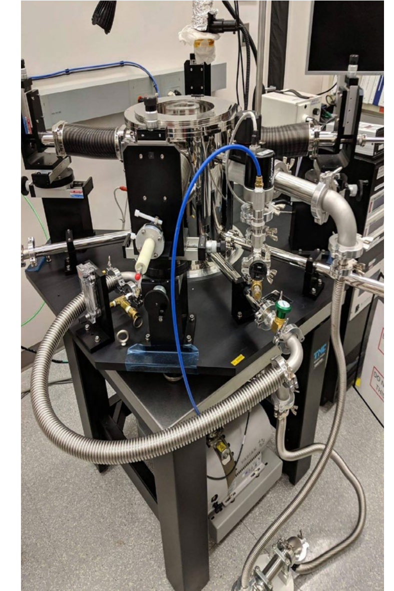
Areas of Activities 1

Areas of Activities and Research Interests:

Low-noise and low-power

- custom analog front-end matched to specific sensors
- front-end circuits optimized for amplitude & time-resolution
- data, event driven or zero-suppressed readout methodologies
- advanced processing AI/ML, highly-digital front-end





probe station at CFN / cryostat at IO operating down to 4K

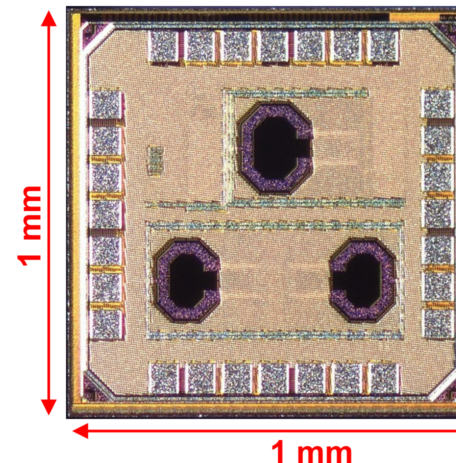
Cryogenic operation

- readouts for Noble liquid TPCs – R&D on RO electronics for DUNE's VD TPC, nEXO (lAr, lXe)
- long lifetime reliability
- development & maintenance of spice-type model parameters and characterization (.lib) of standard cell libraries
- RF electronics for quantum sensors (4K, ≤1K)

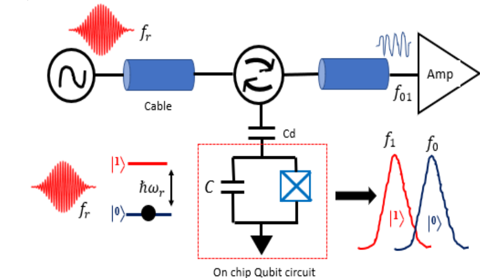
Photonics and interfaces

- Power over Fiber (PoF)
- data transmission (energy efficiency)
- photonic processors, including neuromorphic computing

1 mm



1 mm



4K CryoCMOS 5.12 GHz VCO + QVCO for PLL, CML divider and interfaces QRFIC_P1

V.Manthena et al, 2020 11th IEEE Annual (UEMCON), 2020, pp. 0570-0576

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Areas of Activities 2

Radiation-Hardness

- immunity to TID, NIEL and SEE effects:
  - process (inherent to process)
  - design (achieved through proper design techniques)
- methodologies for SEE immunity
- exploration of next-gen for HEP CMOS and BiCMOS processes
- Beyond Si (SiC for sensors and circuits)

Hybrid-pixel detectors

- spectroscopic & imaging detectors for X-rays (BES, BER, NASA)

Monolithic Active Pixel Sensors

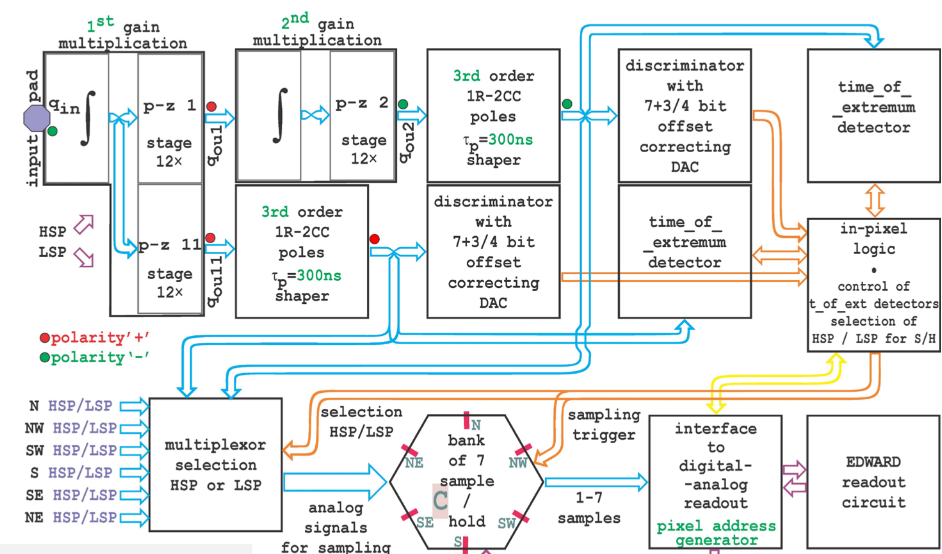
- ePIC SVT and upgrades for the EIC (NP) and FCC

Lightweight detectors, 3D-IC and HDI

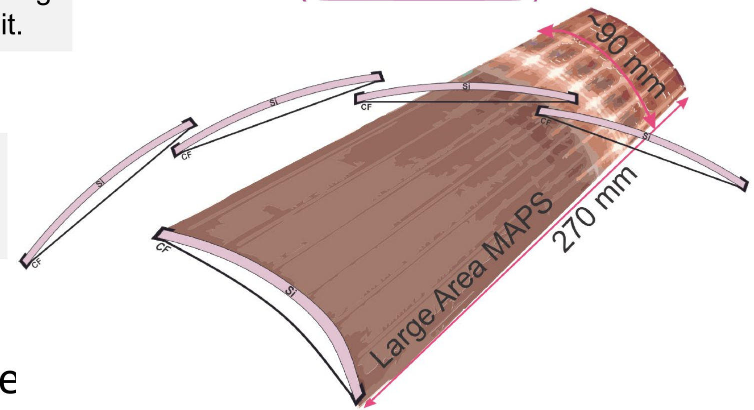
- edgeless and gapless, highly granular pixel detectors with extended functionalitie
- large area sensors for the EIC vertex and tracking layers
- event-driven and neuromorphic suitable arrayed readouts

Embedded AI and neuromorphic processing

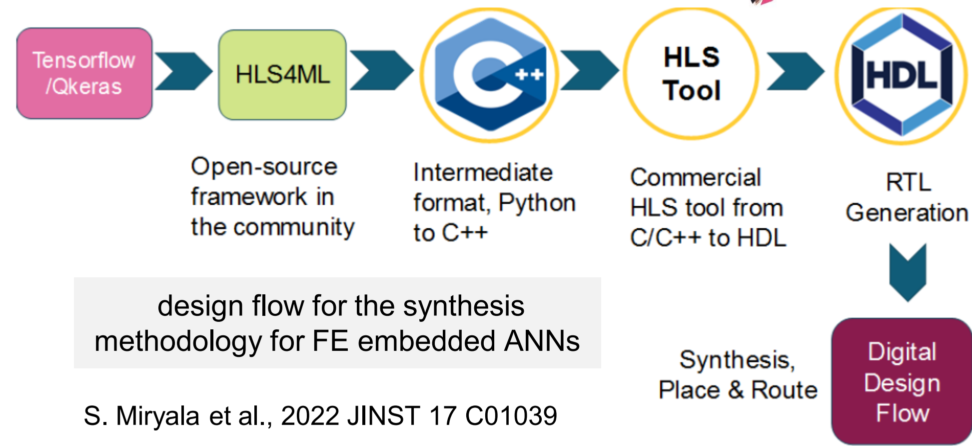
- co-design methodologies for FE ASICs
- VMM processing with new electron devices: memristors



block diagram of the analog in-pixel front-end circuit.



curved monolithic sensor stave made of stitched MAPS.



design flow for the synthesis methodology for FE embedded ANNs

S. Miryala et al., 2022 JINST 17 C01039

Examples of Projects

Cryogenic Low-Noise Front-End (DUNE, and beyond)

Frameless, Configurable Readouts

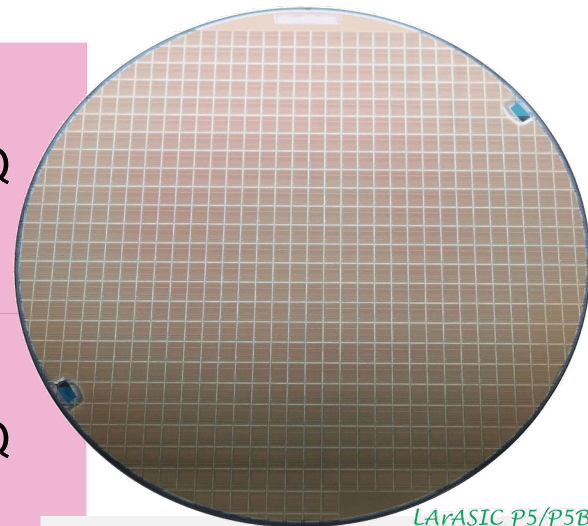
Advanced Pixel Detectors

Monolithic Active Pixel Sensors

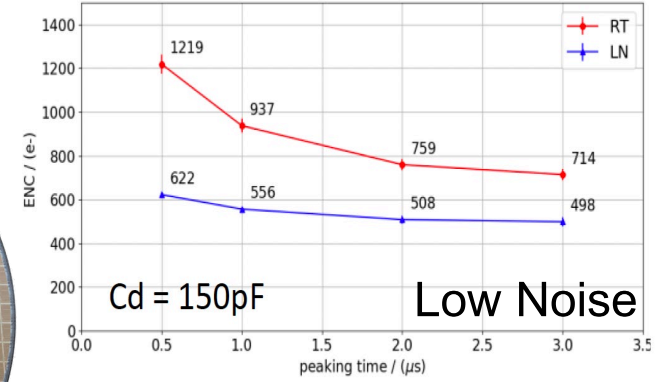
Highly Digital and ML-Assisted Front-Ends

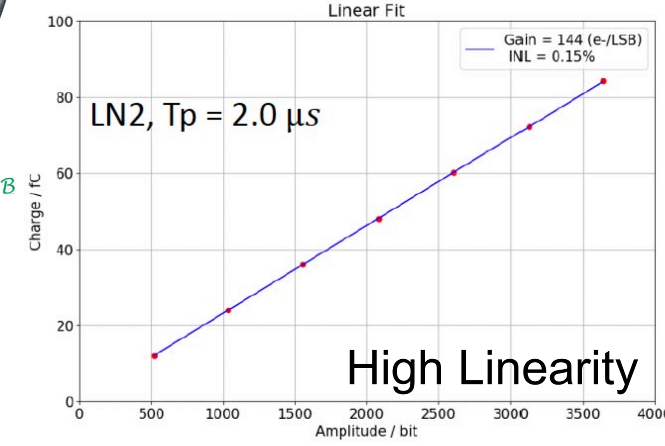
Cryogenic Front-Ends 1

MicroBooNE	LArASIC	COTS ADC	FPGA	DIGITAL LINKS	DAQ
proto-DUNE	BNL LArASIC	LBL/FNAL/BNL COLD_ADC	FPGA	DIGITAL LINKS	DAQ
SBND	LArASIC	COTS ADC	FPGA	DIGITAL LINKS	DAQ
DUNE	LArASIC	COLD_ADC	FNAL/BNL COLD DATA	DIGITAL LINKS	DAQ
	CMOS 180	CMOS 65	CMOS 65	88K	300K

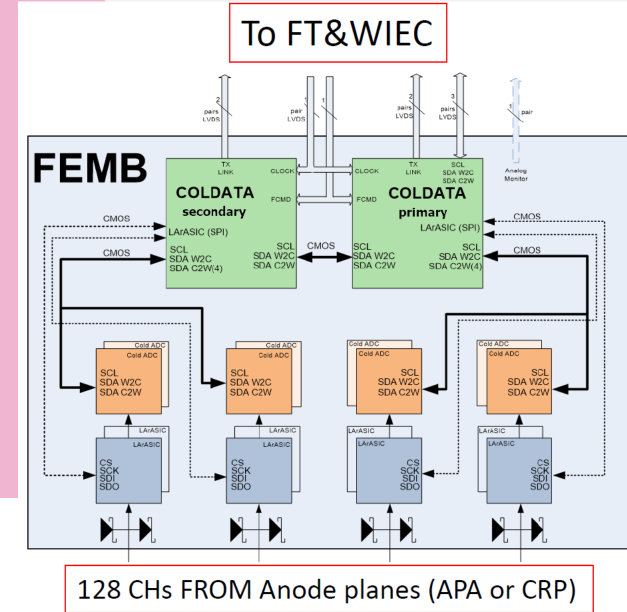


8" wafer with 610 LArASICs P5 and P5A(B) w. increased ESD protection
practically 100% yield



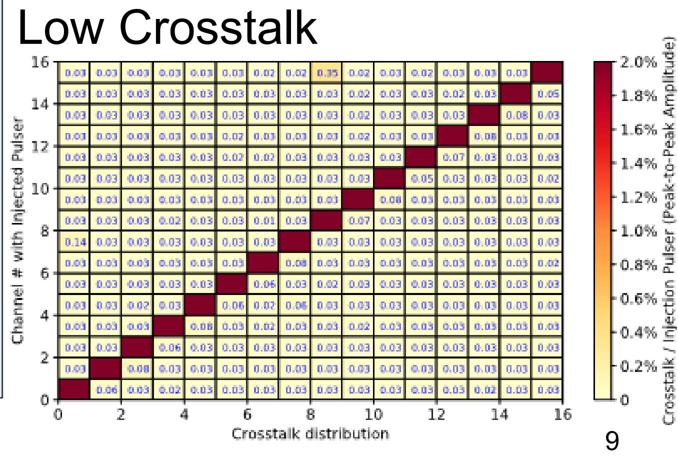


To FT&WIEC



128 CHs FROM Anode planes (APA or CRP)

Low Crosstalk



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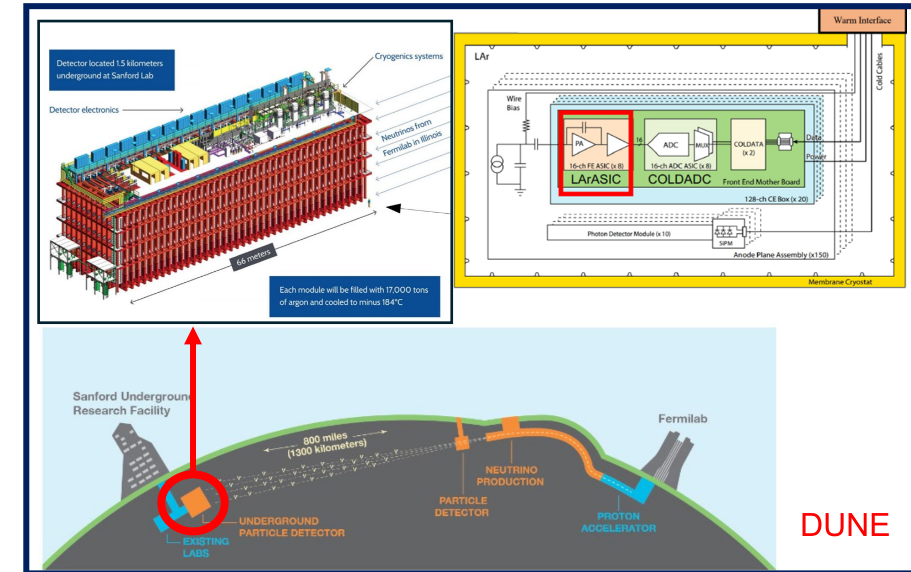
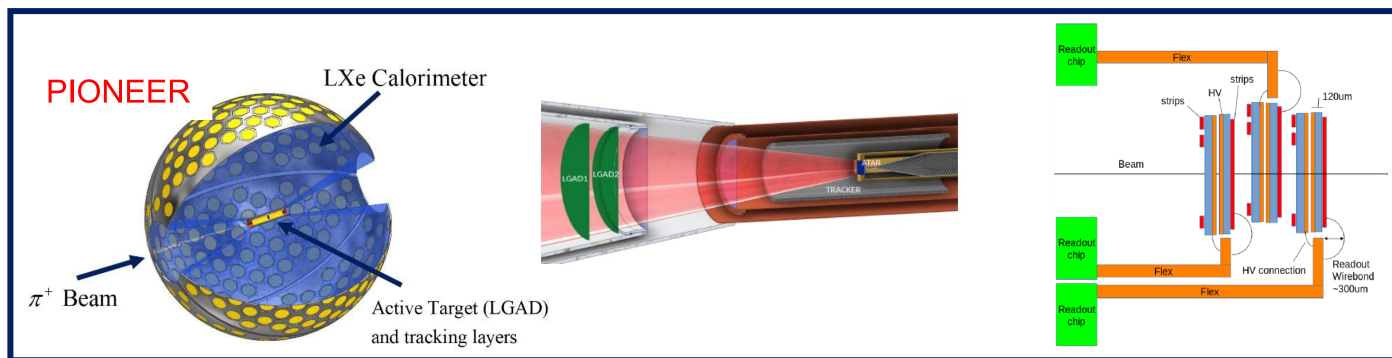
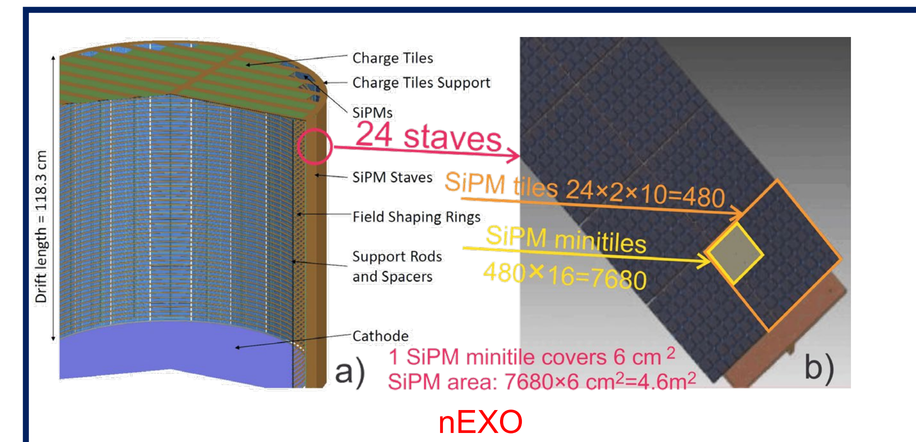
About a decade of development !

Cryogenic New Front-Ends 2

Experiment	Temperature	Detector Capacitance	Shaping Time	Noise	Dynamic Range
DUNE FD 3/4 charge readout	89 K – 300 K	150 pF – 200 pF	250 ns – 2 μs	500 e^- at 87 K	10 bits
nEXO light readout	160 K – 300 K	5 nF	1 μs	0.1 pe^- at 160 K	10 bits
FCC-ee	TBD	TBD	< 250 ns	TBD	> 10 bits
PIONEER	160 K – 300 K	20 pF	20 ns	570 e^- at 160 K	10 bits







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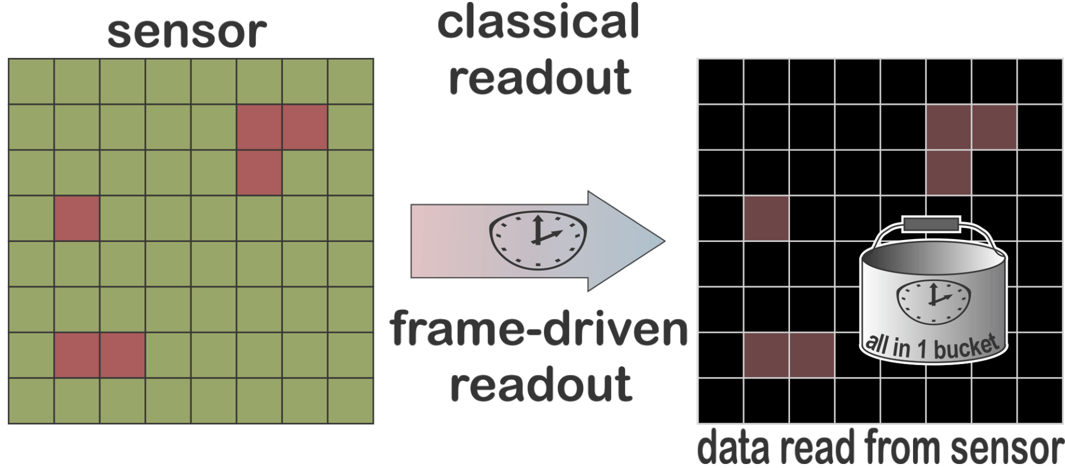
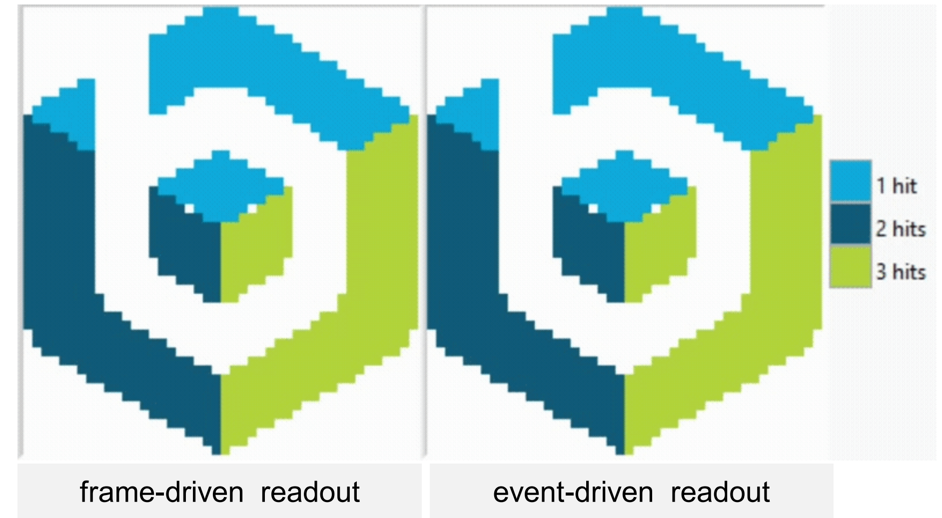
CHARMS250 and CHARMS10 are new developments

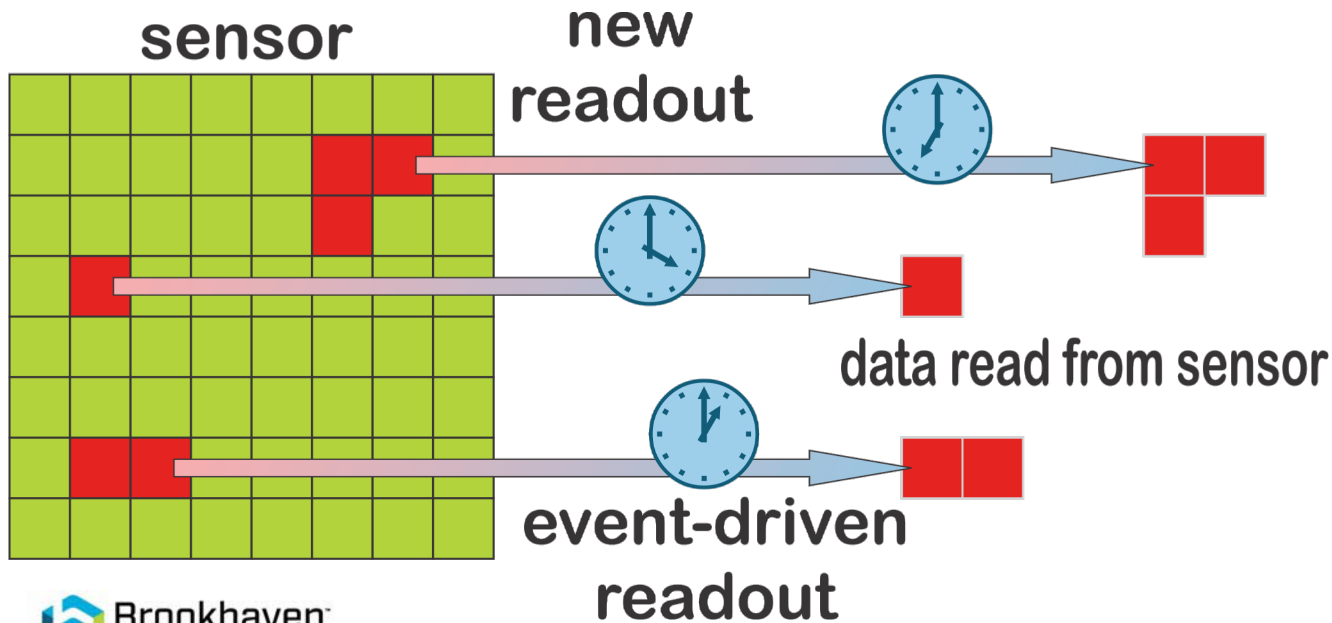
P. Mukim, et al, "Cryogenic Front-End ASICs for Low-Noise Readout of Charge Signals", ready for submission for IEEE TCAS-I review

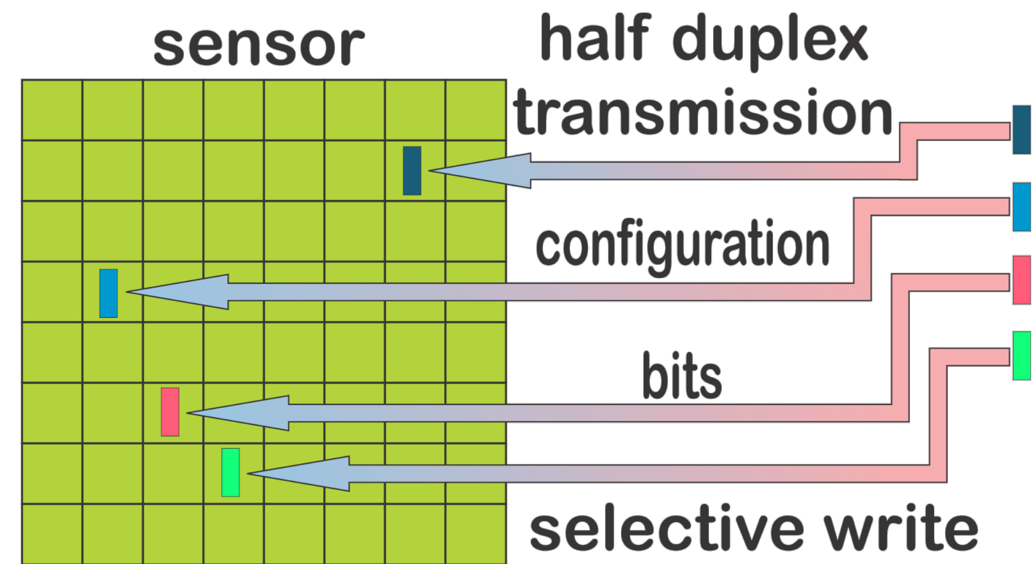
Frameless, Configurable Readout

even if sparsified good timing is disallowed as TDC/ch is required









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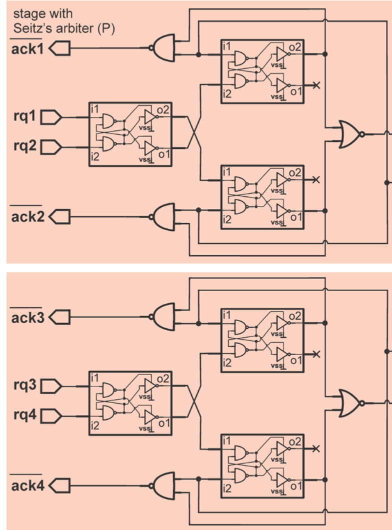
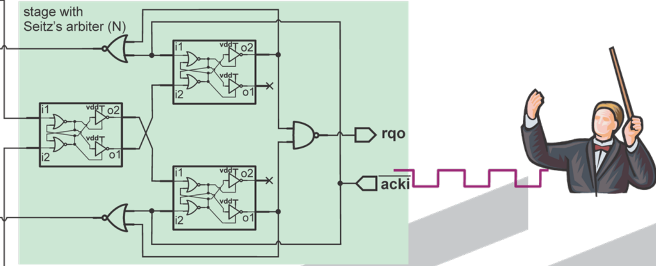
D. Górni, et al., 2024 JINST 19 C04035

Advanced Pixel Detectors



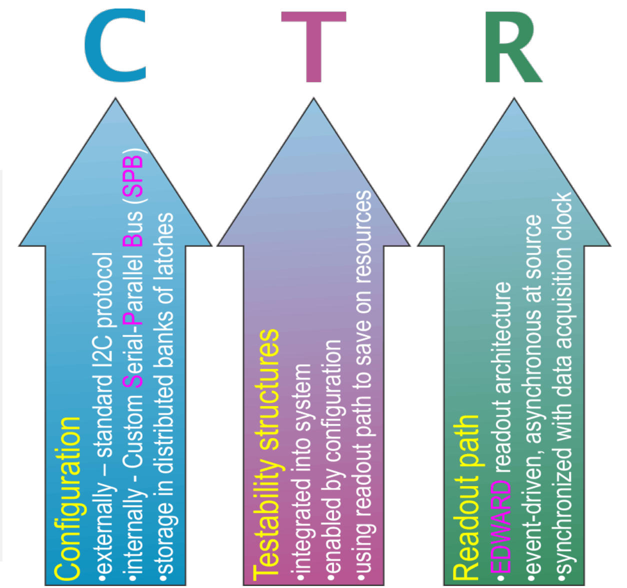
NON-GREEDY ARBITRATION

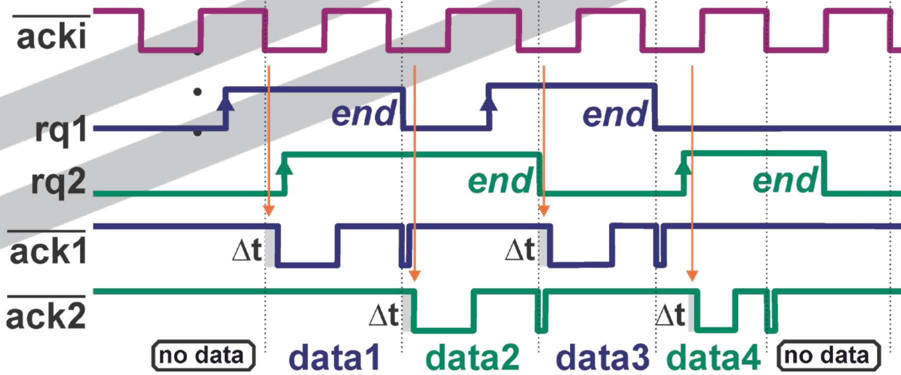
fastest, selective, dead-timeless readout implemented in **BNL's pixel readout ASICs**



CoDesigned **CTR PLATFORM:**

- complete functionality in RTL code;
- parametrized and scalable;
- suitable for "virtual painting" of multichannel readout ASICs;
- RTL with implementation constraints shareable with interested parties;



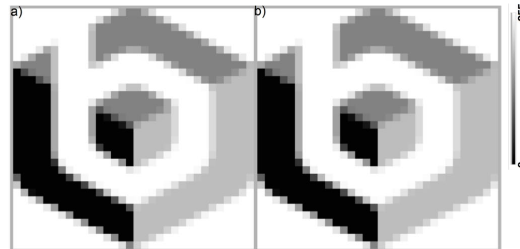


handling of requests and responding with acknowledges

Features:

- **Event-driven** ➡ hits extracted from matrix of pixels on the fly, without snapshotting in readout frames;
- Energy-efficient ⬅ no clock, no strobes distributed to other but being read out pixel;
- Silicon-proven and patent pending;

D. Górni, WO/2022/221068: Event-Driven Readout System with non-priority arbitration for multichannel data sources

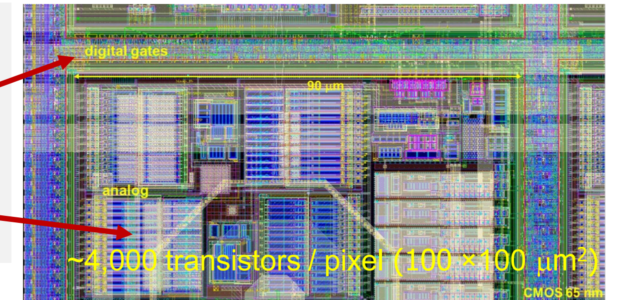


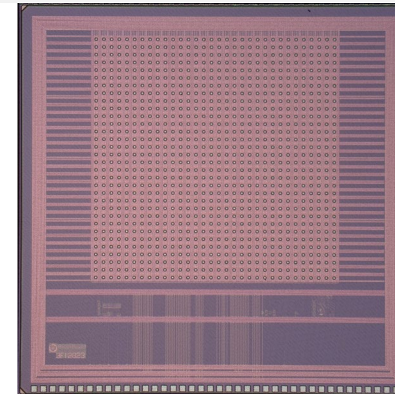
number of readouts as intensity maps:	as programmed using I2C-SPB interface	as actually read out from all pixels

Square and hexagonal pixel for BES, BER, NASA, NP

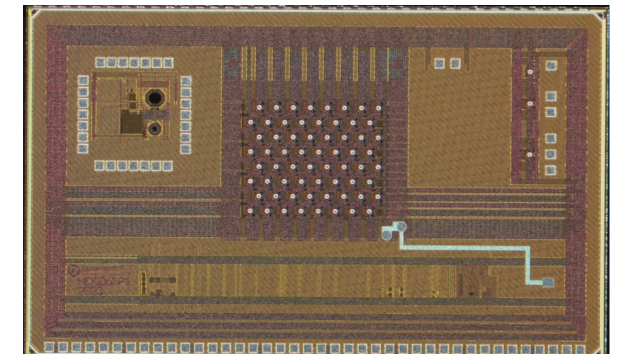
Design:

- new front-end;
- digital skeleton of CTR;
- analog embedded in sea of gates;
- handling of charge sharing;



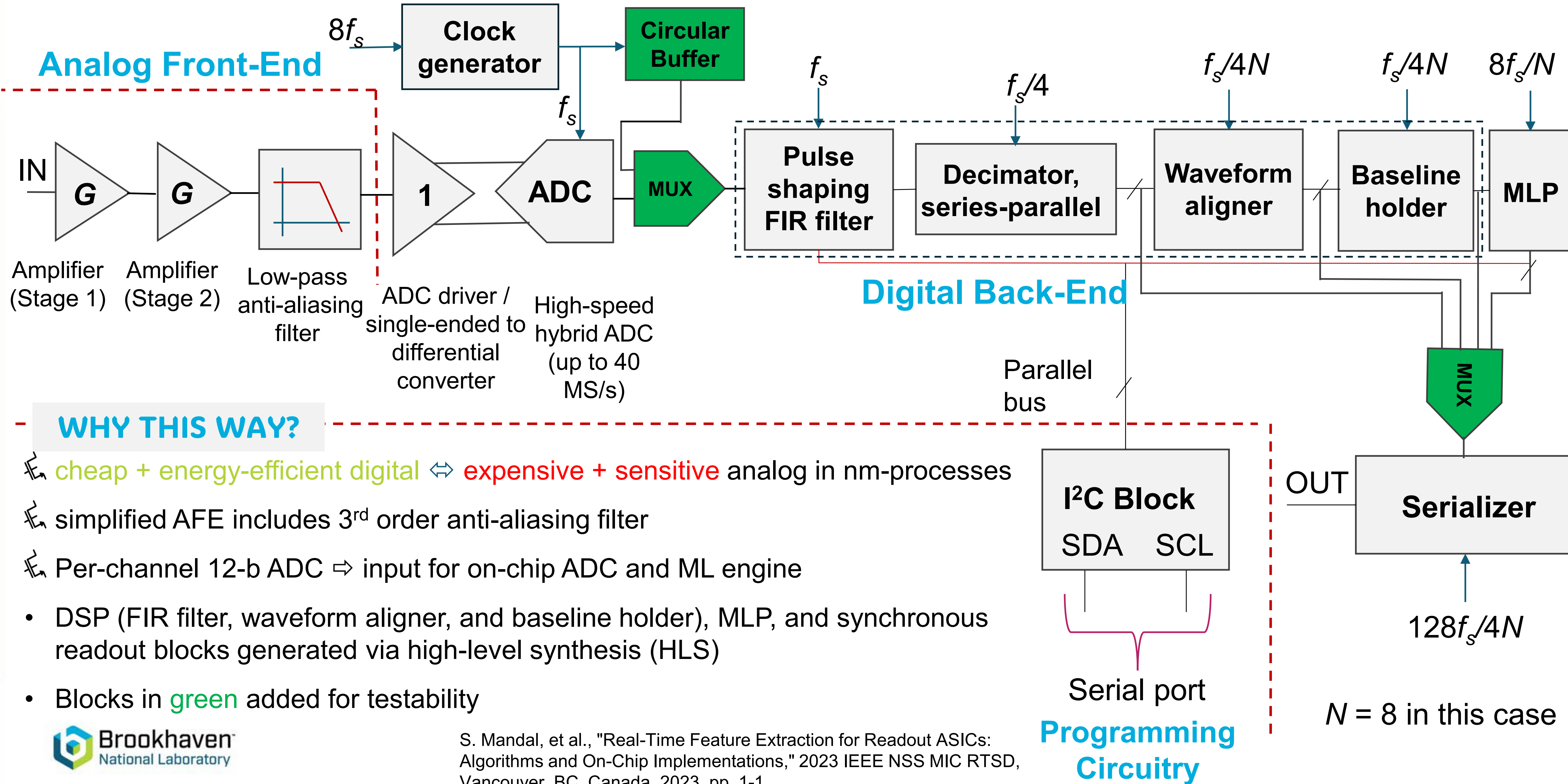


3FI: Soft X-ray Spectroscopy



HEXID: Hard X-ray Space Telescope

Highly-Digital and ML-Assisted FE 1



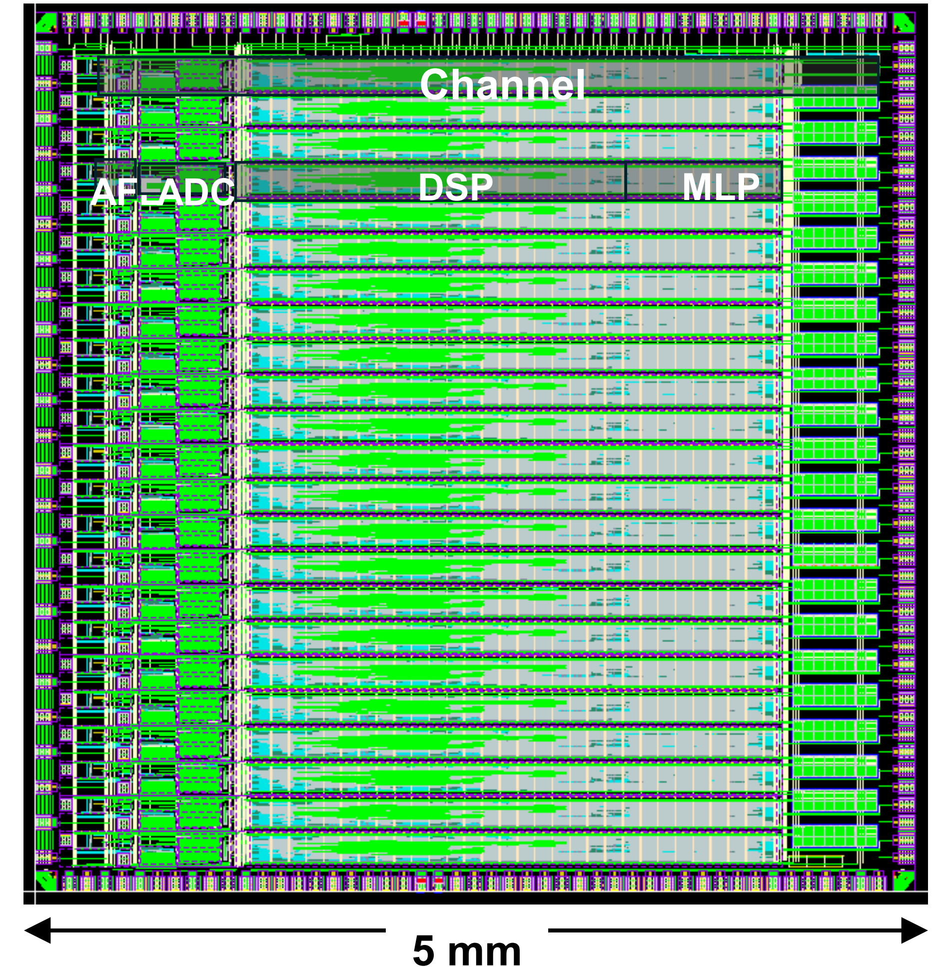
Highly-Digital and ML-Assisted FE 2

Demonstration of feasibility

- channel height: 200 μm (including ADC)
- chip area: 5×5 mm^2
- includes CML receiver for high-frequency input clock (8×f_s = 160 MHz).
- channel 23 is instrumented (additional pad outputs).
- expected DSP power consumption ~10 mW/channel (clock = f_s = 20 MHz).
- design status: Currently being fabricated

Advantages for low-noise operation

- nonstationary filters (disabled during pulses)
- tracking of pedestals / ch. (virtually infinite length, unrestricted windowing)
- inter-channel correlations (common mode)



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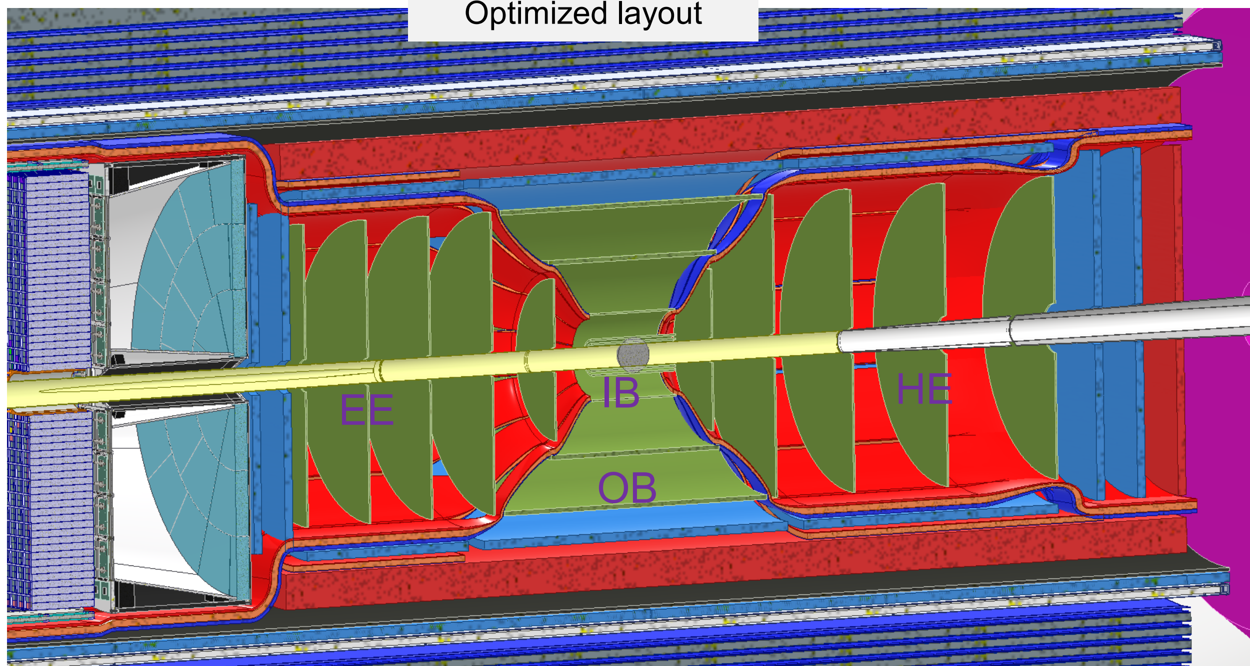
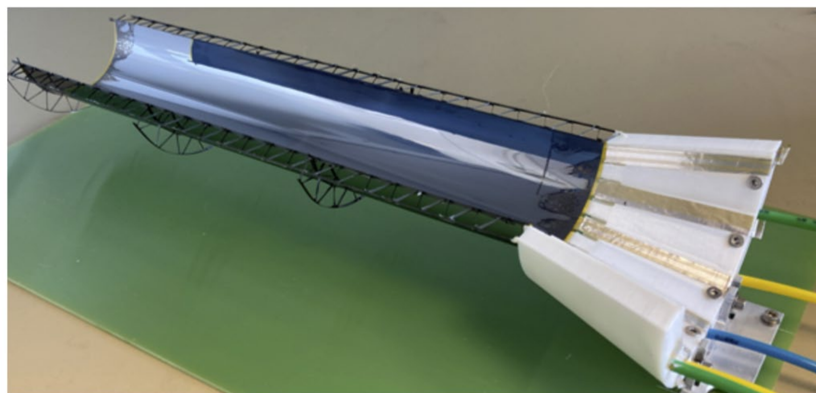
non-achievable in pure analog processing !

MAPS ePIC SVT 1



- cables & services for μvertex & OuterBarrel layers + first 2 disks exite on a cone along 45° line and cables run in-front of MM
- 3 equal sized MM modules
- MM cables can run on front or back face of MM
- fewer sharp bends

MAPS Barrel + Disks
MPGD Barrels + Disks
AC-LGAD based ToF



G. Feofilov et al.,
ITS3 WP4 10 October 2023.

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ePIC SVT detector layout configuration
(in total almost 100B pixels, on ~ 10 m^2 of Si)

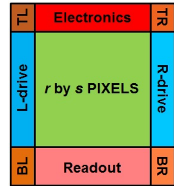
Silicon Barrel Layers				
		Radius [mm] (min, max)	Length [mm]	X/X0 [%]
VX 1 (L0)	IB	36	270	0.05
VX2 (L1)	IB	48	270	0.05
VX3 (L2)	IB	120	270	0.05
Sagitta1 (L3)	OB	270	540	0.25
Sagitta2 (L4)	OB	420	840	0.55
Silicon Hadron Endcap (wheels)				
		Distance [cm]	Radius [mm] (min, max)	X/X0 [%]
HD1	H-End Cap Disks	25	(36.76, 230)	0.24
HD2	H-End Cap Disks	45	(36.76, 430)	0.24
HD3	H-End Cap Disks	70	(38.42, 430)	0.24
HD4	H-End Cap Disks	100	(54.43, 430)	0.24
HD5	H-End Cap Disks	135	(70.14, 430)	0.24
Silicon Electron Endcap (wheels)				
ED1	E-End Cap Disks	-25	(36.76, 230)	0.24
ED2	E-End Cap Disks	-45	(36.76, 430)	0.24
ED3	E-End Cap Disks	-65	(36.76, 430)	0.24
ED4	E-End Cap Disks	-90	(40.0614, 430)	0.24
ED5	E-End Cap Disks	-115	(46.3529, 430)	0.24

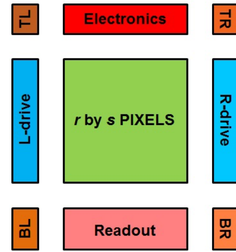
Technology of choice: MAPS in TPSCo 65 nm process, following CERN's ALICE ITS3 upgrade development of bent silicon

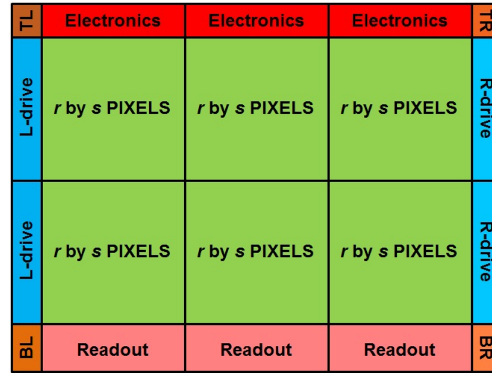
Disclaimer:
some numbers, mainly X/X0, are evolving due to stave approach and cooling.

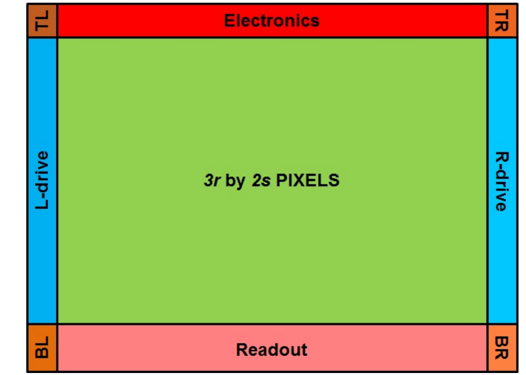
MAPS ePIC SVT 2

MAPS sensors are large (single ASIC) …

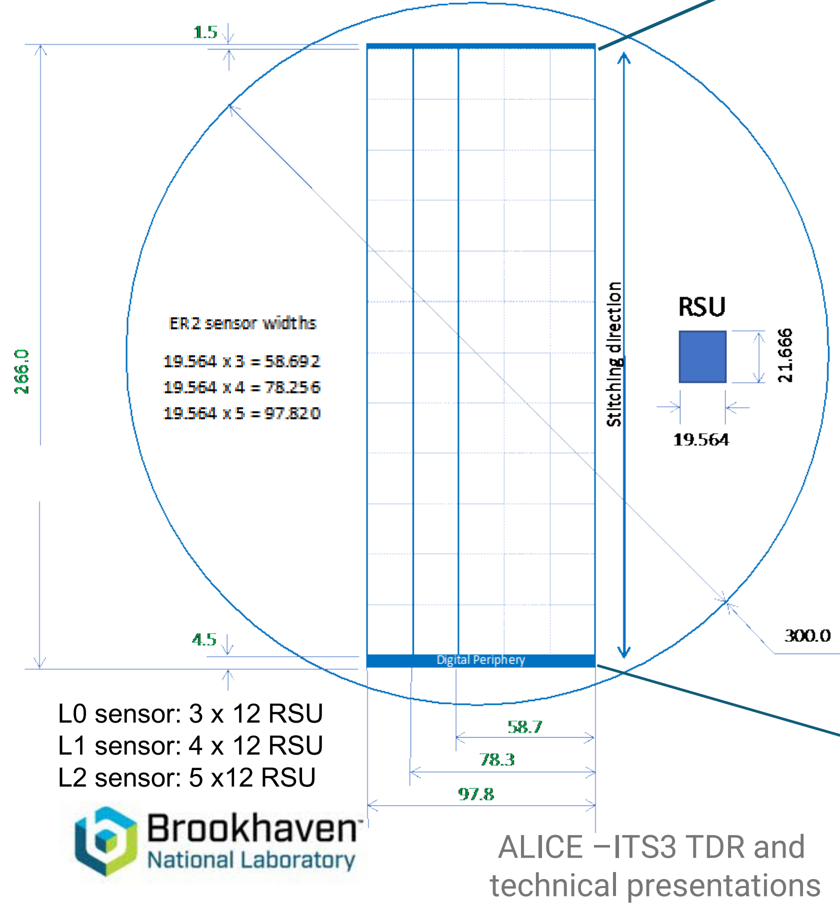




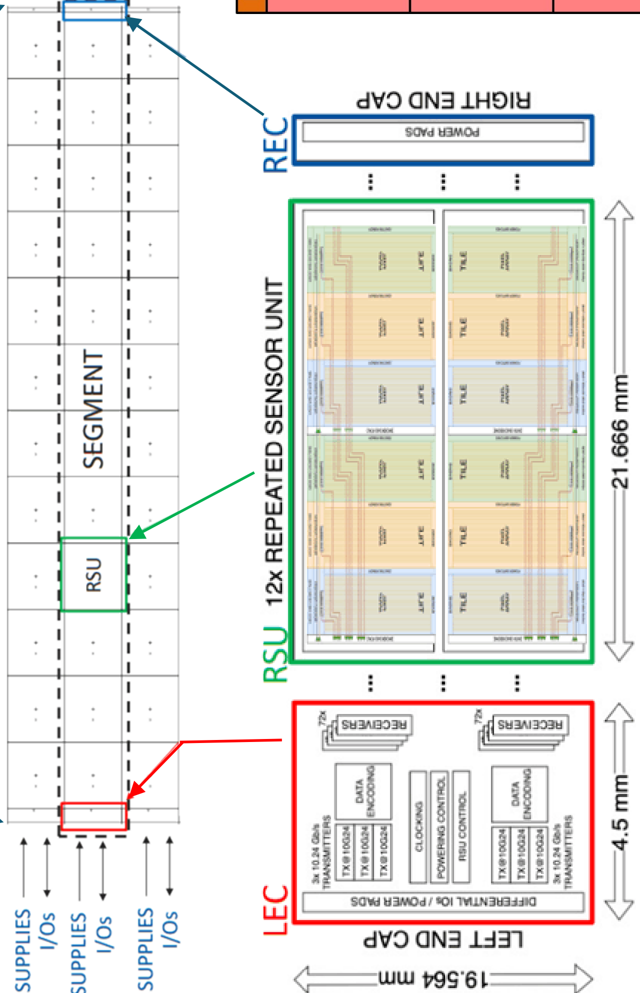




…thanks to reticle stitching

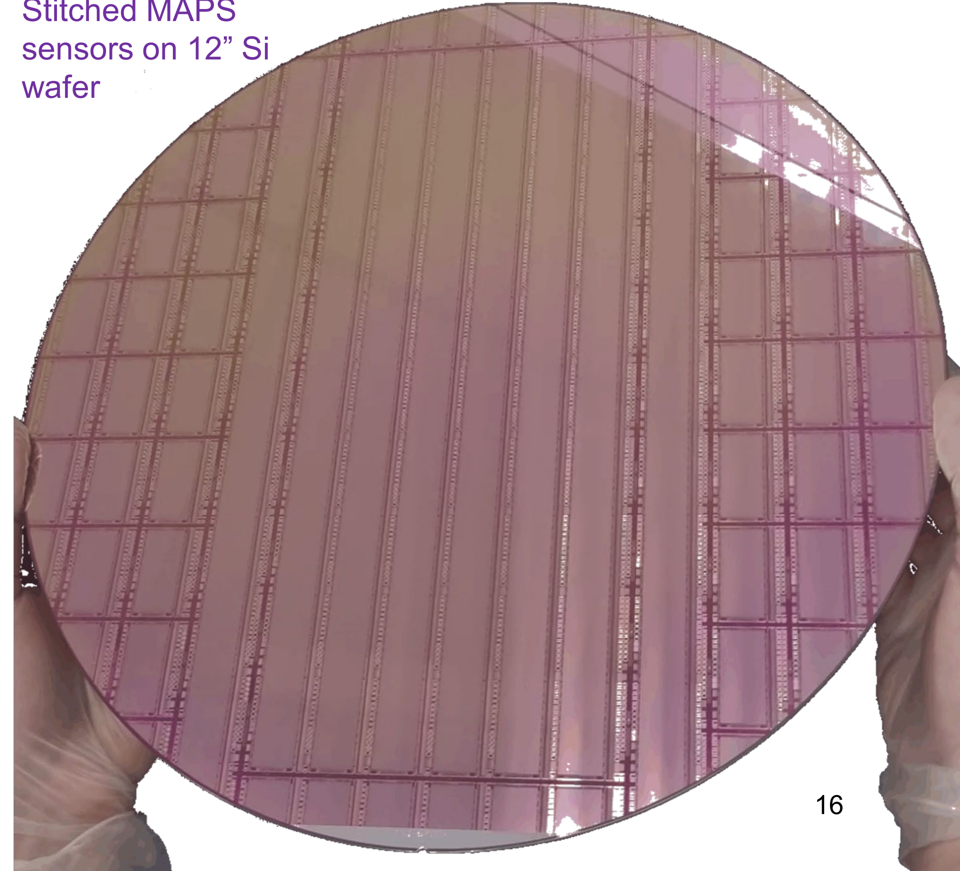


L0 sensor: 3 x 12 RSU
L1 sensor: 4 x 12 RSU
L2 sensor: 5 x12 RSU



ALICE –ITS3 TDR and technical presentations

Stitched MAPS sensors on 12" Si wafer



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Some Further Investments

R&D for MAPS

Data Transmission

ps-level timing (28 nm)

Handling SEU (word-level vs. TMR)

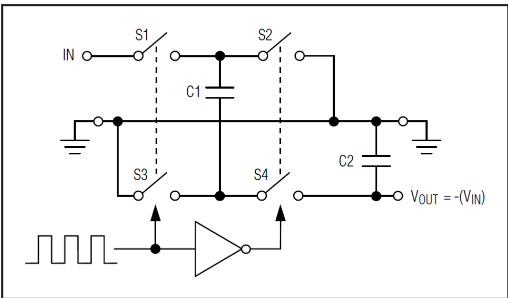
Compound Semiconductors (SiC)

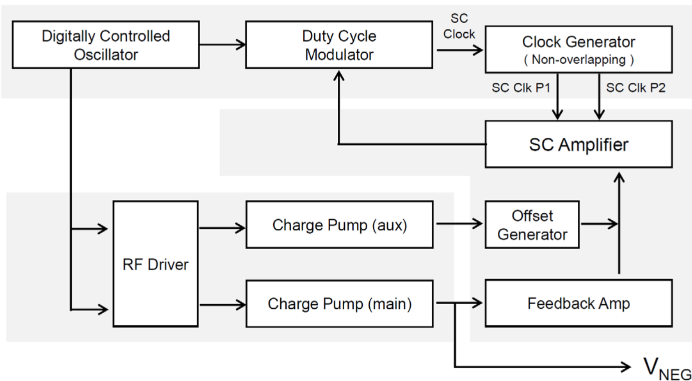
R&D for MAPS 1

Collaboration with CERN, LBNL, RAL, MIT, INFN

Power Management in Serial-Powering: Negative Voltage Generation for biasing sensor, $V_{NEG} \in$ negative (5-10 V)

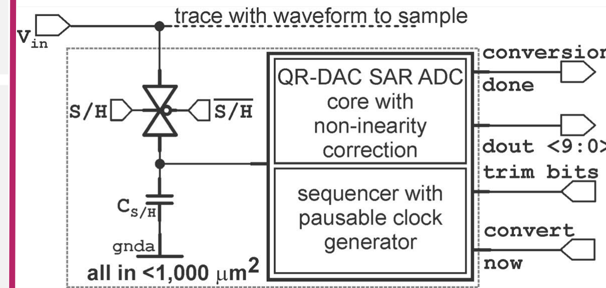
- sensor bias is not serially powered ➡ positive to negative voltage required
- charge pump from positive supply

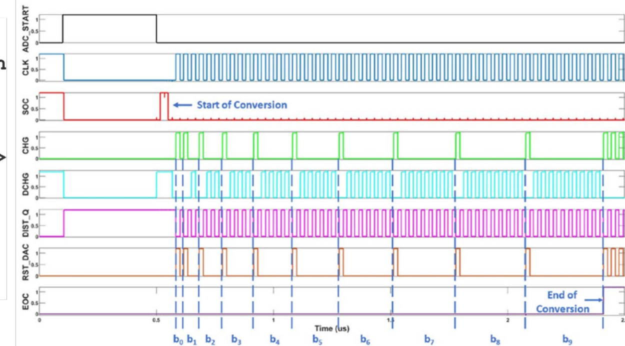




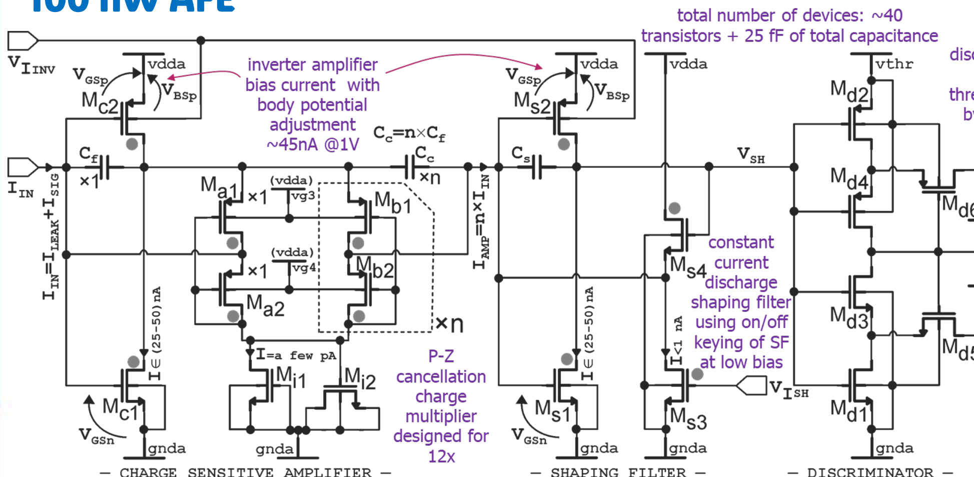
Vital-Function Monitoring ADC for Large-Area MAPS

- Self clocked with sequencer generating pausable clock, <5,000 μm^2 10 b ADC;
- only connection to slow-control

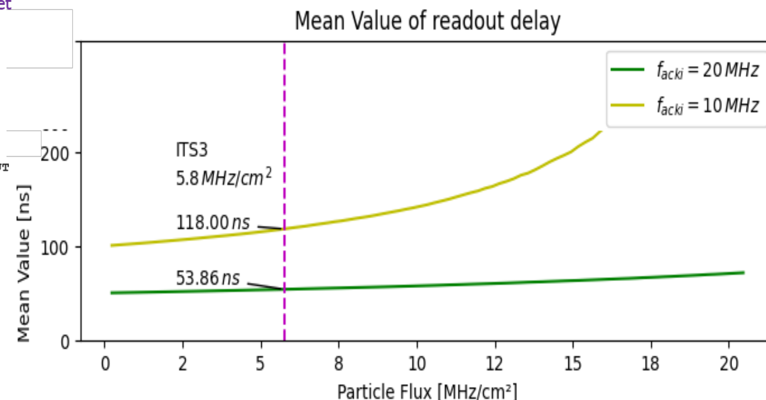


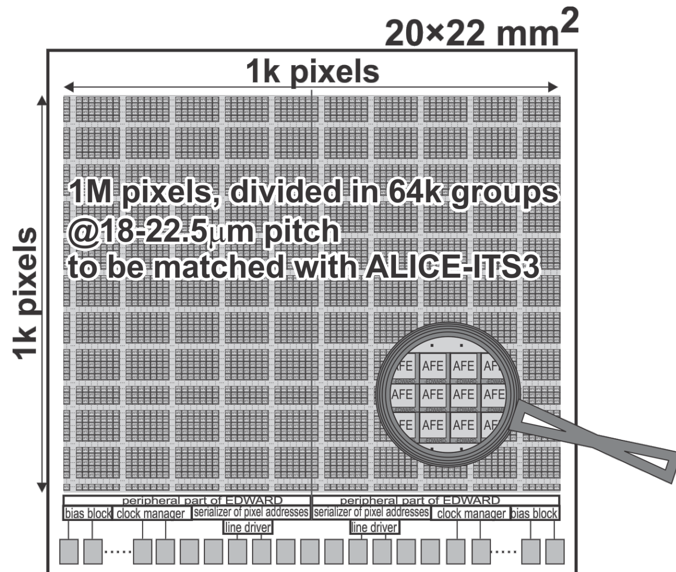


Binary, event-driven mode operated large-area MAPS 100 nW AFE



- ALICE-ITS3 is **priority-encoder** based with **framed readout** ➡ poor σ_t=5 μs);
- **Event-driven** ➡ σ_t=~100 ns);





G. W. Deptuch, "Charge-Sensitive Amplifier with Pole-Zero Cancellation" – patent pending

R&D for MAPS 2

Back-bone Transmission Line Encoding Driver (BTLE - Driver)

- goal: transmit data across stitched sensor (~20 cm) at 160 Mb/s
- to avoid the use of repeaters at boundaries
- high R and C density of metals severely limit bandwidth of wired links across RSUs

160 Mb/s

~ 91% pixel area

ALICE Upgrade Week at CERN: 8 to 12 May 2023

ALICE ITS3: links @ 160 Mbps require inter RSU repeaters ➡ insensitive area;

We want without repeaters

Ideal RCF

Modified RCF

Bias current ≈ 100uA,
Differential current ≈ 100uA

Zin ≈ 100 Ω
Differential swing ≈ 10mV

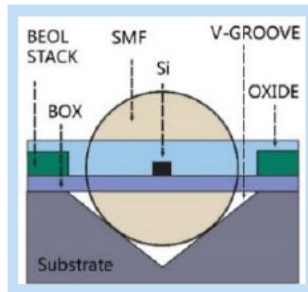
Instead of square wave, stream of synthesized analog symbols are sent ⇨ line encoding

S. Mandal, G.W. Deptuch, A. Iqbal, “A Low-Power Data Link for Stitched Pixel Sensors”, submitted for IEEE MWCAS conference / review

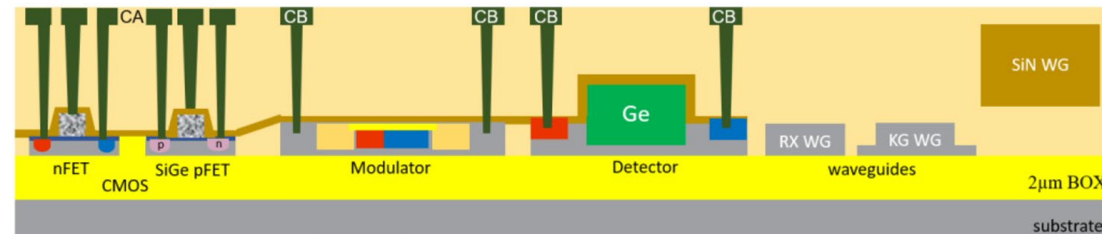
R&D for MAPS 3

Entirely Galvanically Isolated (GalIsol) detector system

- **Power** ➡ by light on fiber (PoF) and PV cells;
- **Slow Control and Reference Clock** ➡ delivered on fiber
- **High-Speed data** ⬅ on fiber, wavelength multiplexed, EOM = Photonic IC (PIC)

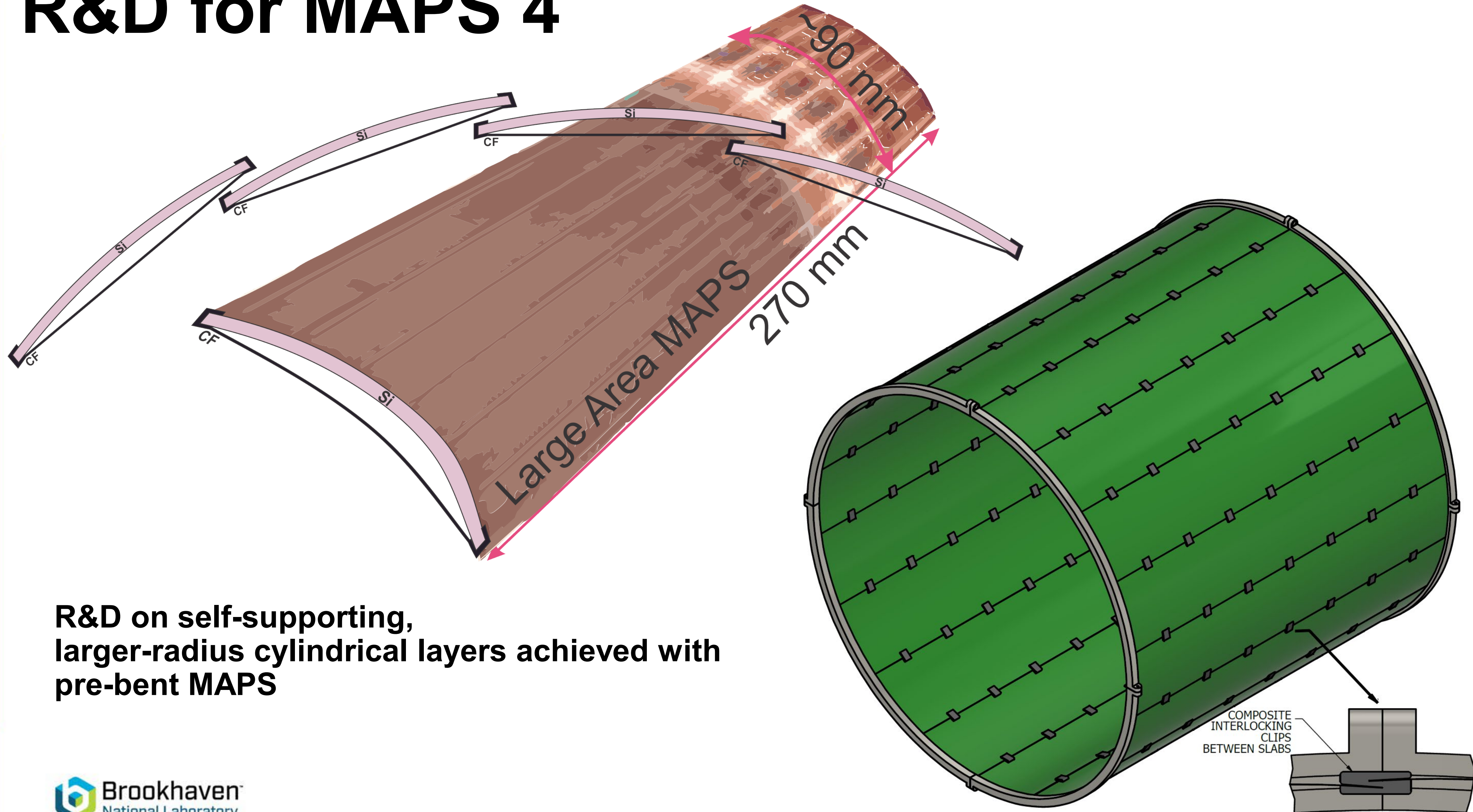


LEFT ENDCAP
RSU
fiber splitter
~99%
~1%
PV cell
PV cell
3.3V
-6.0V
LDO 1.2V(D)
LDO 1.2V(A)
LDO 1.8V(A)
LDO -5.0V (SUB)
top half sensor unit
bottom half sensor unit
lpGBT encoder
lpGBT encoder
slow control (I2C) + reference clock
PIC
data out (mux)
CW laser
reference clock
I2C
data in[0]
data in[n]
TX@10G24
TX@10G24
TX@10G24
TX@10G24
TX@10G24
TX@10G24
passive attach (V-groove)
PCB
MAPS



Attractive for noble liquid detectors

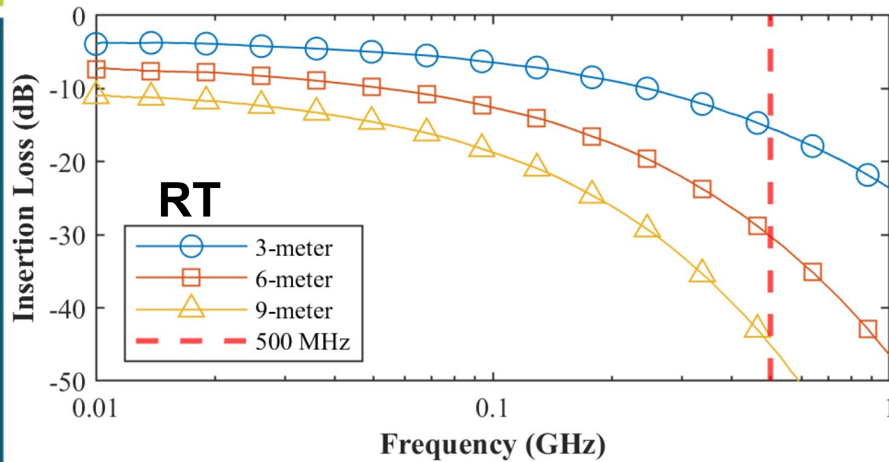
R&D for MAPS 4

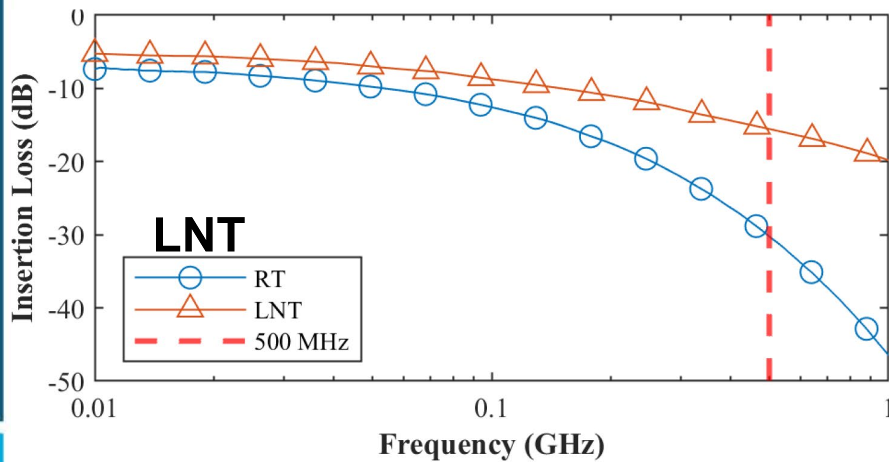


R&D on self-supporting, larger-radius cylindrical layers achieved with pre-bent MAPS

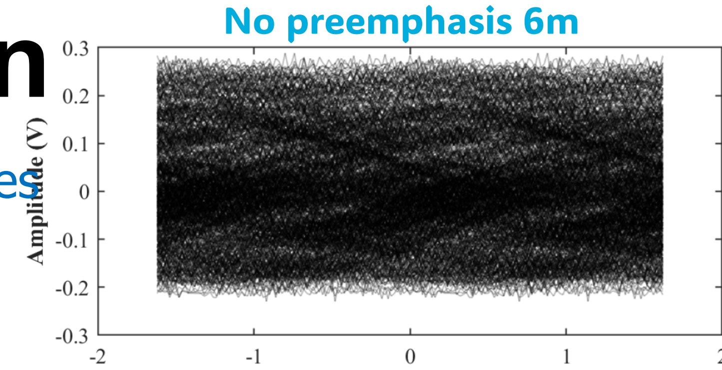
Data transmission

~1Gbps over ~6m of radiopure flex cables

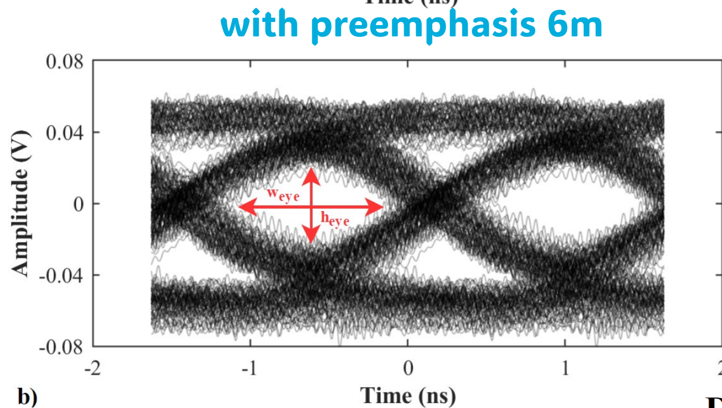


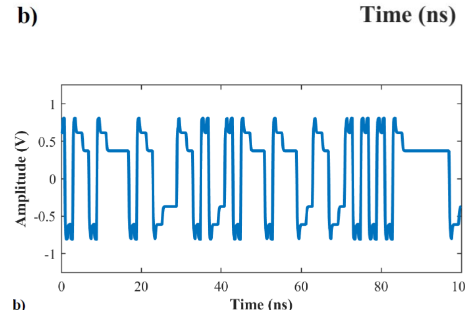


No preemphasis 6m

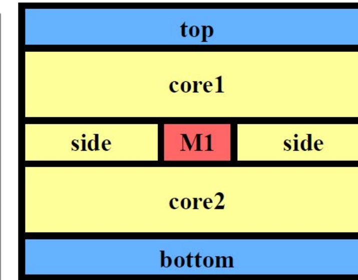


with preemphasis 6m

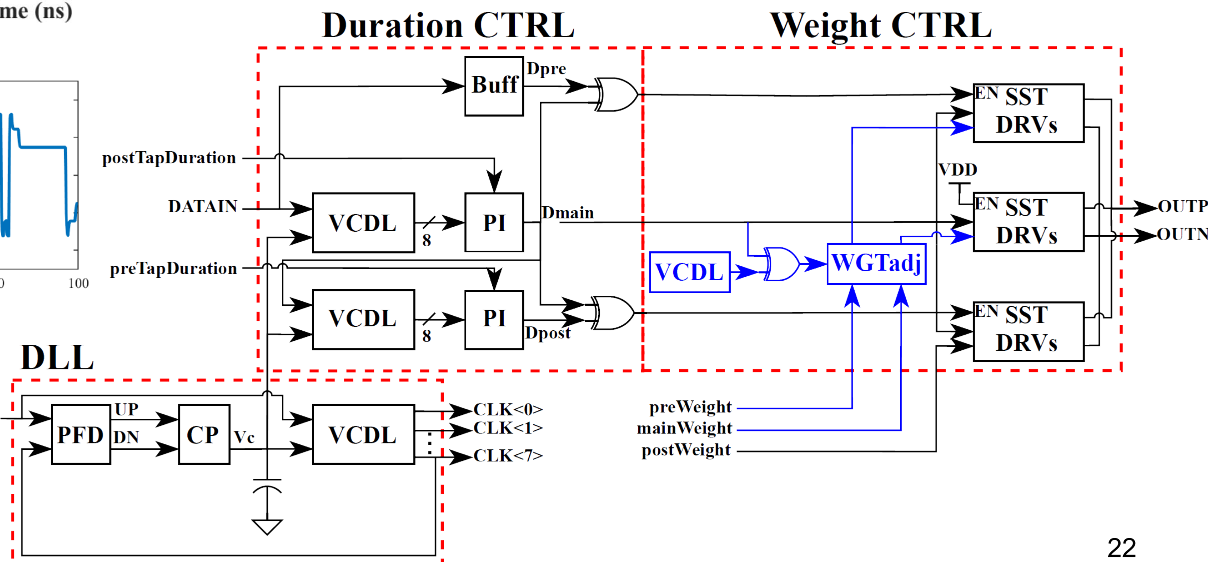




special preemphasis adapted to # 0s or 1s6m



Layer	Thickness	Material
top	17.4 um	Copper
core2	101.6 um	Kapton
side	17.4 um	Kapton
M1	17.4 um	Copper
core1	101.6 um	Kapton
bottom	17.4 um	Copper



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N. St John, et al., "Testing of a line driver with configurable pre-emphasis on lossy transmission lines", submitted for IEEE TNS / review

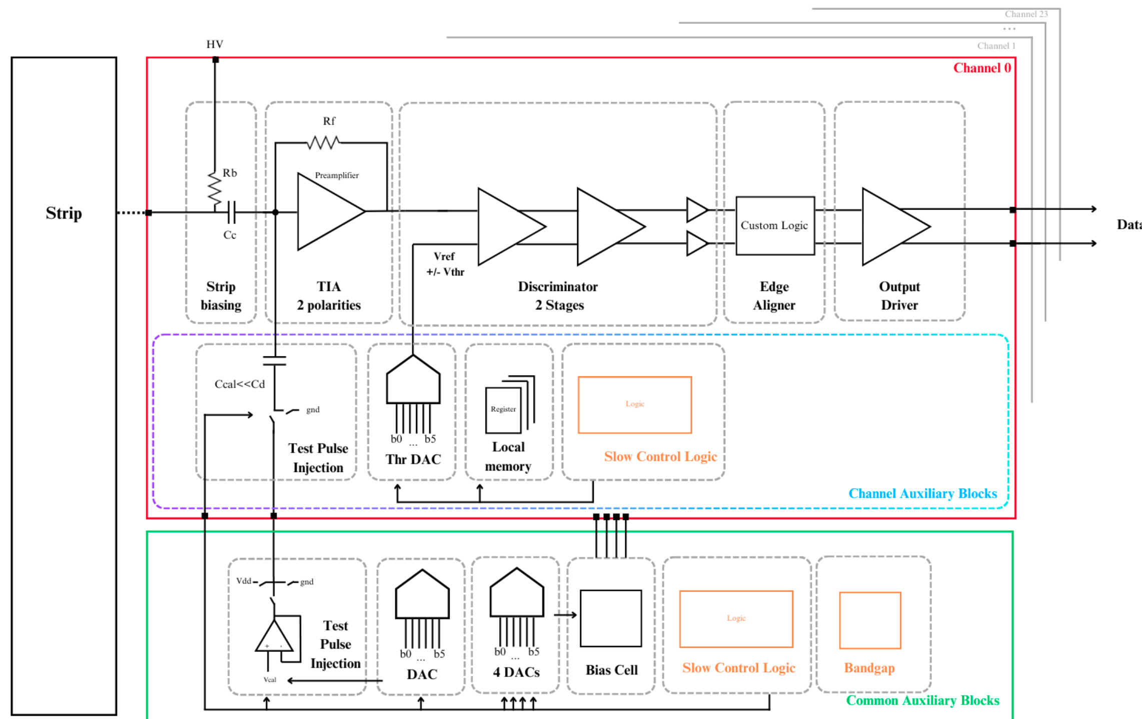
Decananometric process (28 nm)

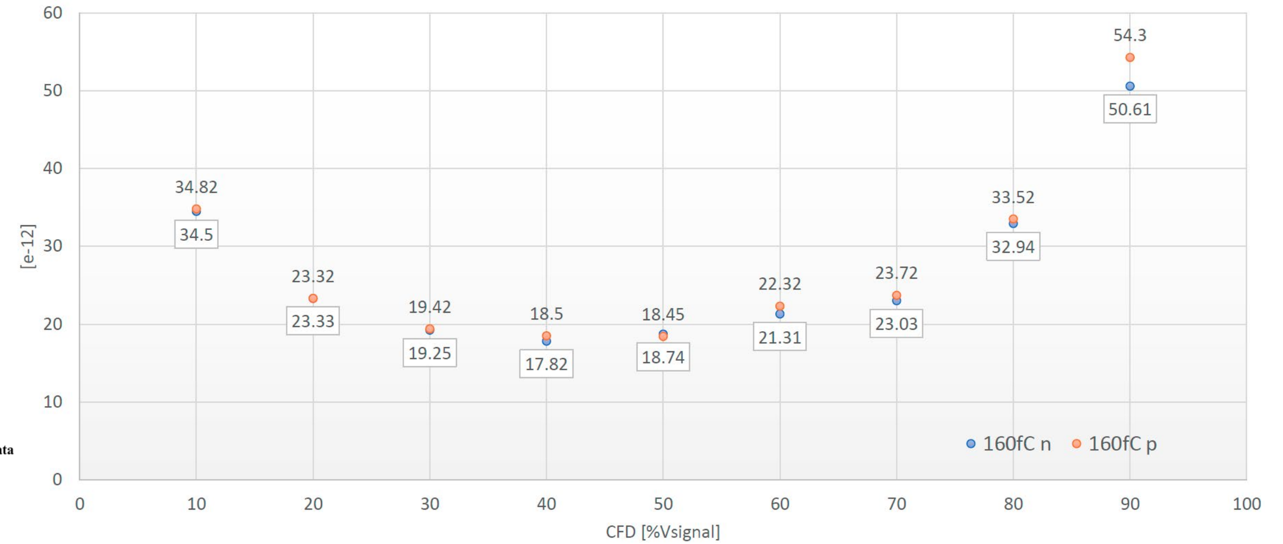
Target application:

Fast-neutron radiography and tomography using Associated Particle Imaging (API) Deuterium-Tritium (D-T) neutron generators.

Follow-up application:

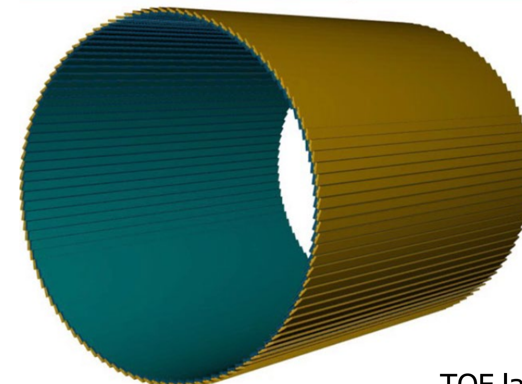
AC-LGAD based TOF systems, e.g., for EIC

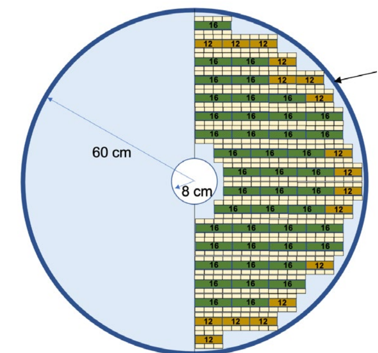




28 nm Amplifier, TIA, Core: Cascoded Inverter+Gain Boosting, 200 MC Transient Noise @ C_{DET}=35 pF

1,200 μA → 795 μW/ch → 19.1 mW (24-channel ASIC)





TOF layers at EIC

- 24-channel, linear layout ASIC, aiming at σ_t=~10-30 ps;
- First step Front-End – Discriminator – Driver than development of TDC

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SEU Mitigation… Comparison

Criteria	Word-Level Correction	Triple Modular Redundancy (TMR)
Objectives	To detect and correct errors within individual words.	To ensure system reliability through redundancy and majority voting.
Implementation Complexity	Can be high; requires complex encoding and decoding mechanisms for error correction.	Moderate; requires triplication of hardware and synchronization mechanisms. However, can leverage tools from HEP Community
Resource Efficiency	Adds overhead for redundant bits.	Requires tripling hardware resources.
Error Detection Capability	Can detect and correct single-bit and potentially multi-bit errors within words.	Can detect discrepancies across modules
Error Correction Capability	Can automatically correct detected errors within the word limit.	Automatically selects the majority output, effectively correcting single-module faults.
Latency/Performance Impact	Adds latency due to error detection and correction processing.	Adds latency due to the need for voting and possibly greater routing complexity.

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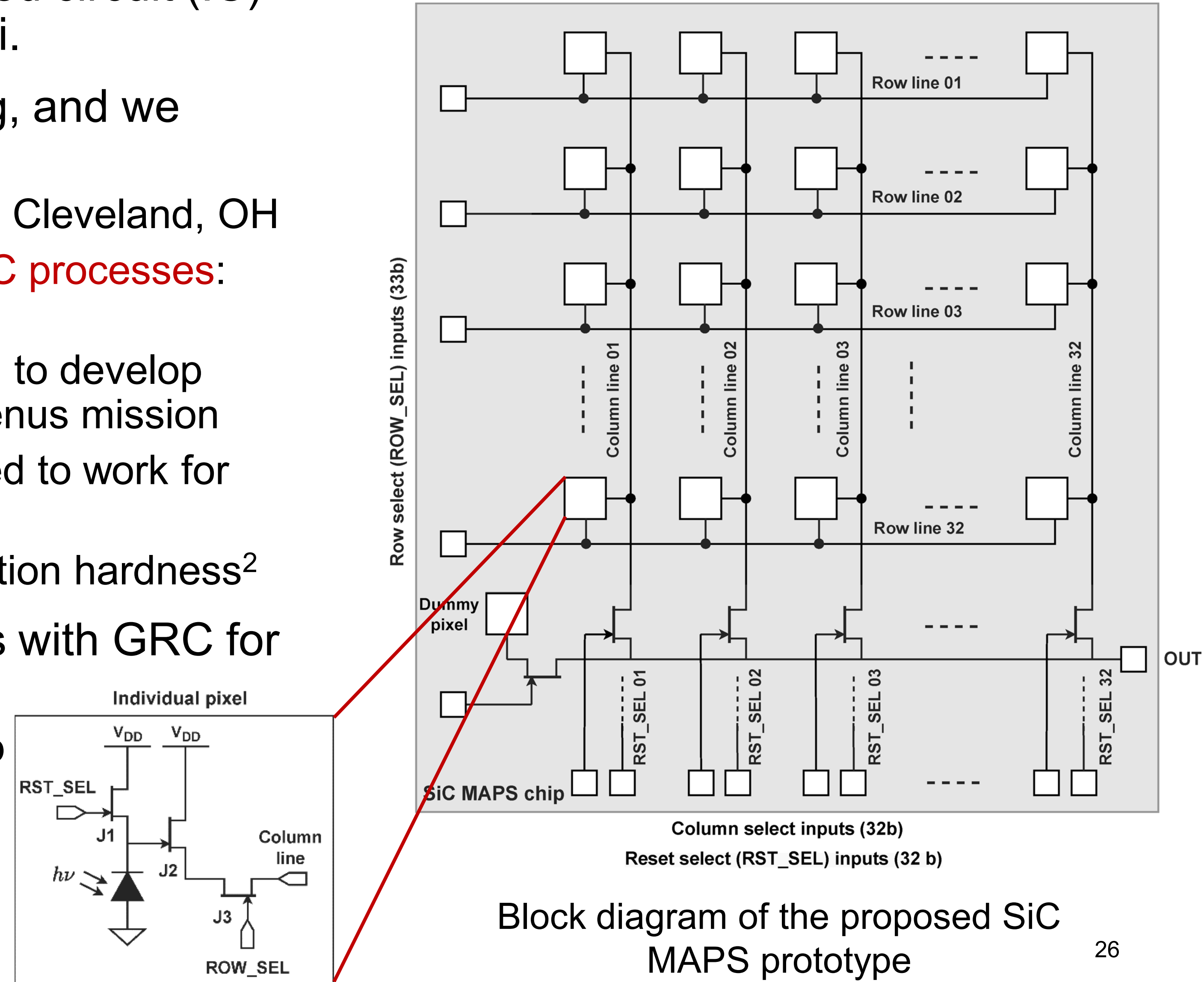
Compound Semi. Materials (sensors/ASICs)

Properties at 300K	Si	4H-SiC	Diamond	GaN
Atomic number (Z)	14	14/6	6	31/7
Density (g/cm^3)	2.33	3.22	3.51	6.15
Relative permittivity, ε_r	11.9	9.7	5.7	9.6
Band gap energy, E_g (eV)	1.12	3.23	5.5	3.39
e-h pair creation energy, ε (eV)	3.6	7.6-8.4	13	8.9
e-h pair creation rate, MIP (eh/μm)	80	57	25	65
Displacement energy, E_d (eV)	13-15	20-35	43	10-20
Breakdown electric field, E_{max} (V/cm)	3×10^5	$3\text{-}4 \times 10^6$	10^7	4×10^6
Electron mobility, μ_e ($cm^2/V.s$)	1450	800-1000	1800-2200	1000
Hole mobility, μ_h ($cm^2/V.s$)	450	50-115	1200-1600	30
Saturated e^- drift velocity, v_{sat} (cm/s)	0.8×10^7	2×10^7	2.2×10^7	1.4×10^7
Thermal conductivity, κ (W/K.cm)	1.5	4.9	24-25	2.5

- Diamond has the best material properties but is difficult to use for implementing electronics.
- 4H-SiC is commercially available and has an excellent combination of material and electronic properties:
  - High band-gap: low dark current, insensitivity to low-energy photons
  - High charge production rate: high sensitivity
  - High displacement energy: radiation hardness
  - High breakdown electric field: high reverse bias voltages
  - High saturation velocity: fast signals, short transit times, low trapping probability

SiC MAPS for FCC-xx

- Bad news: Ecosystem for SiC integrated circuit (IC) fabrication is decades behind that of Si.
- Good news: The ecosystem is growing, and we already have an interested partner.
  - NASA Glenn Research Center (GRC), Cleveland, OH
  - GRC has developed two unique SiC IC processes: SiC-sensor and SiC-JFET
  - The SiC-JFET process has been used to develop many functional circuits for a future Venus mission
  - These circuits have been demonstrated to work for thousands of hours up to 900°C[1]
  - Initial test results show excellent radiation hardness[2]
- We have been engaged in discussions with GRC for several months
  - Collaboration mechanism being set up



Block diagram of the proposed SiC MAPS prototype

[1]P. G. Neudeck, D. J. Spry, M. Krasowski, N. F. Prokop, and L. Y. Chen, in *Materials Science Forum*, 2019, vol. 963, pp. 813–817.

[2]J.-M. Lauenstein *et al.*, in *2019 IEEE Radiation Effects Data Workshop*, 2019, pp. 1–7.

Summary

- **ASIC / microelectronics efforts span broad spectrum of:**
  - applications
  - fabrication processes
  - technologies and techniques (electro-opto-mechanics)
- **Topics**
  - cryogenically operated FEs and readouts
  - advanced readouts
  - Hybrid Pixels and MAPS
  - RF design and deep cryogenic circuits
  - PoF and PICs (integrated photonics)
  - edge processing and beyond-CMOS
  - power management
  - data conversion and transmission
  - decananometric processes (28 nm)
  - TOF and picosecond timing
  - SEU mitigation
  - SiC as next level of radiation hardness