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Enhancing ASIC Verification for HEP with Cocotb and PyUVM

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Over the past decade, functional verification of IP or ASIC/SoCs has been dominated by the SystemVerilog-based Universal Verification Methodology (UVM), which, while offering benefits like reusability and modularity, often adds significant overhead in terms of project costs and deadlines. This is particularly challenging for High Energy Physics (HEP) projects, which require time-constrained and complex verification. Recent efforts aim to reduce this overhead by using structured testbenches, and one promising methodology is the open-source Python coroutine-based co-simulation testbench environment (Cocotb). Cocotb focuses on signal-level stimulus in an event-driven simulator and utilizes Python, which is widely known among physicists, making testbench development more accessible and faster compared to UVM's transaction-level stimulus and SystemVerilog usage. At FermiLab, we applied Cocotb to verify a CMS IP fast command controller and found it significantly reduced verification timelines. Additionally, we implemented PyUVM, a Python-based universal verification methodology offering a systematic approach similar to UVM but with the simplicity of Python. Our study highlights Cocotb and PyUVM as promising alternatives for efficient and effective IP verification in HEP projects.

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