DAPHNE Cross Correlation Self Trigger

General update for SPE-DPE-TPE

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Colombia

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Quick Recap

- The trigger consists of a cross correlation algorithm. Calculating this value is easy using MATLAB's *xcorr* function, but in Hardware it consists of multiplications and additions.
- The trigger has been implemented in DAPHNE_V2's firmware, it is located in the eia_matching_trigger branch.
- All of the different variations of this algorithm that will be presented have been implemented in order to verify resource utilization.
- Our main concern was the DSP usage, up to 91%, with these new versions DSP utilization is reduced to 10%, however the quantity of Logic slices increase. This should not be a concern with DAPHNE V3.

The Average Single Photoelectron and More

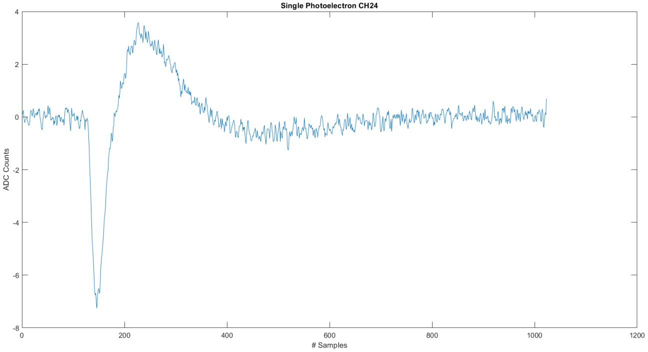
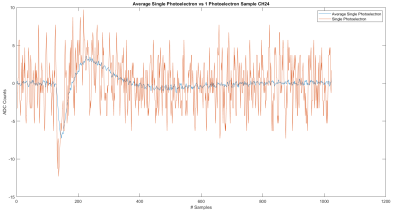
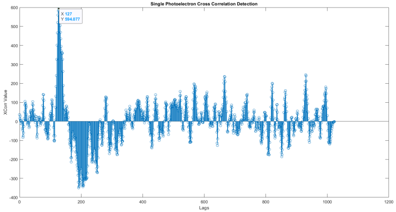


Figure: Average Single Photoelectron

The Average Single Photoelectron and 1 SPE Sample

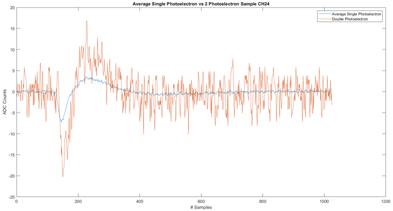


(a) Average Single Photoelectron vs Single PE

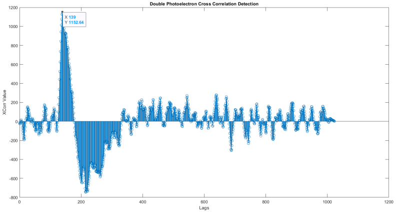


(b) Cross Correlation for the Sample of 1 SPE

The Average Single Photoelectron and 2 SPE Sample

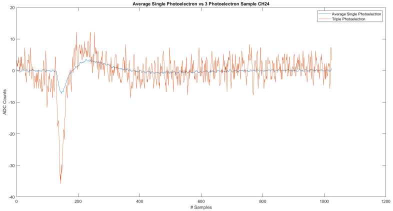


(a) Average Single Photoelectron vs Double PE

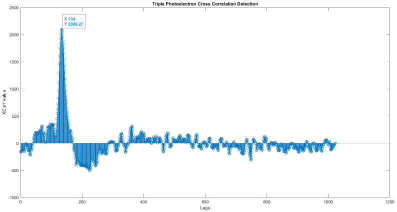


(b) Cross Correlation for the Sample of 2 SPE

The Average Single Photoelectron and 3 SPE Sample

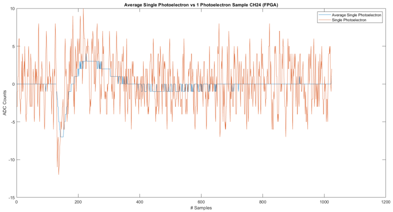


(a) Average Single Photoelectron vs Triple PE

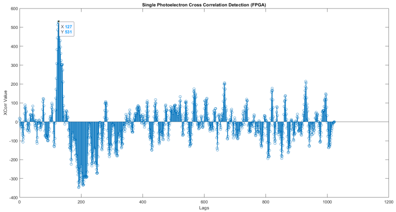


(b) Cross Correlation for the Sample of 3 SPE

Rounding the Data as It Should be Used Inside the FPGA



(a) Average Single Photoelectron vs 1 PE (FPGA)

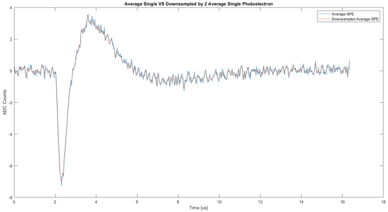


(b) Cross Correlation for the Sample of 1 SPE (FPGA)

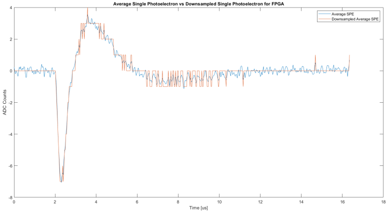
Downsides

- Using 16 registers brings a heavy toll for the FPGA because the DSP usage is pretty high, and also 16 consecutive register is a quarter of the peak seen in these plots.
- Because of this, different strategies were implemented: 16 registers with a downsampling of 4, to cover 1.024μs of signal, and 32 registers with a downsampling of 2, to cover the same length in time.

Undersampling The Template By 2 Clock Ticks

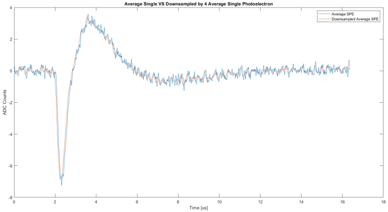


(a) Downsampling the Average SPE by 2

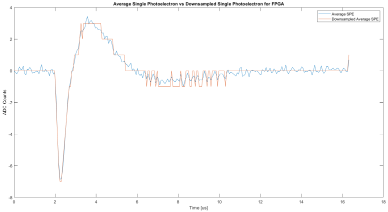


(b) Rounding the Downsampled Signal

Undersampling The Template By 4 Clock Ticks



(a) Downsampling the Average SPE by 4



(b) Rounding the Downsampled Signal

The Initial Template

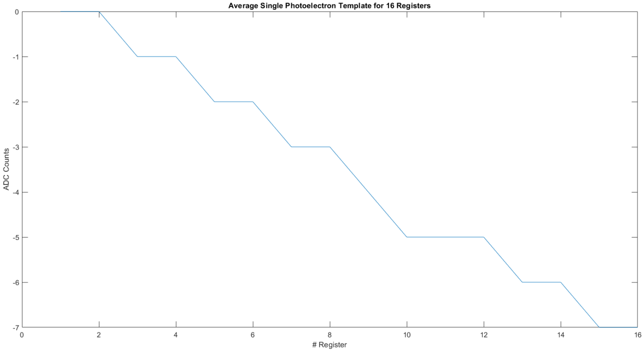
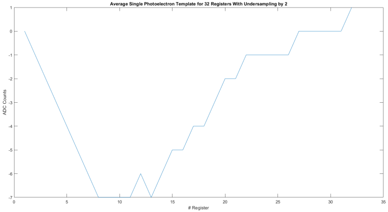
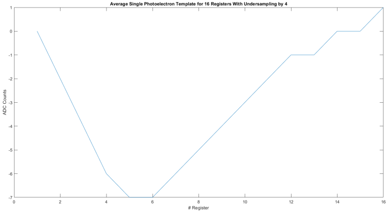


Figure: Template for 16 Regs

The Undersampled Templates



(a) Template for 32 Regs Undersampling=2



(b) Template for 16 Regs Undersampling=4

Compare Each Strategy (1/4)

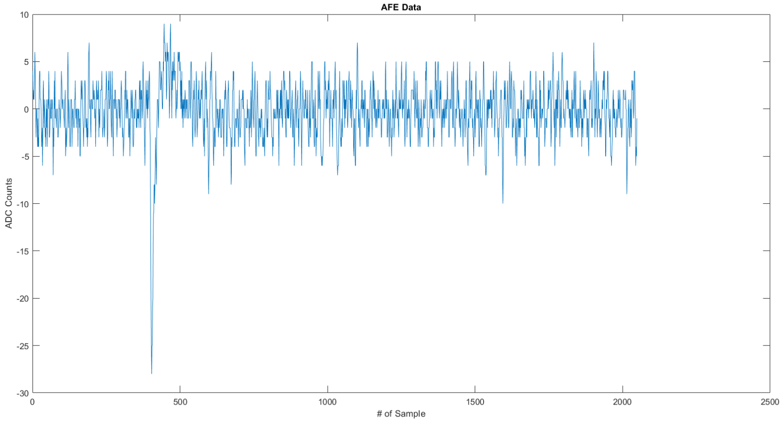
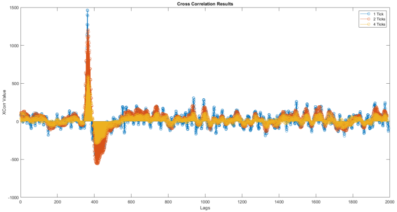
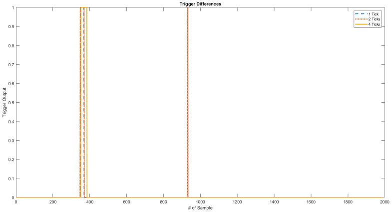


Figure: AFE Sample from Milano #1

Compare Each Strategy (2/4)



(a) Cross Correlation for Each Case



(b) The Trigger for Each Case

Compare Each Strategy (3/4)

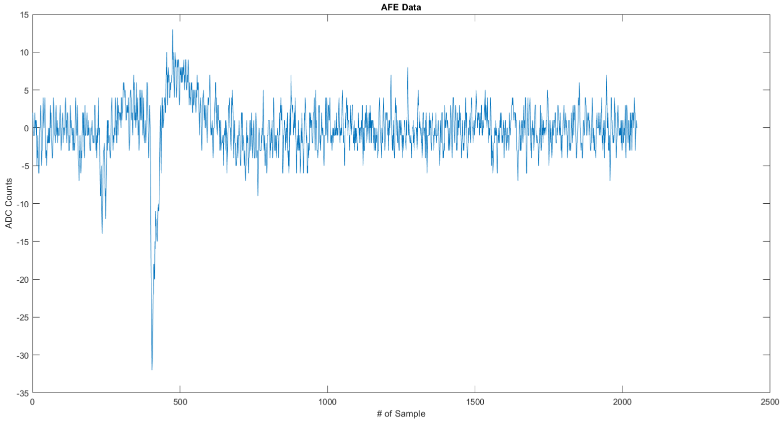
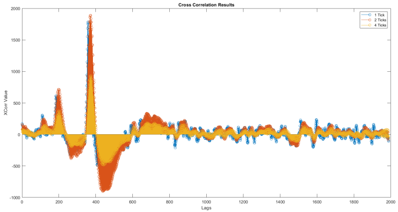
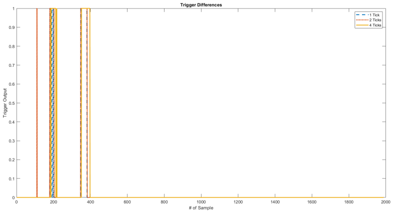


Figure: AFE Sample from Milano #2

Compare Each Strategy (4/4)

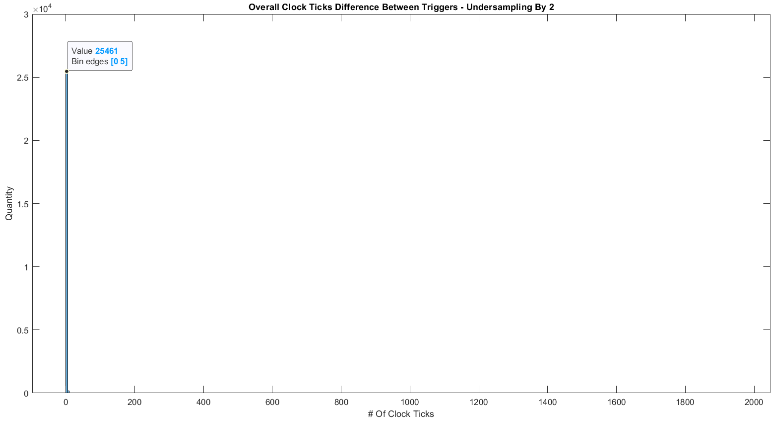


(a) Cross Correlation for Each Case



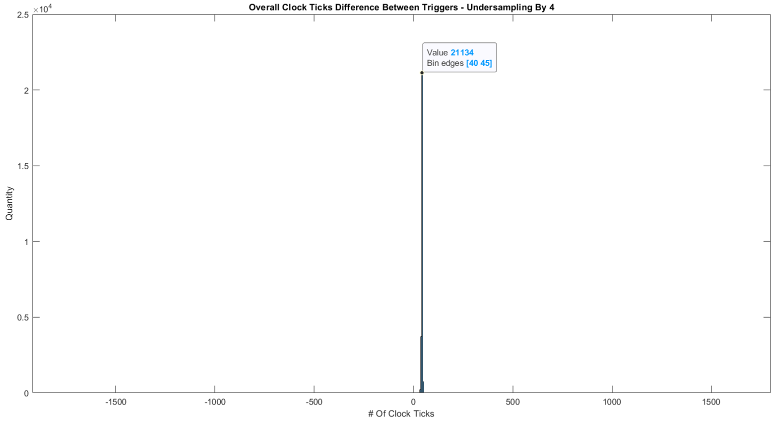
(b) The Trigger for Each Case

How Big Is The Difference? (1/2)



May 9, 2024 Figure: Histogram Downsampling by 2 Trigger Delay

How Big Is The Difference? (2/2)



May 9, 2024 Figure: Histogram Downsampling by 4 Trigger Delay

What About Large Events? (1/2)

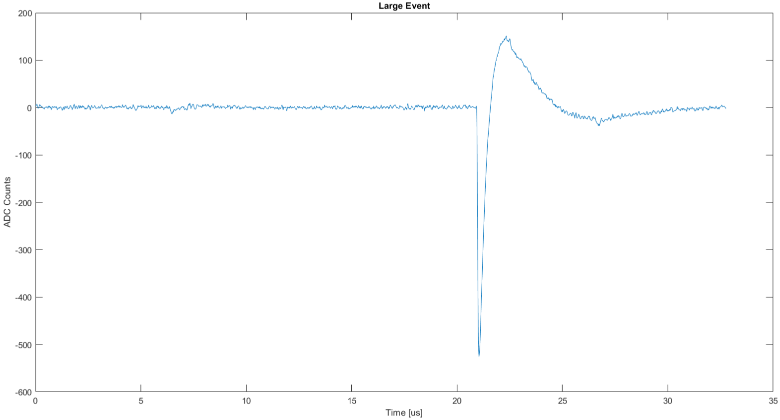
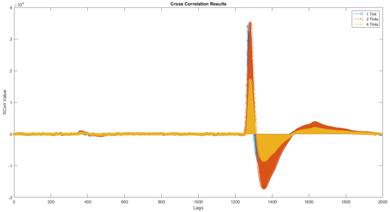
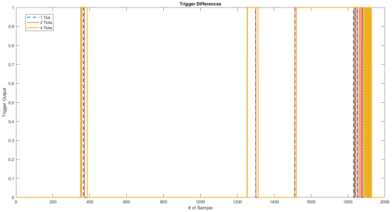


Figure: Hypothetical Large Event

What About Large Events? (2/2)



(a) Cross Correlation for Each Case



(b) The Trigger for Each Case

Self Trigger Block Diagram

Figure: Block Diagram for VHDL

- The module has the same inputs as DAPHNE's simple self trigger, as well as the same outputs. But in this case, the module outputs the baseline, rather than needing it as a prior input.
- Threshold window can be set through registers, to change detection if the user wants to ignore Singles, or Doubles, or keep them and ignore large events.

Baseline Calculation Capabilities

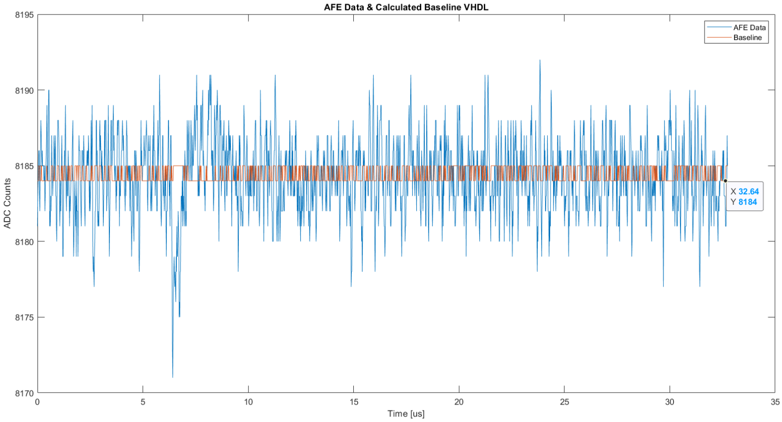


Figure: AFE Data vs Calculated Baseline

Some of the Module's Signals in Simulation

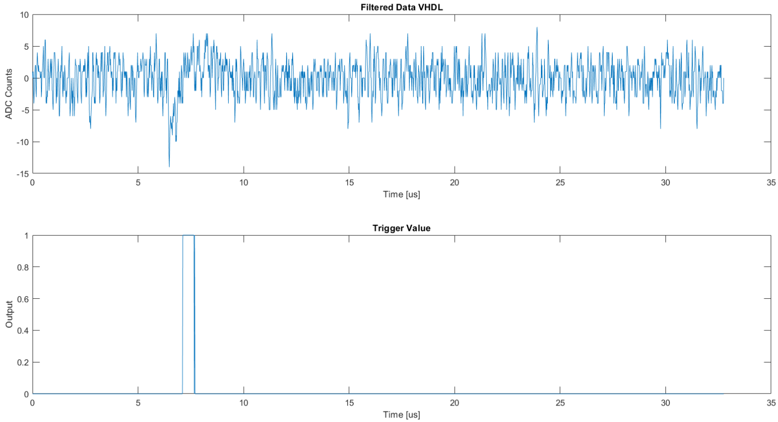


Figure: Full Trigger Output VHDL Sim

Simulation in VHDL for Large Event (1/2)

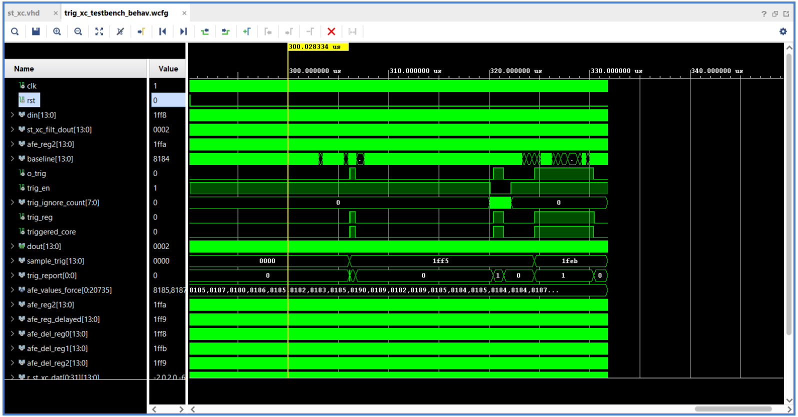


Figure: VHDL Simulation for Large Event With Trigger Disabled

Simulation in VHDL for Large Event (2/2)

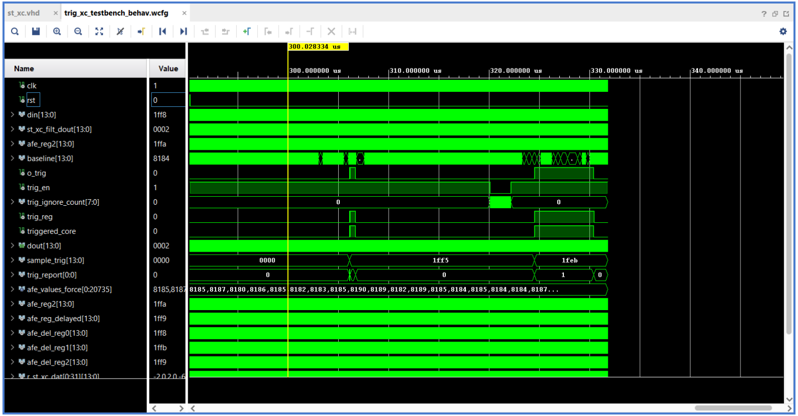


Figure: VHDL Simulation for Large Event With Trigger Enabled

Implementation for DAPHNE firmware and 40 Channels

2. Slice Logic Distribution

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice	19583	0	200	33450	58.54
SLICEL	12085	0			
SLICEM	7498	0			
LUT as Logic	53447	0	800	133800	39.95
using O5 output only	280				
using O6 output only	40290				
using O5 and O6	12877				
LUT as Memory	9670	0	0	46200	20.93
LUT as Distributed RAM	18	0			
using O5 output only	0				
using O6 output only	18				
using O5 and O6	0				
LUT as Shift Register	9652	0			
using O5 output only	10				
using O6 output only	6514				
using O5 and O6	3128				
Slice Registers	35248	0	0	269200	13.09
Register driven from within the Slice	20957				
Register driven from outside the Slice	14291				
LUT in front of the register is unused	5453				
LUT in front of the register is used	8838				
Unique Control Sets	796		200	33450	2.38

* * Note: Available Control Sets calculated as Slice * 1, Review the Control Sets Report for more information regarding control sets.

(a) Resource Utilization for 16 Registers by Undersampling of 4

2. Slice Logic Distribution

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice	25581	0	200	33450	76.48
SLICEL	16238	0			
SLICEM	9343	0			
LUT as Logic	72255	0	800	133800	54.00
using O5 output only	443				
using O6 output only	53734				
using O5 and O6	18078				
LUT as Memory	14150	0	0	46200	30.63
LUT as Distributed RAM	18	0			
using O5 output only	0				
using O6 output only	18				
using O5 and O6	0				
LUT as Shift Register	14132	0			
using O5 output only	10				
using O6 output only	7634				
using O5 and O6	6488				
Slice Registers	46324	0	0	269200	17.21
Register driven from within the Slice	32394				
Register driven from outside the Slice	13930				
LUT in front of the register is unused	4411				
LUT in front of the register is used	9519				
Unique Control Sets	886		200	33450	2.65

* * Note: Available Control Sets calculated as Slice * 1, Review the Control Sets Report for more information regarding control sets.

(b) Resource Utilization for 32 Registers by Undersampling of 2

NP04 Results at CERN (1/2)

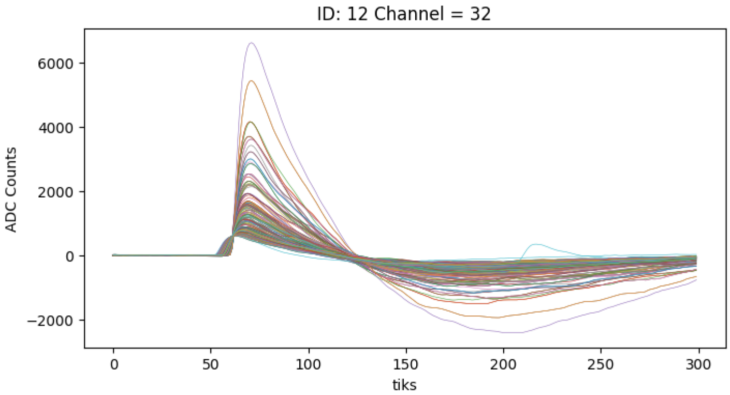


Figure: Simple Threshold Trigger Event Detection at NP04.

NP04 Results at CERN (2/2)

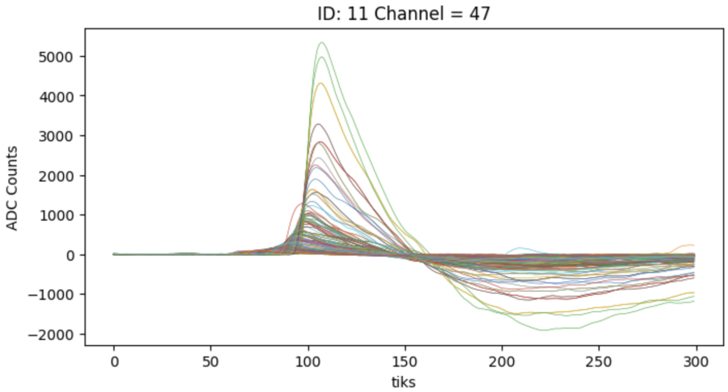


Figure: Matching Trigger Event Detection at NP04.

Conclusions

- The self trigger module can be used to calculate a baseline for any other module/logic that needs it, or including it in the self trigger frame.
- The self trigger would fit with CIEMAT's primitives in a full design for 40 channels for sure if 16 registers are used, with 32 this is uncertain but removing some repeated logic would improve this situation.
- The module should be capable of finding events that lie in the range between both Single Photoelectrons and large events, but the last must go through more simulations. Update: The module has already been tested. It was capable of detecting signals within a window, both small and large but not that big, the main issue is the jitter between each trigger.

What is next

- More simulations and verifications will be performed to validate the trigger capabilities for dealing with really large events and the jitter it has.
- The module must be tested within a really small events window, in order to see how good it is catching Single PEs. This will be done in the course of these next two weeks.
- Although we consider the filter output to be performing really well, the baseline calculation might be affected by huge events, so we would like to continue fine tuning it.
- More comments will be added to the code in order to make it easier to understand and maintain.

DUNE

DEEP UNDERGROUND NEUTRINO EXPERIMENT