## DAPHNE Cross Correlation Self Trigger General update for SPE-DPE-TPE

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### **Quick Recap**

- The trigger consists of a cross correlation algorithm. Calculating this value is easy using MATLAB's *xcorr* function, but in Hardware it consists of multiplications and additions.
- The trigger has been implemented in DAPHNE\_V2's firmware, it is located in the eia\_matching\_trigger branch.
- All of the different variations of this algorithm that will be presented have been implemented in order to verify resource utilization.
- Our main concern was the DSP usage, up to 91%, with these new versions DSP utilization is reduced to 10%, however the quantity of Logic slices increase. This should not be a concern with DAPHNE V3.



### The Average Single Photoelectron and More



Figure: Average Single Photoelectron



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### The Average Single Photoelectron and 1 SPE Sample



(a) Average Single Photoelectron vs Single PE



(b) Cross Correlation for the Sample of 1 SPE



## The Average Single Photoelectron and 2 SPE Sample



(a) Average Single Photoelectron vs Double PE



(b) Cross Correlation for the Sample of 2 SPE



## The Average Single Photoelectron and 3 SPE Sample



(a) Average Single Photoelectron vs Triple PE



(b) Cross Correlation for the Sample of 3 SPE



# Rounding the Data as It Should be Used Inside the FPGA



(a) Average Single Photoelectron vs 1 PE (FPGA)



(b) Cross Correlation for the Sample of 1 SPE (FPGA)



### **Downsides**

- Using 16 registers brings a heavy toll for the FPGA because the DSP usage is pretty high, and also 16 consecutive register is a quarter of the peak seen in these plots.
- Because of this, different strategies were implemented: 16 registers with a downsampling of 4, to cover 1.024µs of signal, and 32 registers with a downsampling of 2, to cover the same length in time.



## **Undersampling The Template By 2 Clock Ticks**



(a) Downsampling the Average SPE by 2



(b) Rounding the Downsampled Signal



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## **Undersampling The Template By 4 Clock Ticks**



(a) Downsampling the Average SPE by 4



(b) Rounding the Downsampled Signal



## **The Initial Template**



Figure: Template for 16 Regs



## **The Undersampled Templates**



(a) Template for 32 Regs Undersampling=2



(b) Template for 16 Regs Undersampling=4



# Compare Each Strategy (1/4)



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Figure: AFE Sample from Milano #1



## Compare Each Strategy (2/4)



(a) Cross Correlation for Each Case



(b) The Trigger for Each Case



## Compare Each Strategy (3/4)



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Figure: AFE Sample from Milano #2



# Compare Each Strategy (4/4)



(a) Cross Correlation for Each Case



(b) The Trigger for Each Case



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# How Big Is The Difference? (1/2)



May 9, 2024 Figure: Histogram Downsampling by 2 Trigger Delay



# How Big Is The Difference? (2/2)



May 9, 2024 Figure: Histogram Downsampling by 4 Trigger Delay



# What About Large Events? (1/2)



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Figure: Hypothetical Large Event



# What About Large Events? (2/2)



(a) Cross Correlation for Each Case



(b) The Trigger for Each Case



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# Self Trigger Block Diagram



Figure: Block Diagram for VHDL

- The module has the same inputs as DAPHNE's simple self trigger, as well as the same outputs. But in this case, the module outputs the baseline, rather than needing it as a prior input.
- Threshold window can be set through registers, to change detection if the user wants to ignore Singles, or Doubles, or keep them and ignore large events.



## **Baseline Calculation Capabilities**



May 9, 2024 Figure: AFE Data vs Calculated Baseline



### Some of the Module's Signals in Simulation



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Figure: Full Trigger Output VHDL Sim



## Simulation in VHDL for Large Event (1/2)



Figure: VHDL Simulation for Large Event With Trigger Disabled



## Simulation in VHDL for Large Event (2/2)



Figure: VHDL Simulation for Large Event With Trigger Enabled



### **Implementation for DAPHNE firmware and 40 Channels**

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(a) Resource Utilization for 16 Registers by Undersampling of 4

(b) Resource Utilization for 32 Registers by Undersampling of 2



# NP04 Results at CERN (1/2)



Figure: Simple Threshold Trigger Event Detection at NP04.



# NP04 Results at CERN (2/2)



Figure: Matching Trigger Event Detection at NP04.



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## Conclusions

- The self trigger module can be used to calculate a baseline for any other module/logic that needs it, or including it in the self trigger frame.
- The self trigger would fit with CIEMAT's primitives in a full design for 40 channels for sure if 16 registers are used, with 32 this is uncertain but removing some repeated logic would improve this situation.
- The module should be capable of finding events that lie in the range between both Single Photoelectrons and large events, but the last must go through more simulations. Update: The module has already been tested. It was capable of detecting signals within a window, both small and large but not that big, the main issue is the jitter between each trigger.



### What is next

- More simulations and verifications will be performed to validate the trigger capabilities for dealing with really large events and the jitter it has.
- The module must be tested within a really small events window, in order to see how good it is catching Single PEs. This will be done in the course of these next two weeks.
- Although we consider the filter output to be performing really well, the baseline calculation might be affected by huge events, so we would like to continue fine tuning it.
- More comments will be added to the code in order to make it easier to understand and maintain.



