

# DCEM1.3 backup for Module 0 replacement

Test @ Fermilab

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# Boards summary 1: 8x backup boards

Boards have been set and tested with 4x HPK flexes in LAr using the same testing DCDC.

## 4x: CMOS setup (1,2,3,4)

DCEM 3 and 4 are boards recycled from Jan 2024 cold box. Those two have their own DCDC installed.

### List of changes:

- **C9, C27, R5, R11, R24, R30, R17, R36:** removed and left open
- **R1, R20:** replaced with **8.2k Ohm**
- **C10, C26:** replaced with **0 Ohm**
- **R18, R37:** replaced with **160 Ohm**

Changes listed here are made from the original scheme shown in the following slides.

## 4x: BiPolar+Transistor setup (5,6,7,8)

### List of changes:

- **U1,U2,U3,U4:** replaced with **LMH6642**
- **Q1, Q2:** installed **MT3S11**
- **C9, C27, R5, R24, R10, R29, R17, R36:** removed and left open
- **R1, R20:** replaced with **8.2k Ohm**
- **C10, C26:** replaced with **510 Ohm**
- **R11, R30:** replaced with **510 Ohm**
- **R18, R37:** replaced with **81 Ohm**
- **510 Ohm** bridge between **U2, U4:** place a inputs (legs 2, 3)

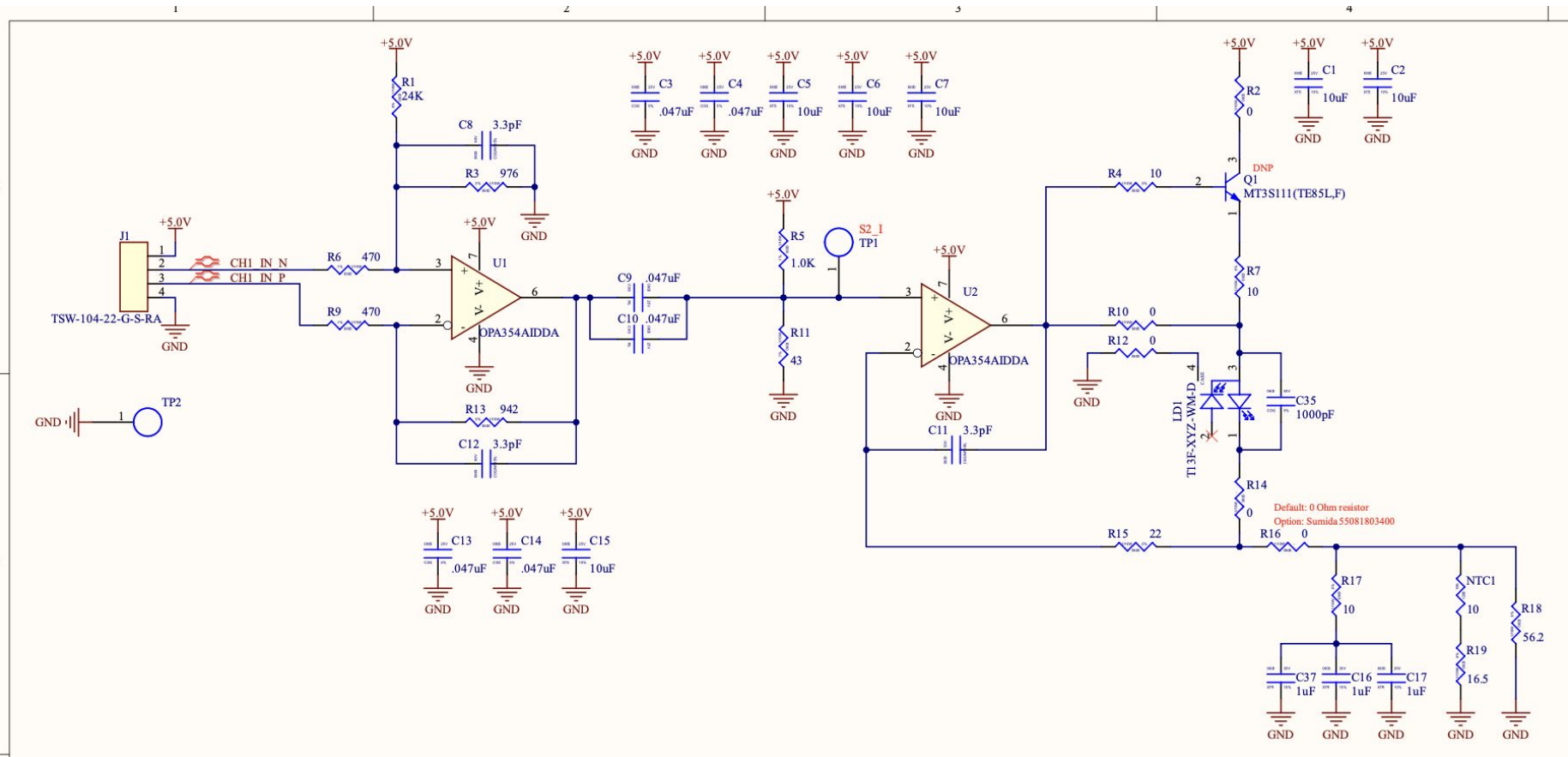
# Summary 2:

Same DCDC for [1,2, 5,6,7,8] [3, 4] have their own DCDC			Room T, no flexes connected						LAr, 4x HPK flex connecte in ch 2					
DCEM	Type	V_bias (V)	I (mA)	DCDC out (V)	DCDC LDO (V)	OpAmp LDO (V)	Offset Ch1 (mV)	Offset Ch2 (mV)	I (mA)	DCDC out (V)	DCDC LDO (V)	OpAmp LDO (V)	Offset Ch1 (mV)	Offset Ch2 (mV)
1	CMOS	5.3	124	56.3	4.99	4.99	185	195	60	47.0	5.02	5.00	135	117
2	CMOS	5.3	124	56.4	4.98	4.99	187	181	60	47.0	5.03	5.00	97	87
3	CMOS	5.3	126	56.4	4.98	5.00	205	184	60	47.0	4.93	4.95	125	83
4	CMOS	5.3	126	56.4	5.00	4.98	204	154	60	47.1	5.01	4.92	115	90
5	BiPolar	5.3	104	56.4	4.99	4.99	46	56	54	47.0	5.00	4.97	81	74
6	BiPolar	5.3	105	56.3	4.99	4.98	48	45	55	47.0	4.98	5.02	103	104
7	BiPolar	5.3	104	56.5	4.98	4.99	37	37	55	47.0	5.01	5.01	90	102
8	BiPolar	5.3	105	56.4	4.98	5.00	45	47	54	47.0	5.01	5.02	97	103

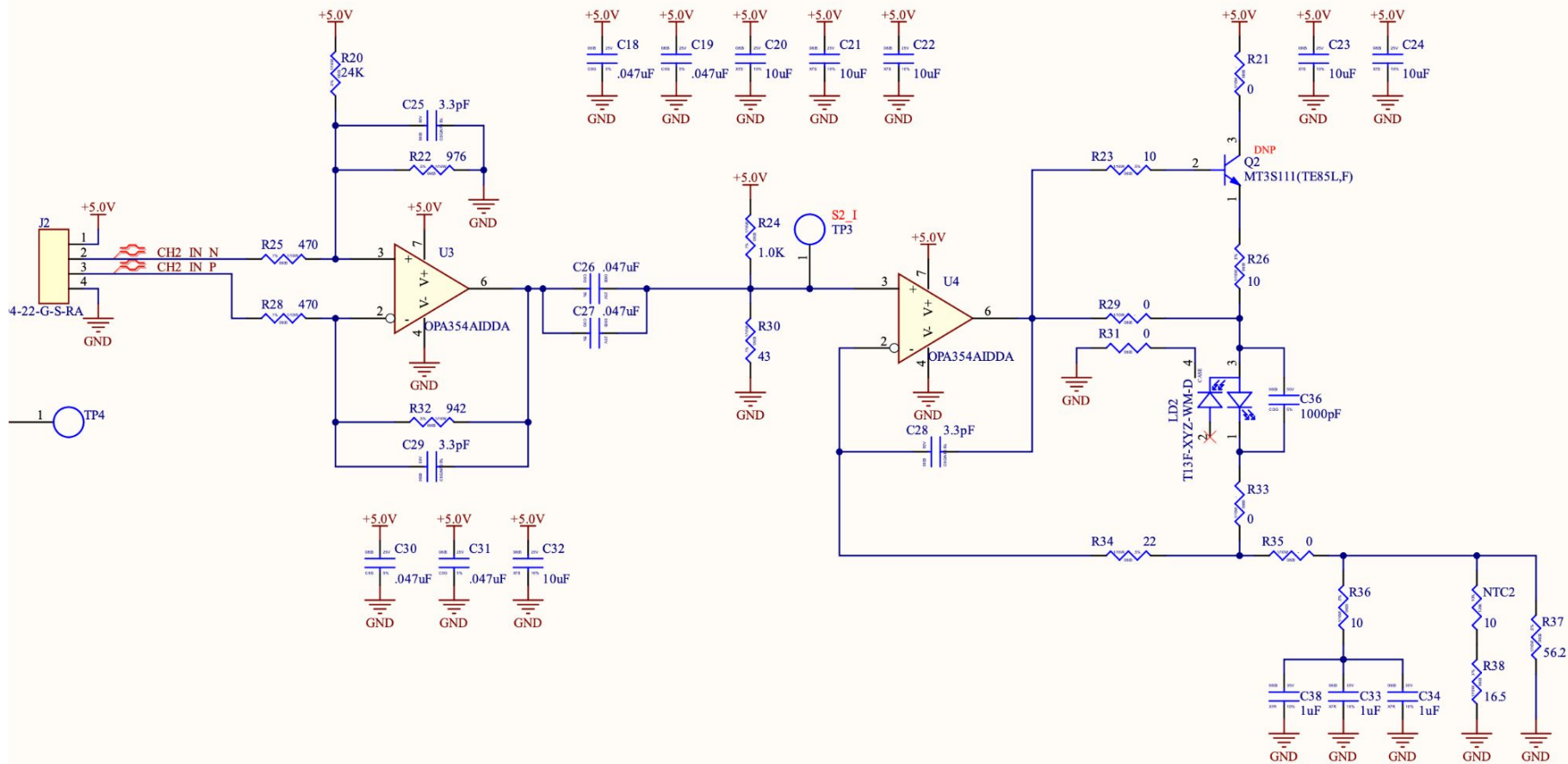
# Summary 3:

4x HPK flex, LAr, DCDC		SNR		SNR (20 MhZ cut)		<SPE> ampl (mV)		Dynamic Range (Number of PE)		Undershoot (%)	
DCEM	Type	Ch1	Ch2	Ch1	Ch2	Ch1	Ch2	Ch1	Ch2	Ch1	Ch2
1	CMOS	8.0	6.8	8.1	8.3	1.1	1.2	1545	1417	1.9	1.5
2	CMOS	9.8	7.1	7.3	8.0	1.0	0.8	1600	1500	1.7	1.8
3	CMOS	8.5	5.1	9.2	5.2	1.0	1.0	1600	1600	1.8	2.1
4	CMOS	10.1	4.7	9.8	4.6	1.1	1.0	1545	1500	1.5	1.7
5	BiPolar	7.1	7.8	7.9	8.2	0.8	0.8	2000	2000	2.0	1.7
6	BiPolar	8.0	7.2	9.3	7.1	1.0	1.0	1700	1700	1.7	2.2
7	BiPolar	7.6	8.1	8.3	8.0	0.9	1.0	1889	1700	2.8	1.7
8	BiPolar	8.8	6.3	9.7	10.1	1.0	1.1	1700	1545	1.8	1.3

# Laser card Ch 1, original schematic



# Laser card Ch 2, original schematic



# DCEM #1, CMOS, HPK, DCDC\_test

## DCEM #1

### Room T

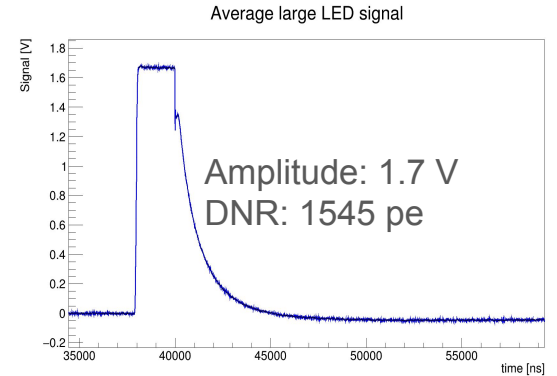
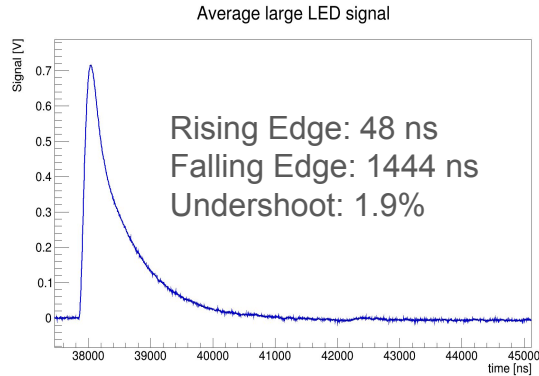
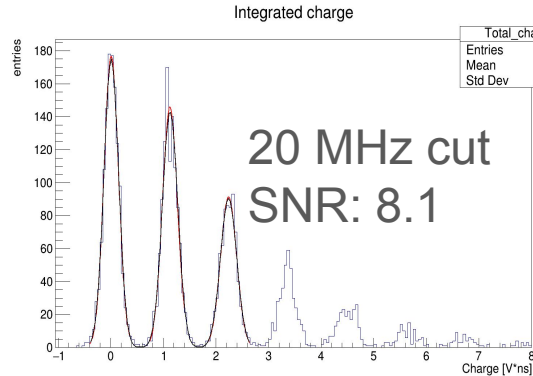
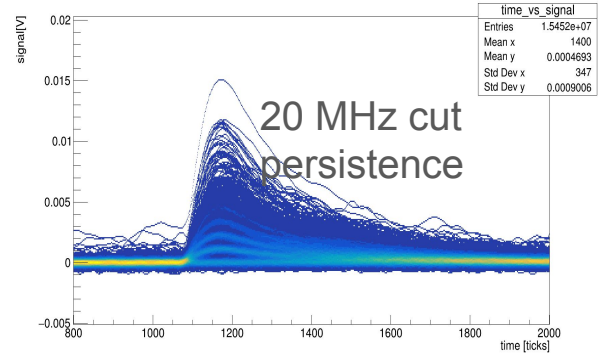
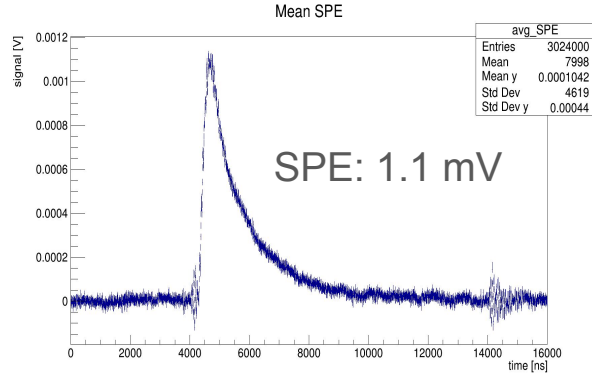
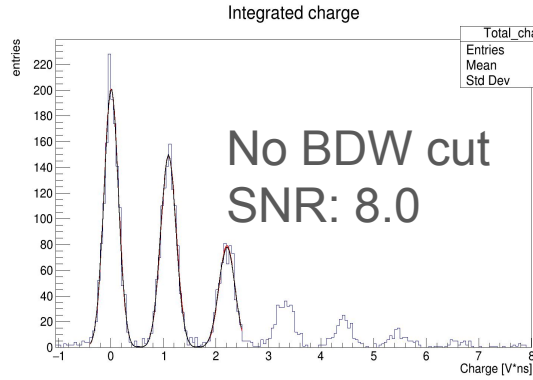
No flex, test DCDC,  
V\_bias= 5.3V,  
I=124 mA,  
DCDC out=56.3V,  
LDO\_DCDC= 4.99V,  
LDO\_OpAmp=4.99V,  
Offset Ch1=185 mV  
Offset Ch2=195 mV

## DCEM #1

### LAr

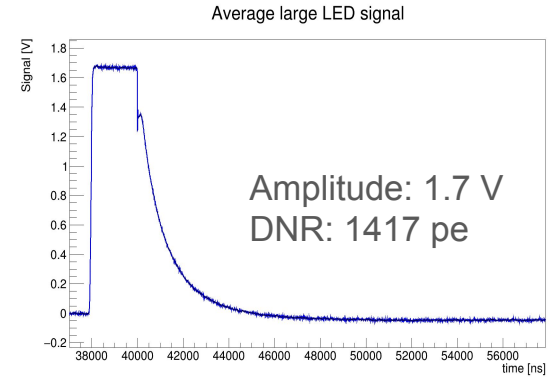
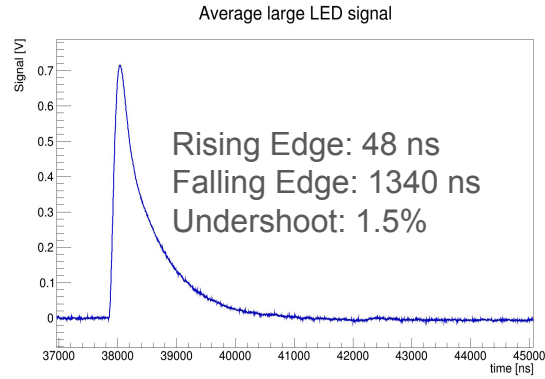
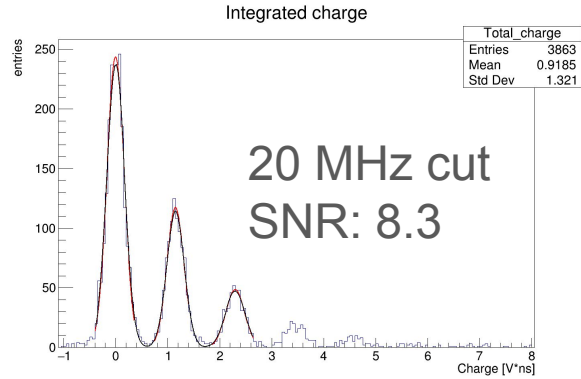
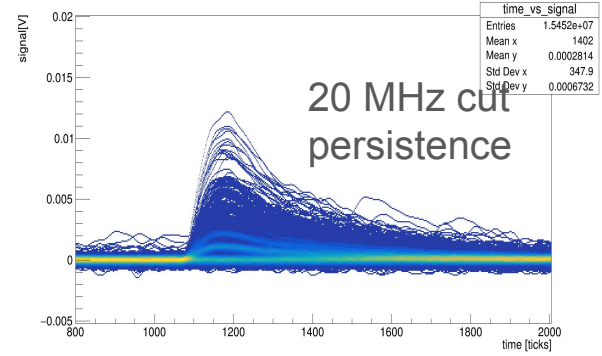
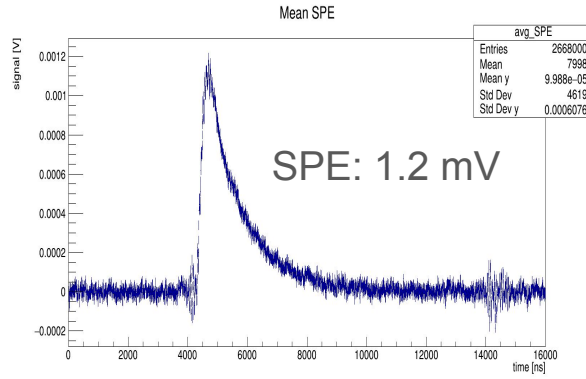
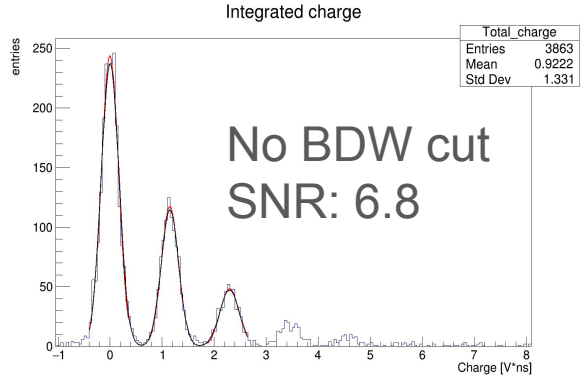
4x flex in ch1, test DCDC,  
V\_bias= 5.3V,  
I=60 mA,  
DCDC out=47.0V,  
LDO\_DCDC= 5.02V,  
LDO\_OpAmp=5.00V,  
Offset Ch1=135 mV  
Offset Ch2=117 mV

# DCEM #1, Ch1





# DCEM #1, Ch2



# DCEM #2, CMOS, HPK, DCDC\_test

## DCEM #2

### Room T

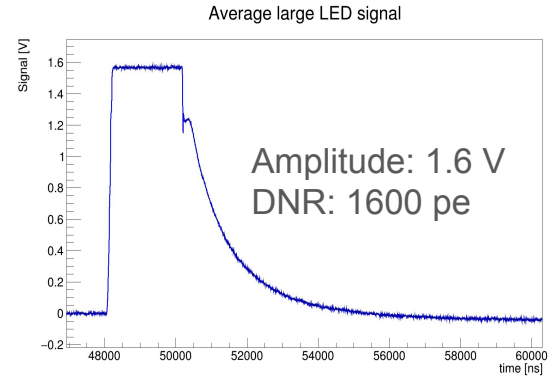
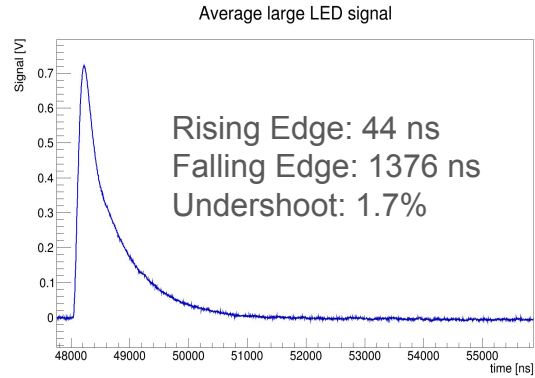
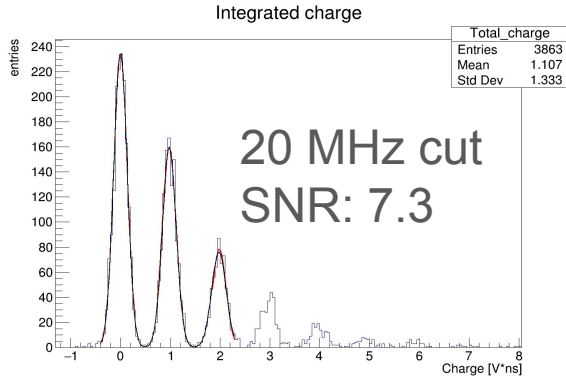
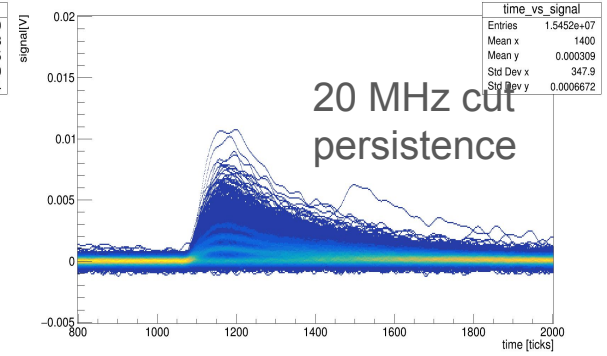
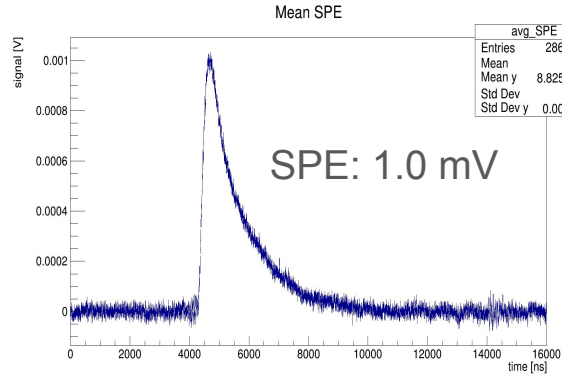
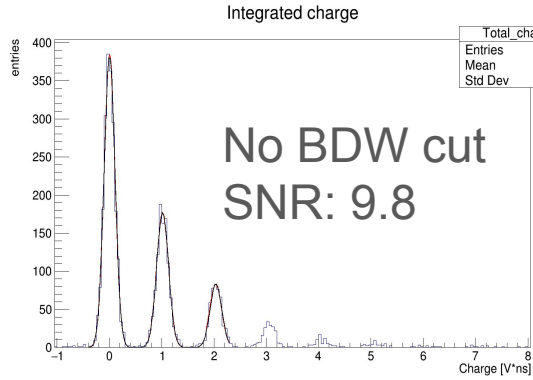
No flex, test DCDC,  
V\_bias= 5.3V,  
I=124 mA,  
DCDC out=56.4V,  
LDO\_DCDC= 4.98V,  
LDO\_OpAmp=4.99V,  
Offset Ch1=187 mV  
Offset Ch2=181 mV

## DCEM #2

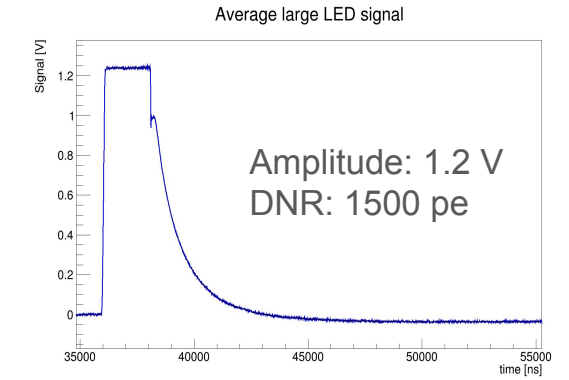
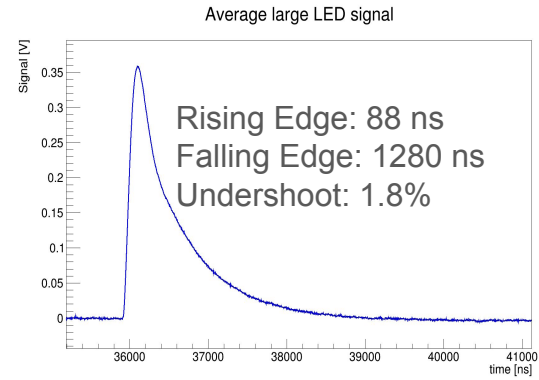
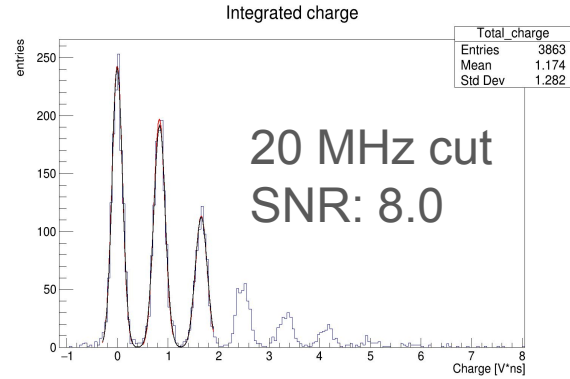
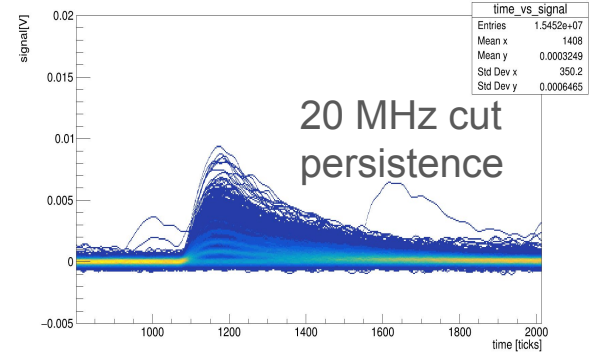
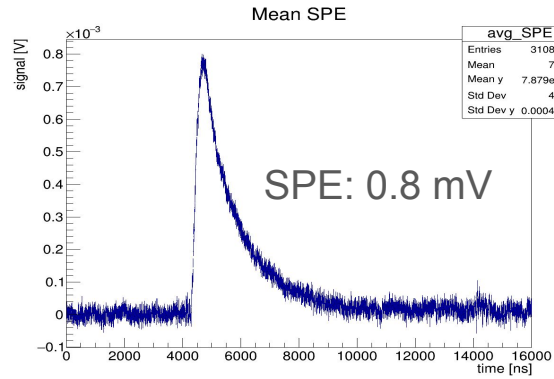
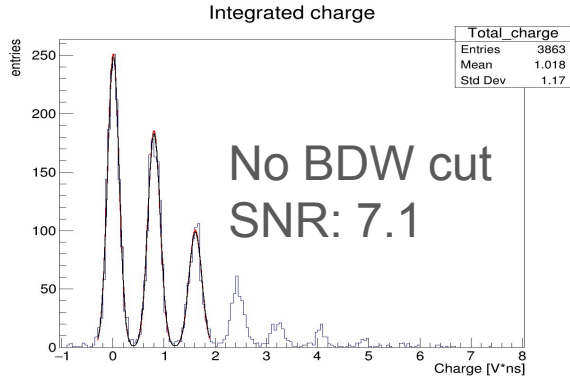
### LAr

4x flex in ch1, test DCDC,  
V\_bias= 5.3V,  
I=60 mA,  
DCDC out=47.0V,  
LDO\_DCDC= 5.03V,  
LDO\_OpAmp=5.00V,  
Offset Ch1=97 mV  
Offset Ch2=87 mV

# DCEM #2, Ch1



# DCEM #2, Ch2



# DCEM #3, CMOS, HPK, own\_DCDC

## DCEM #3

### Room T

No flex, own DCDC,  
V\_bias= 5.3V,  
I=126 mA,  
DCDC out=56.4V,  
LDO\_DCDC= 4.98V,  
LDO\_OpAmp=5.00V,  
Offset Ch1=205 mV  
Offset Ch2=184 mV

## DCEM #3

### LAr

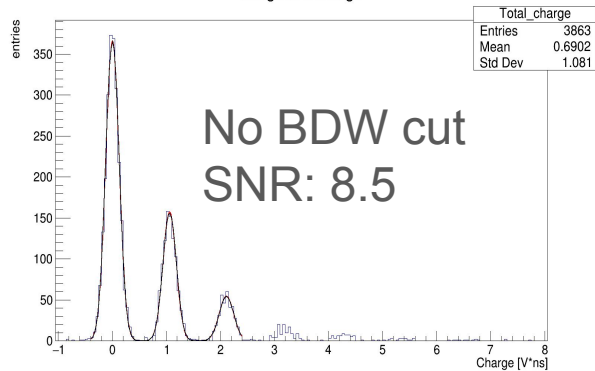
4x flex in ch1, own DCDC,  
V\_bias= 5.3V,  
I=60 mA,  
DCDC out=47.0V,  
LDO\_DCDC= 4.93V,  
LDO\_OpAmp=4.95V,  
Offset Ch1=125 mV  
Offset Ch2=83 mV

DCEM #3 Ch2  
shows a  
baseline slow  
oscillation (5us).

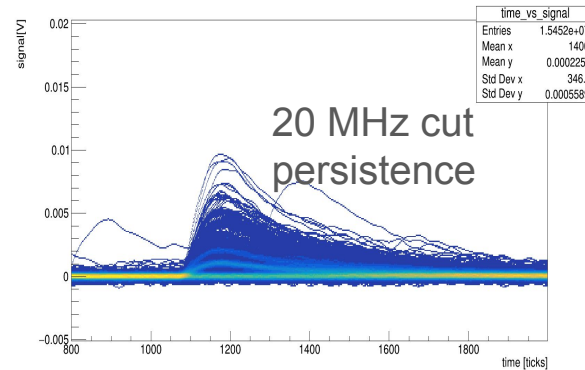
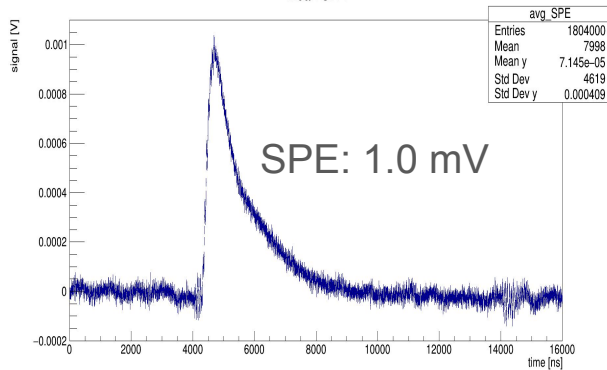
Laser daughter  
card ground pin  
was not well  
soldered. 2nd  
run of data taken  
after fixing it.

# DCEM #3, Ch1

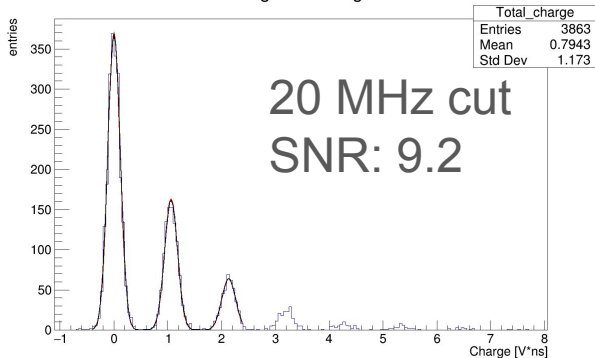
Integrated charge



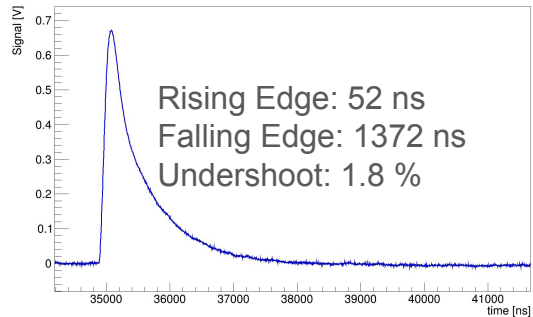
Mean SPE



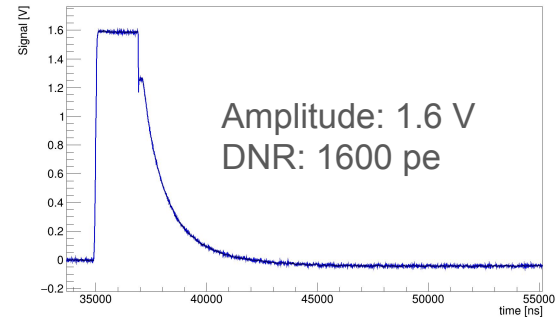
Integrated charge



Average large LED signal

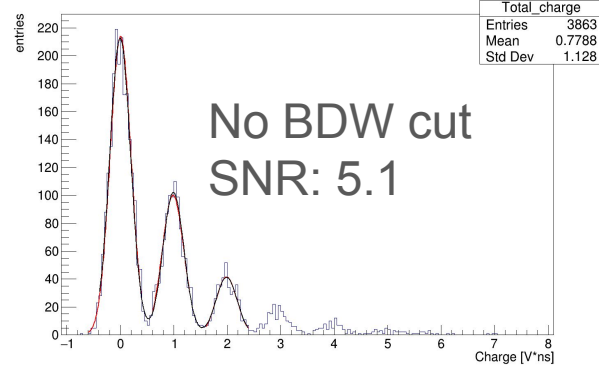


Average large LED signal

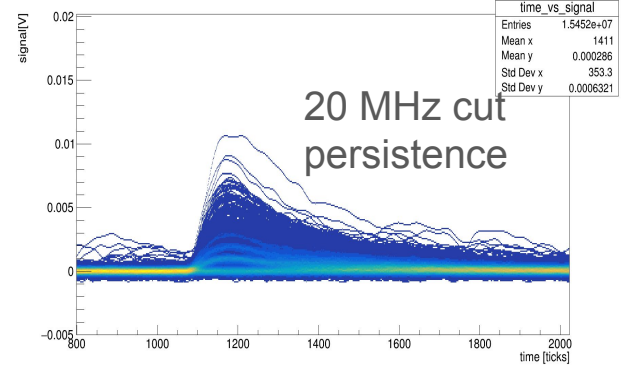
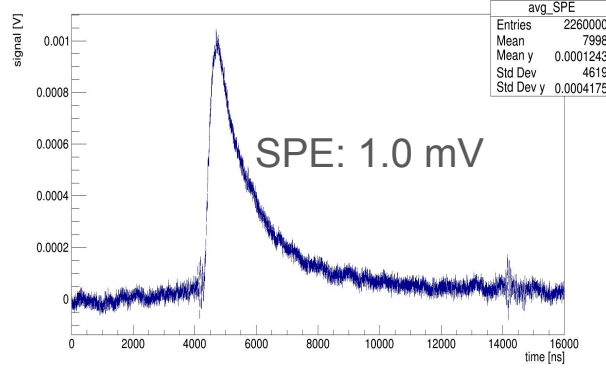


# DCEM #3, Ch2 (bad soldering pin)

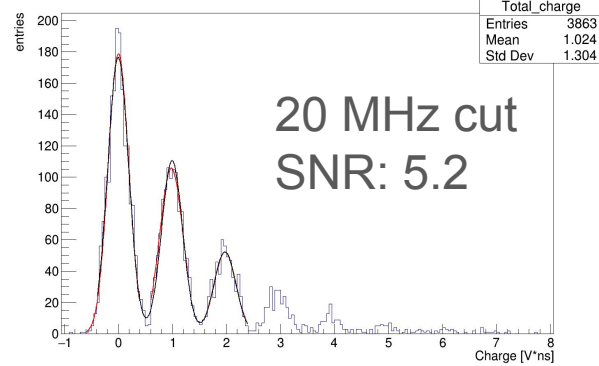
Integrated charge



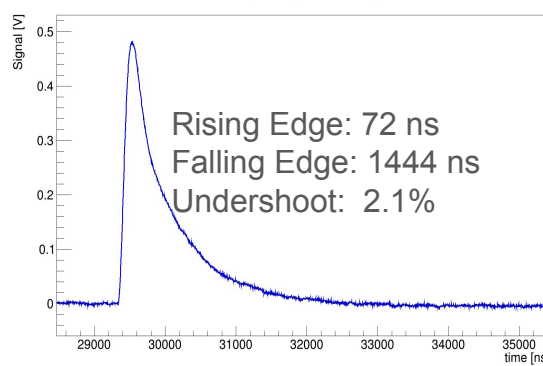
Mean SPE



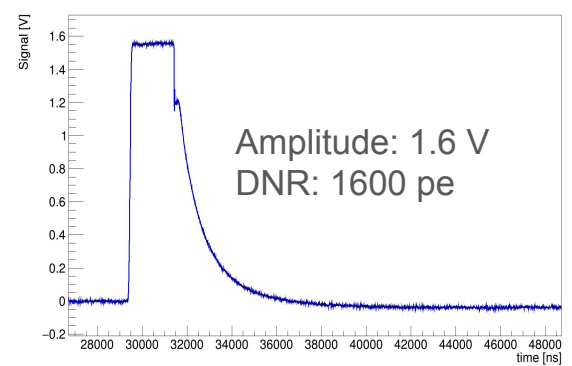
Integrated charge



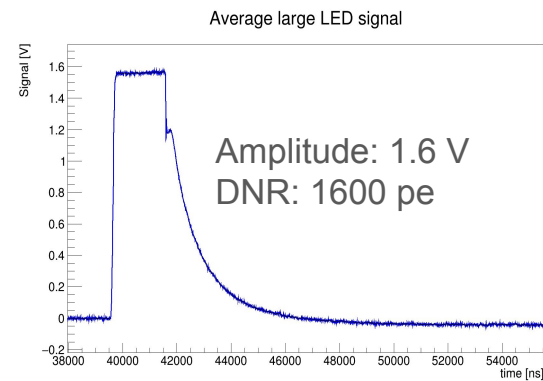
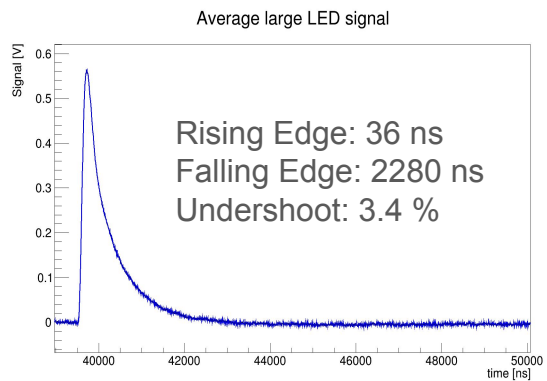
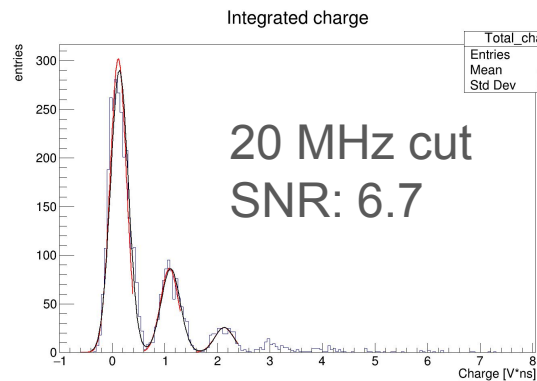
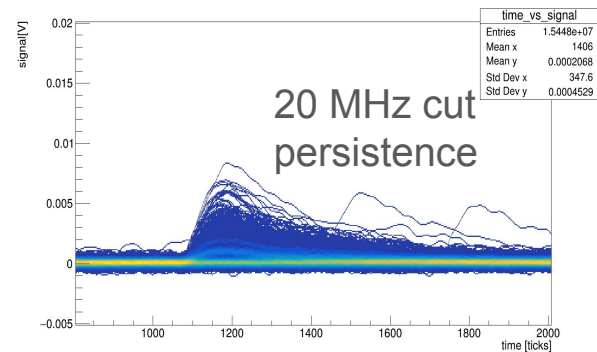
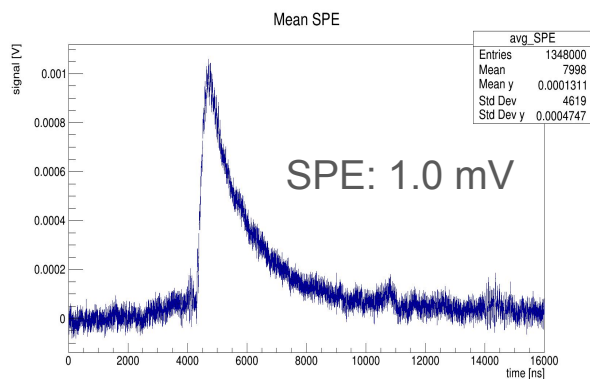
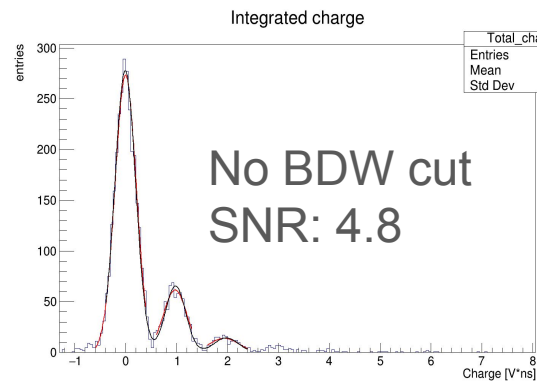
Average large LED signal



Average large LED signal



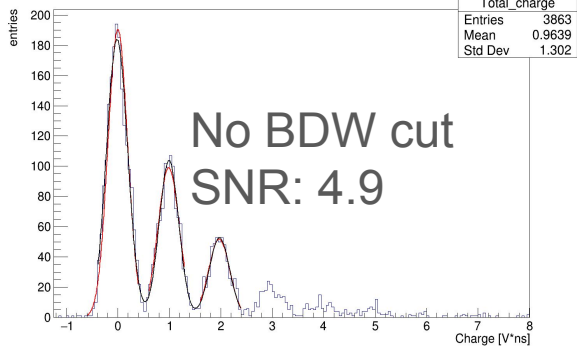
# DCEM #3, Ch2\_b (after pin fixed)



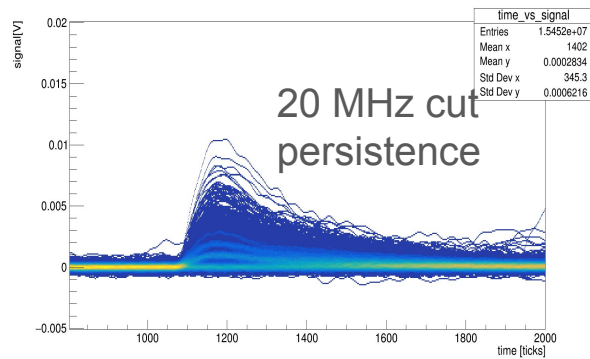
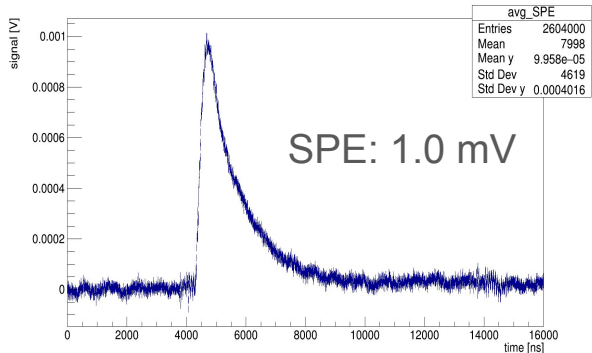


# DCEM #3, Ch2\_c

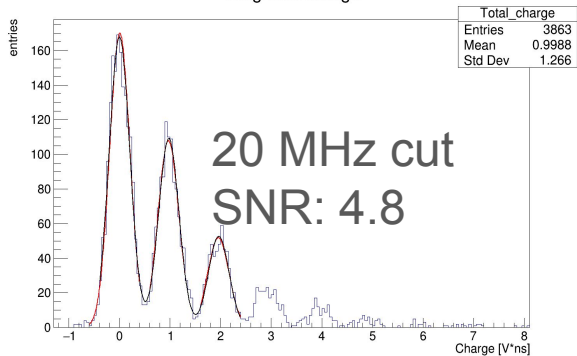
Integrated charge



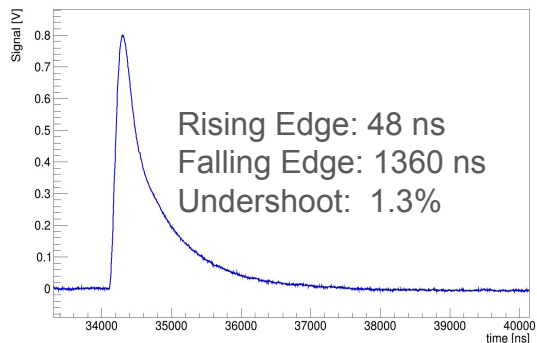
Mean SPE



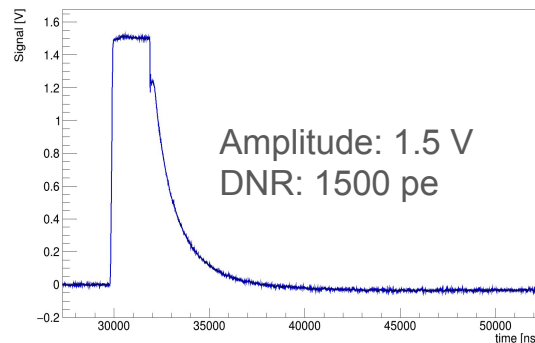
Integrated charge



Average large LED signal



Average large LED signal



# DCEM #4, CMOS, HPK, own\_DCDC

## DCEM #4

### Room T

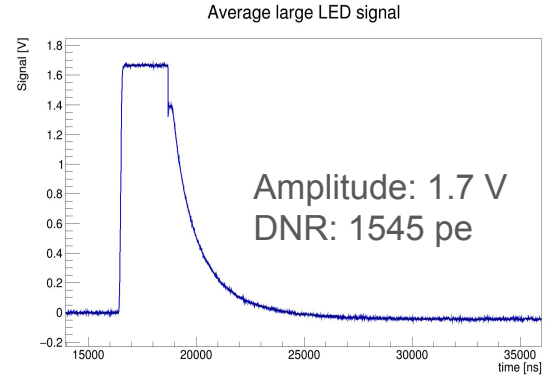
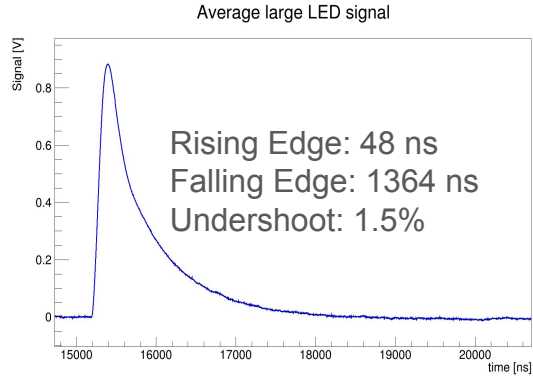
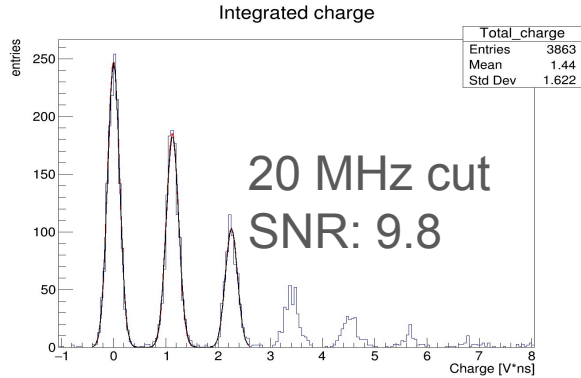
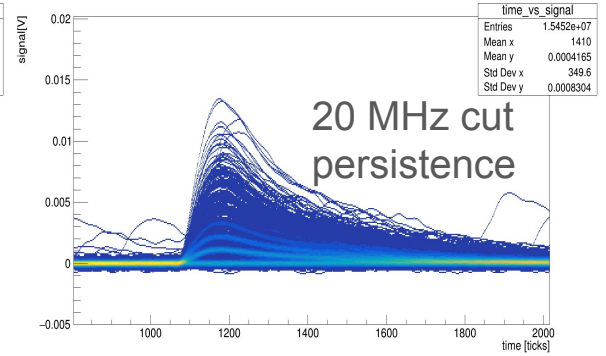
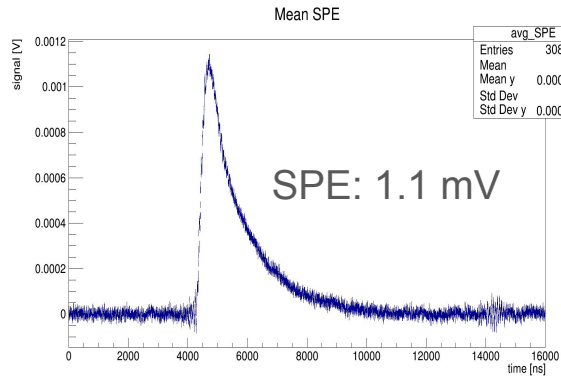
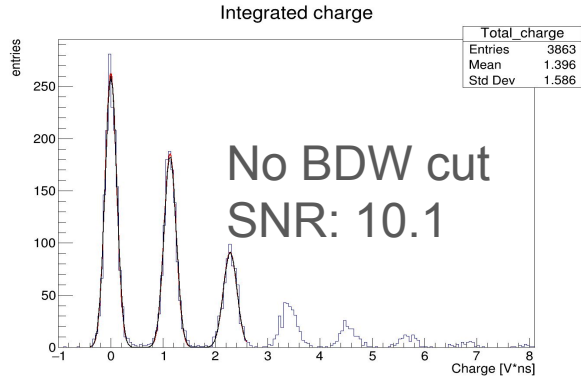
No flex, own DCDC,  
V\_bias= 5.3V,  
I=126 mA,  
DCDC out=56.4V,  
LDO\_DCDC= 5.00V,  
LDO\_OpAmp=4.98V,  
Offset Ch1=204 mV  
Offset Ch2=154 mV

## DCEM #4

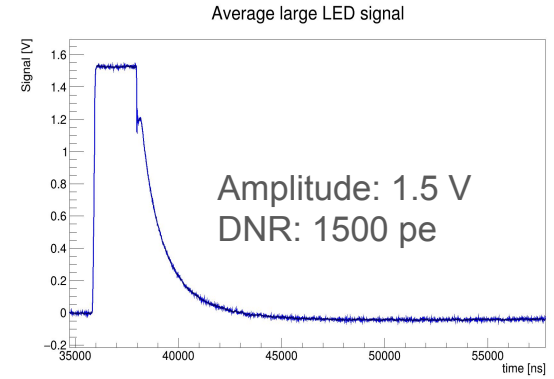
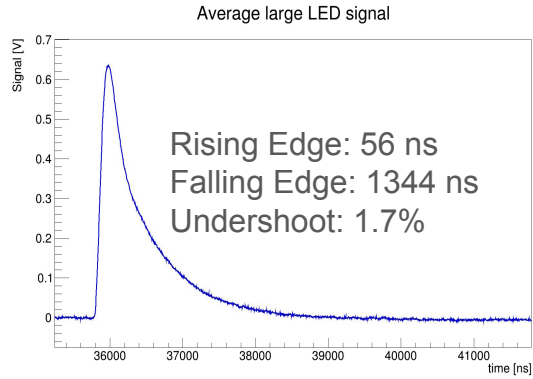
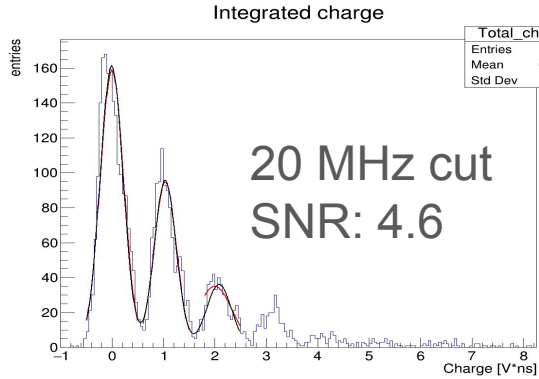
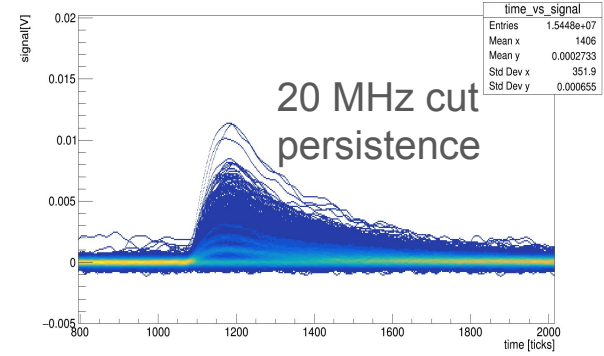
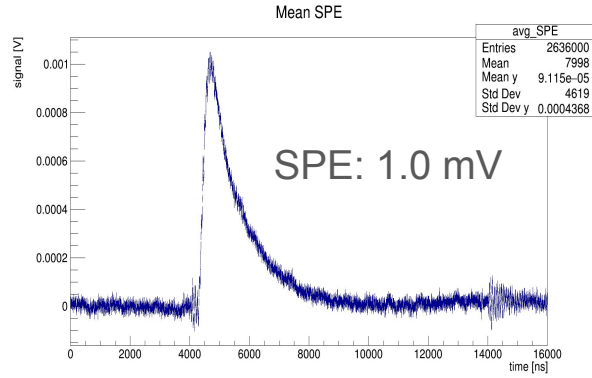
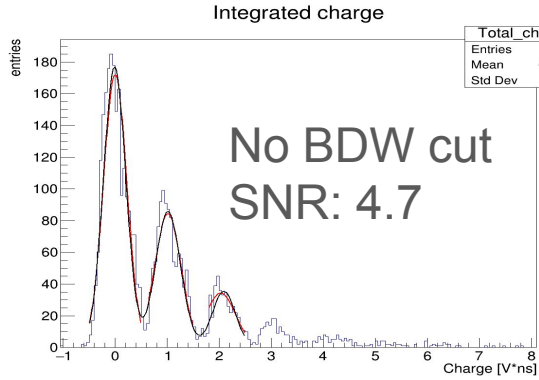
### LAr

4x flex in ch1, own DCDC,  
V\_bias= 5.3V,  
I=60 mA,  
DCDC out=47.1V,  
LDO\_DCDC= 5.01V,  
LDO\_OpAmp=4.92V,  
Offset Ch1=115 mV  
Offset Ch2=90 mV

# DCEM #4, Ch1 b



# DCEM #4, Ch2



# DCEM #5, BiPolar, HPK, DCDC\_test

## DCEM #5

### Room T

No flex, test DCDC,  
V\_bias= 5.3V,  
I=104 mA,  
DCDC out=56.4V,  
LDO\_DCDC= 4.99V,  
LDO\_OpAmp=4.99V,  
Offset Ch1=46 mV  
Offset Ch2=56 mV

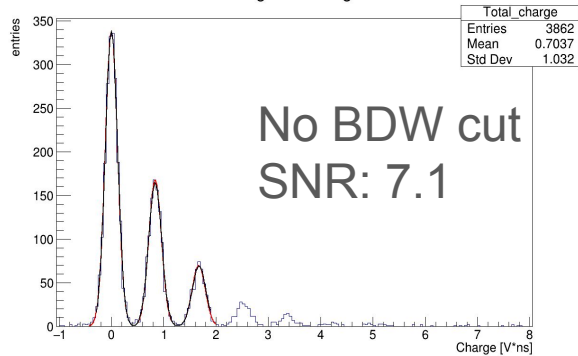
## DCEM #5

### LAr

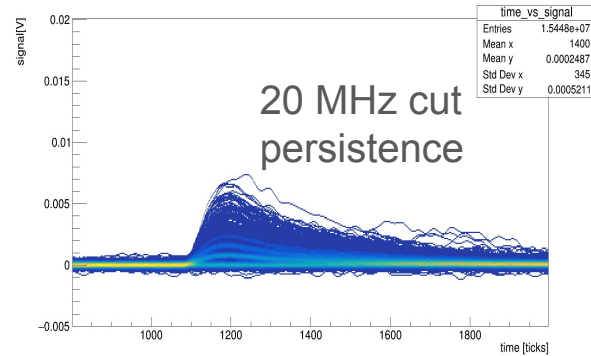
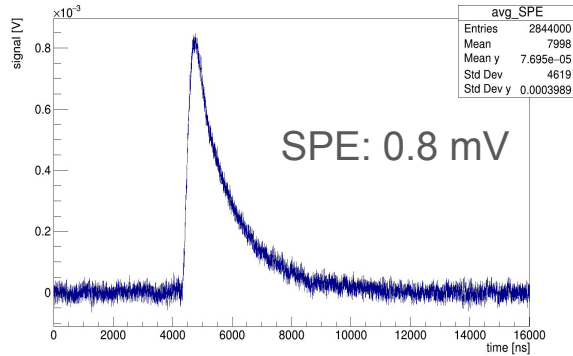
4x flex in ch1, test DCDC,  
V\_bias= 5.3V,  
I=54 mA,  
DCDC out=47.0V,  
LDO\_DCDC= 5.00V,  
LDO\_OpAmp=4.97V,  
Offset Ch1=81 mV  
Offset Ch2=74 mV

# DCEM #5, Ch1

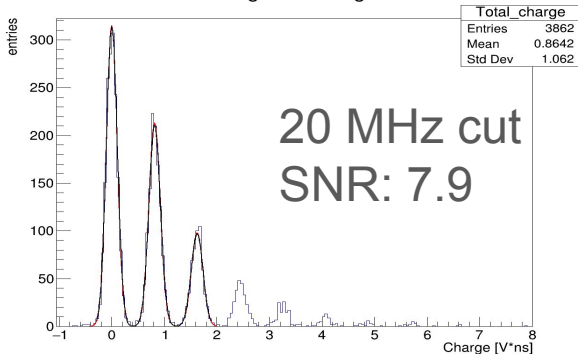
Integrated charge



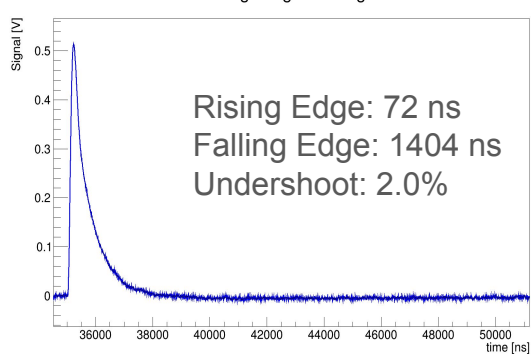
Mean SPE



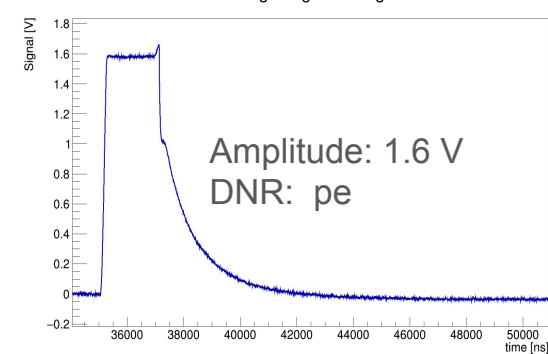
Integrated charge



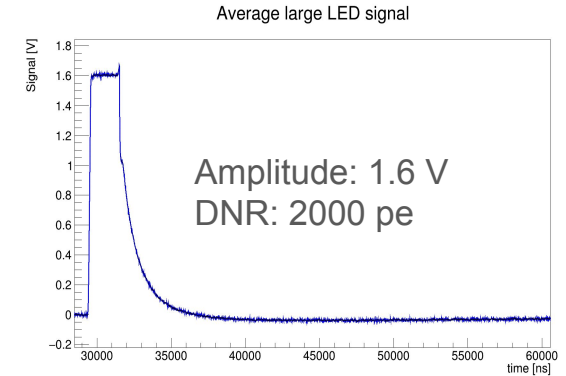
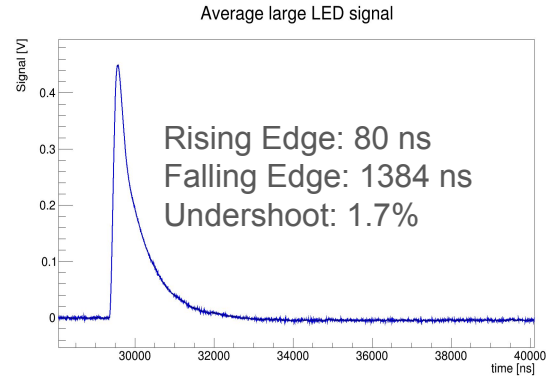
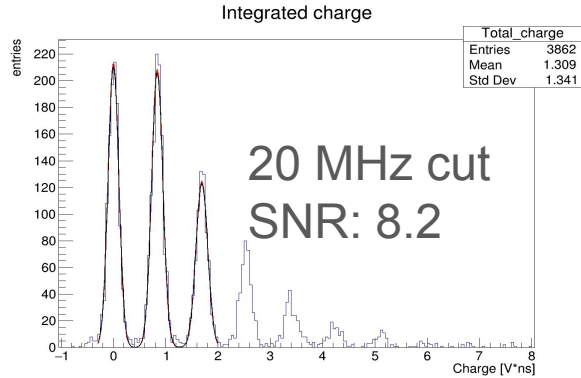
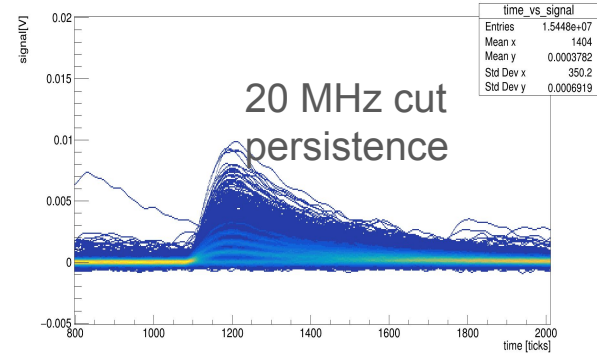
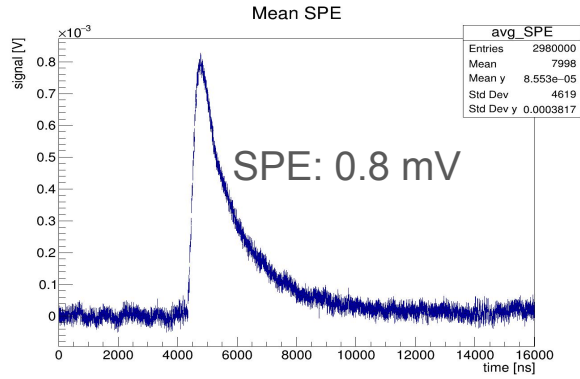
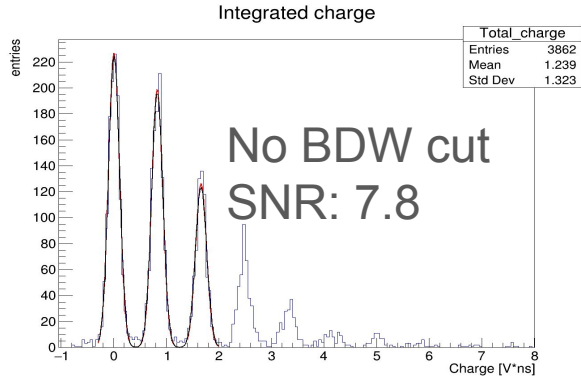
Average large LED signal



Average large LED signal



# DCEM #5, Ch2



# DCEM #6, BiPolar, HPK, DCDC\_test

## DCEM #6

### Room T

No flex, test DCDC,  
V\_bias= 5.3V,  
I=105 mA,  
DCDC out=56.3V,  
LDO\_DCDC= 4.99V,  
LDO\_OpAmp=4.98V,  
Offset Ch1=48 mV  
Offset Ch2=45 mV

## DCEM #6

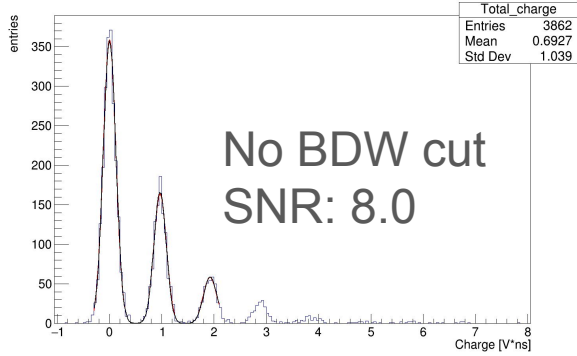
### LAr

4x flex in ch1, test DCDC,  
V\_bias= 5.3V,  
I=55 mA,  
DCDC out=47.0V,  
LDO\_DCDC= 4.98V,  
LDO\_OpAmp=5.02V,  
Offset Ch1=103 mV  
Offset Ch2= 104 mV

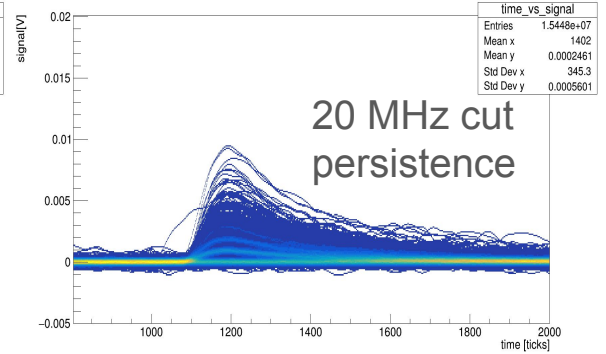
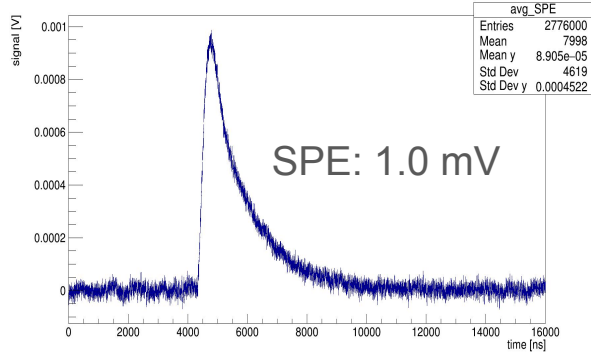


# DCEM #6, Ch1

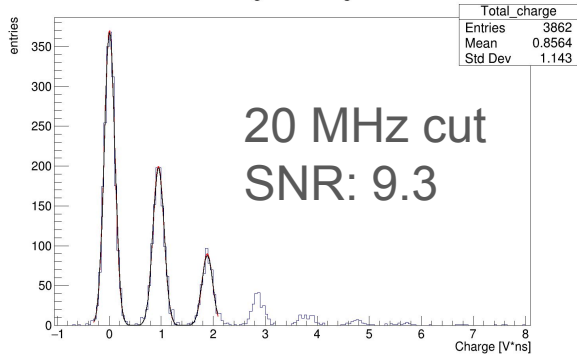
Integrated charge



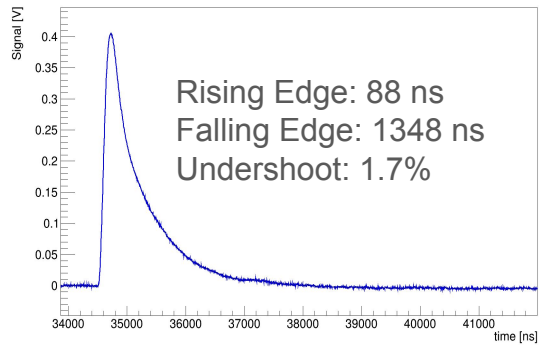
Mean SPE



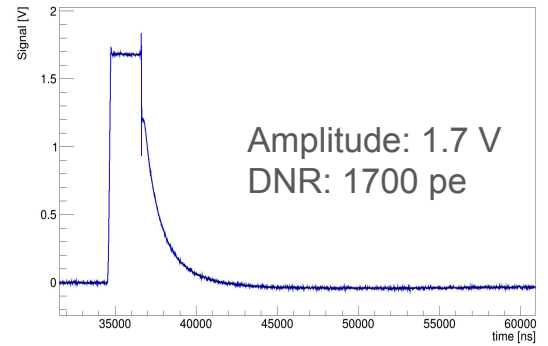
Integrated charge



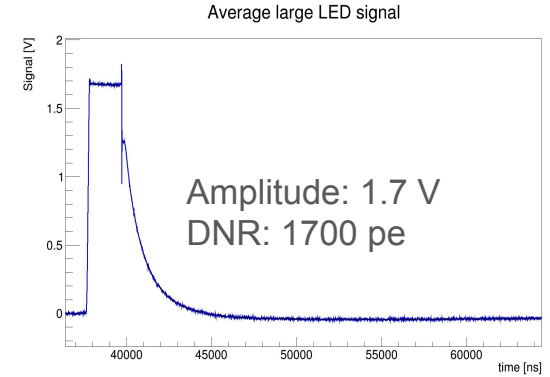
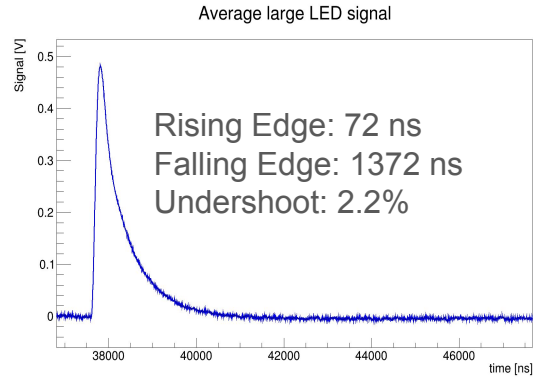
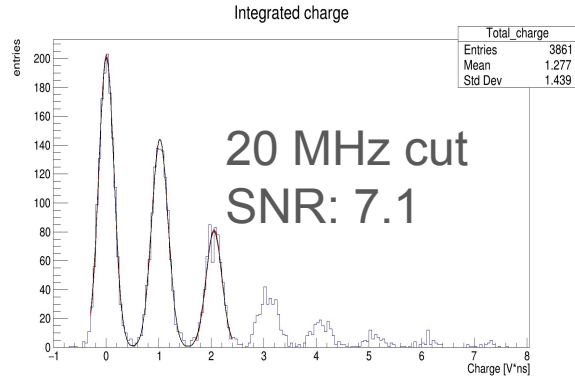
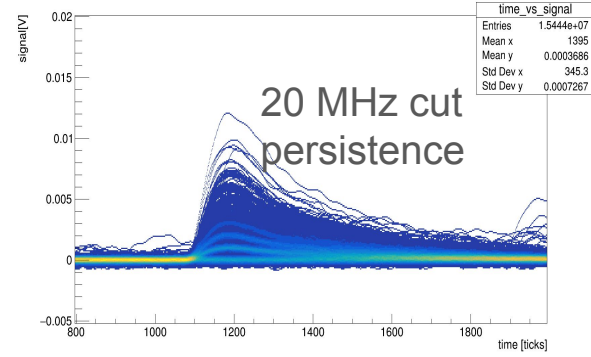
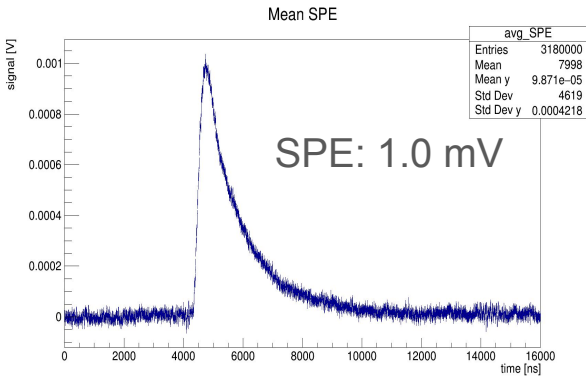
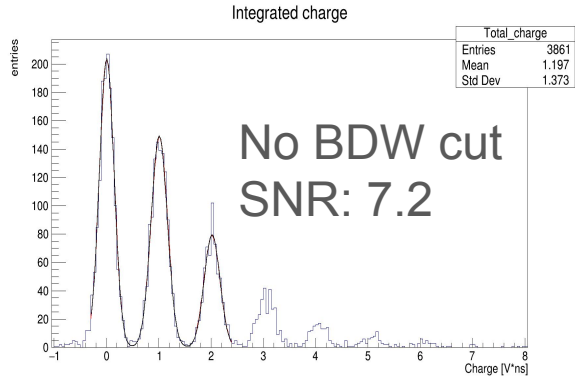
Average large LED signal



Average large LED signal



# DCEM #6, Ch2



# DCEM #7, BiPolar, HPK, DCDC\_test

## DCEM #7

### Room T

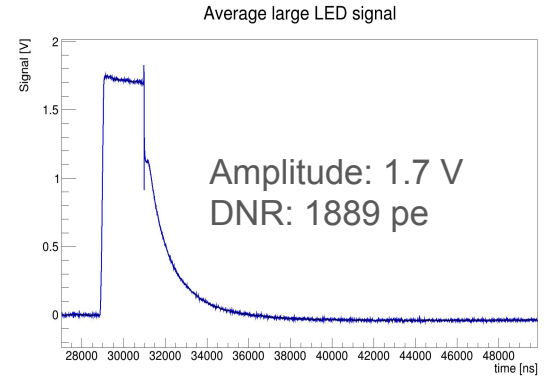
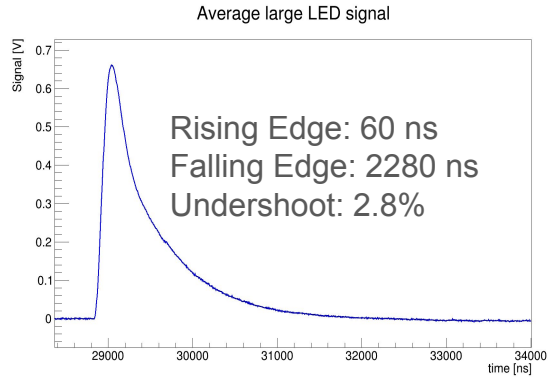
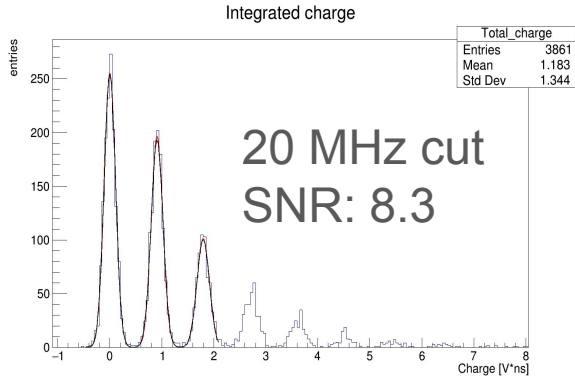
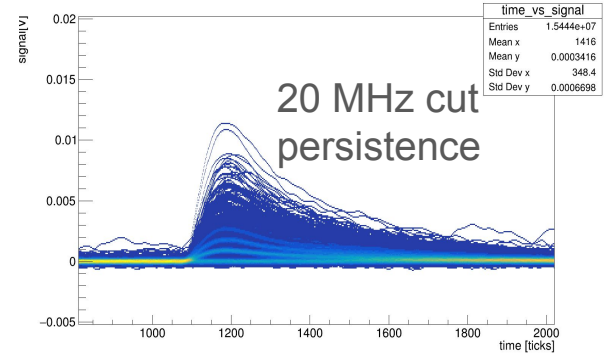
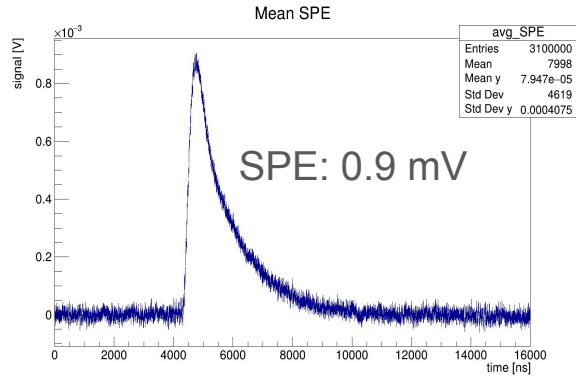
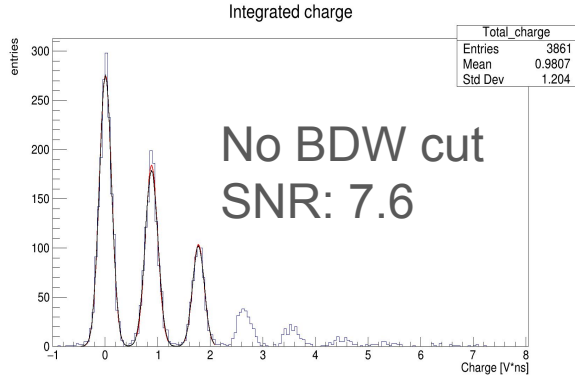
No flex, test DCDC,  
V\_bias= 5.3V,  
I=104 mA,  
DCDC out=56.5V,  
LDO\_DCDC= 4.98V,  
LDO\_OpAmp=4.99V,  
Offset Ch1=37 mV  
Offset Ch2=37 mV

## DCEM #7

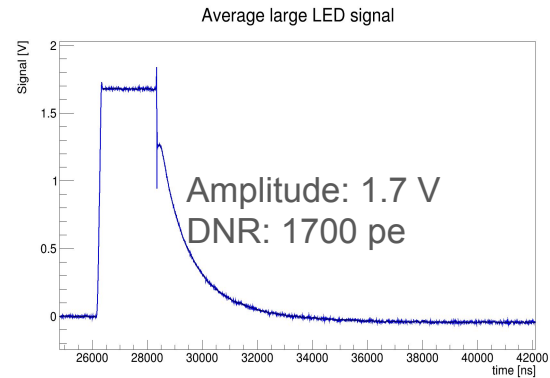
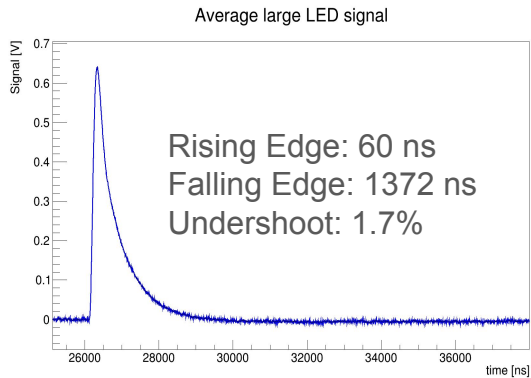
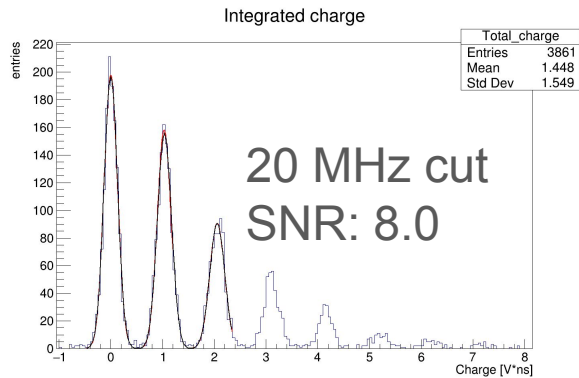
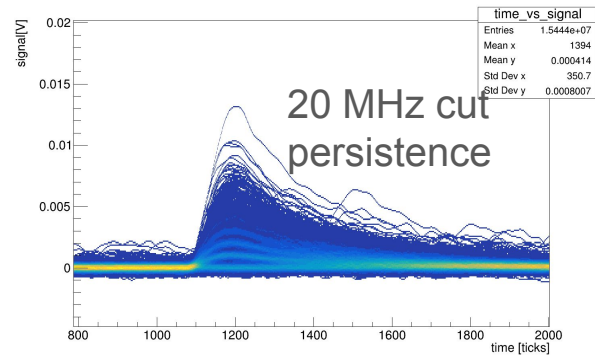
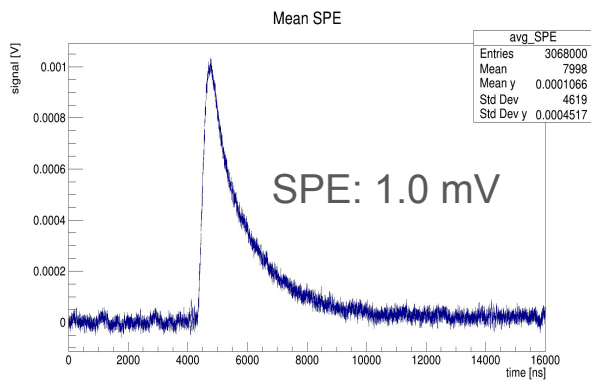
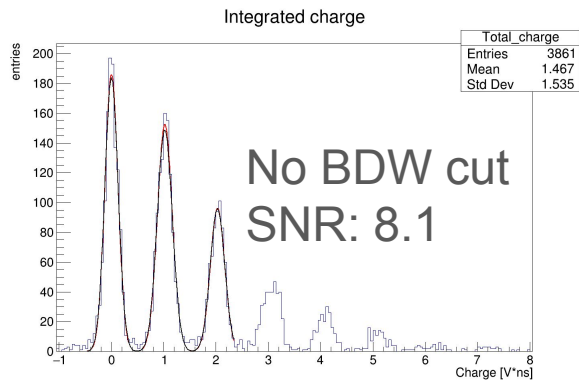
### LAr

4x flex in ch1, test DCDC,  
V\_bias= 5.3V,  
I=55 mA,  
DCDC out=47.0V,  
LDO\_DCDC= 5.01V,  
LDO\_OpAmp=5.01V,  
Offset Ch1=90 mV  
Offset Ch2= 102 mV

# DCEM #7, Ch1



# DCEM #7, Ch2



# DCEM #8, BiPolar, HPK, DCDC\_test

## DCEM #8

### Room T

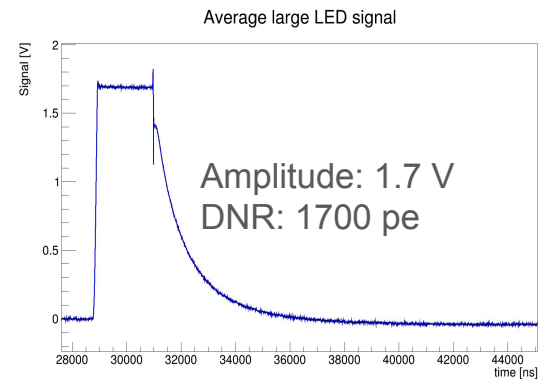
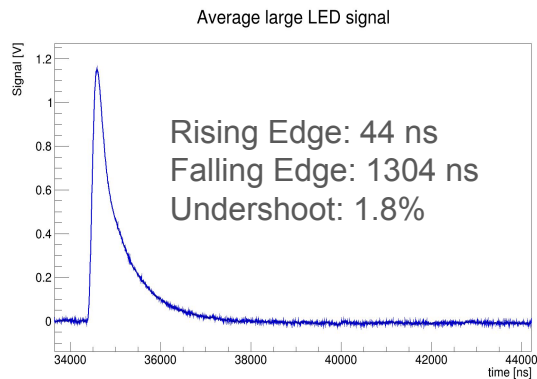
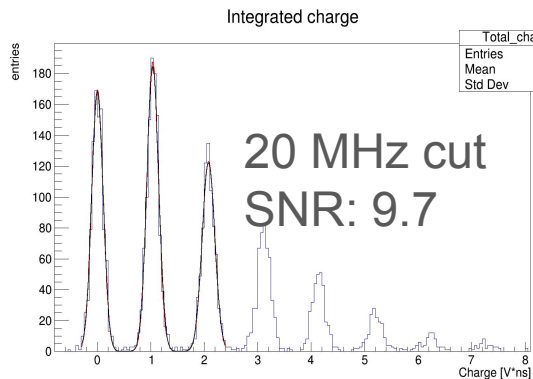
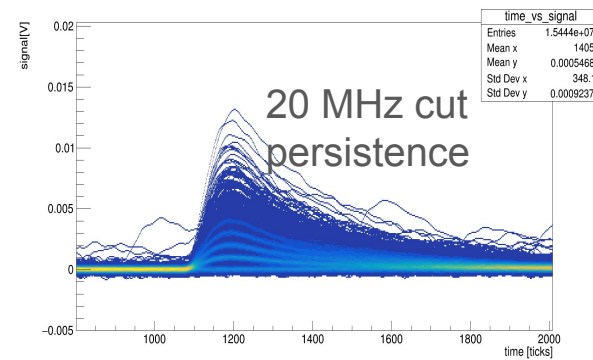
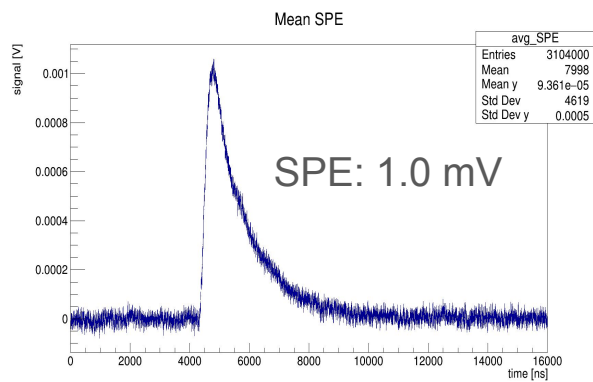
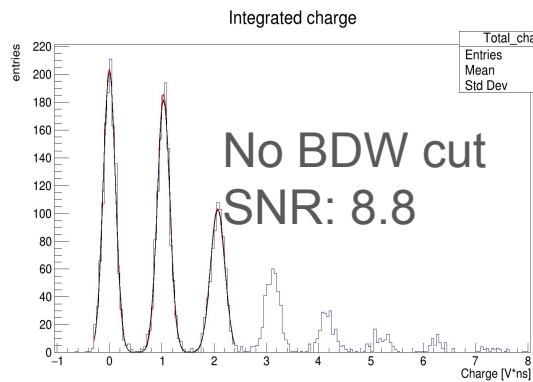
No flex, test DCDC,  
V\_bias= 5.3V,  
I=105 mA,  
DCDC out=56.4V,  
LDO\_DCDC= 4.98V,  
LDO\_OpAmp=5.00V,  
Offset Ch1=45 mV  
Offset Ch2=47 mV

## DCEM #8

### LAr

4x flex in ch1, test DCDC,  
V\_bias= 5.3V,  
I=54 mA,  
DCDC out=47.0V,  
LDO\_DCDC= 5.01V,  
LDO\_OpAmp=5.02V,  
Offset Ch1=97 mV  
Offset Ch2=103 mV

# DCEM #8, Ch1



# DCEM #8, Ch2

