Low Level RF Control System

Brian Chase Project X Machine Advisory Committee March 18-19, 2013







• Low Level RF

- Goals and associated scope of work
- Progress to date with existing designs
- Primary technical challenges



LLRF Goals and Scope



Goals

- Meet all functional and longitudinal beam dynamic requirements through RF cavity field, resonance and Beam Chopper pattern control
- Scope
 - Master Oscillator and multiple phase reference lines
 - LLRF field and resonance control for all accelerating cavities and deflecting cavities
 - LEBT and MEBT Chopper Program Module
 - Interface with Timing Machine Protection, Instrumentation and Controls
 - Diagnostic and control software
 - Start up and fault recovery
 - Slow tuner control
 - Beam-based calibration



Power and Control Requirements (10% control overhead,10% loss)



Section	Freq (MHz)	Microphonic amplitude (peak Hz)	Minimal half bandwidth (Hz)	Max loaded Qext	Max Required power (kW)	Regulation (Short term RMS)	Quantity cav/cryomod
RFQ	162.5	-	-	-	79	0.2% 0.2 deg	1
Buncher	162.5	-	17,000	9.5e3	1.5	0.2% 0.2 deg	3
HWR	162.5	20	24	3.4e6	4.9	0.2% 0.2 deg	8/1
SSR1	325	20	27	5.8e6	5.5	0.2% 0.2 deg	16/2
SSR2	325	20	23	7.2e6	17	0.2% 0.2 deg	35/7
LB 650	650	20	23	1.4e7	34	0.2% 0.2 deg	30/5
HB1 650	650	20	23	1.4e7	50	0.2% 0.2 deg	42/7
HB2 650	650	20	23	1.4e7	31	0.2% 0.2 deg	120/15
9-cell 1300	1300	30	65	1e7	50	0.2% 0.2 deg	224/28
Splitting	243.75	-	21,500	11.3e3	4	0.2% 0.2 deg	1



PIXIE RF Stations Diagram







RF Reference and Clock Generation



- 81.25 MHz is the beam
- fundamental after the RF splitter
- 101.5 kHz is a suggested fundamental frequency for the chopper
- Pulsed operation is selected from the Chopper fundamental



Project X High Stability Reference Line









Control system interface diagram (NML)





NML CM1 LLRF Racks

Receivers and Up-converter

VXI CPU & 3 R3MFC Controllers

Master Oscillator







Controller Hardware



Technologies of

interest:

- -Multi-channel ADCs -Low Voltage Differential Signaling (LVDS) high speed serial connections
- -Differential IF signal
- paths
- -8 channel coax
- connectors
- -Shielded enclosure
- -Low cost per channel



Project X Ch Receiver and MFC



Multi-Channel Field Control Module





Harting IF Mini-coax

8 Channel Receiver





<u>Measured SNR for one channel</u> (<u>12bit ADC</u>): SNR@fs/2 = 112dB - 10log10(32k/2) = 70dB <u>Measured SNR for vector sum</u> (<u>8x12bit ADC</u>): SNR@fs/2 + 10log10(8) = 79dB The SNR -156dBc/Hz (0.0016% BW:1MHz) is expected.

NML CM1 Flattop Errors (no beam)



Project X





Compensation of mechanical vibrations induced by external mechanical noise sources (e.g. pumps, cranes, etc.).

The Piezo tuner actively damped vibrations induced by external sources. An IIR filter bank was used to isolate and reverse the phase of the particular spectral line. The phase reversed signal then fed back to the piezo tuner.



EFFICIENCY - WHY?



GMRR VG12-1



HIGH-EFFICIENCY PA





DSP + HIGH-EFFICIENCY RF PAs

- Max efficiency for given amplitude
- Phase errors corrected
- Control and monitoring



Project X Primary technical challenges

- Project X is not a simple CW accelerator
 - 100% beam current modulation including gaps of 1ms
 - Cavities have the Qs of CW machines along with some of the complexity of pulsed machines
 - Real-time beam based feedforward compensation
- Fast turn on and trip recovery require:
 - Self Excited Loop and Generator Driven Resonator loop integration
 - Resonance control integration
- Resonance control of new cavities designs
- Beamed based calibration of cavity fields
- Development of the LEBT/MEBT Chopper Program Module
 - Wideband beam-based learning algorithm





6U CPCIe based 25 channel Digital board

India

CPCIe-DB25:

Tentative specifications

- Interface & size: CPCI, 6U (233 x 160mm)
- 24 14 bit, 80MSPS ADC input channels (LTM9009-14, Octal ADCs)
- 1 14 bit, 105MSPS ADC (ADS6144)
- 8 14 bit, 260MSPS DAC channels (Texas DAC5672, Dual DAC)
- 2 10 bit, 80MSPS Dual DAC (MAX5853)
- 2 5 differential output clock generator (Texas CDCE62005)
- Analog Devices (Sharc ADSP21369)
- SDRAM for data storage
- CPCIe (features under consideration)

Applications : Suitable for control of 8 NC/SC RF cavities **Status:** Design in progress