



# GRAIN ASIC Specs and Project Timeline

GRAIN Detector INFN Group Meeting  
May 27th, 2024

**Stefano Durando**

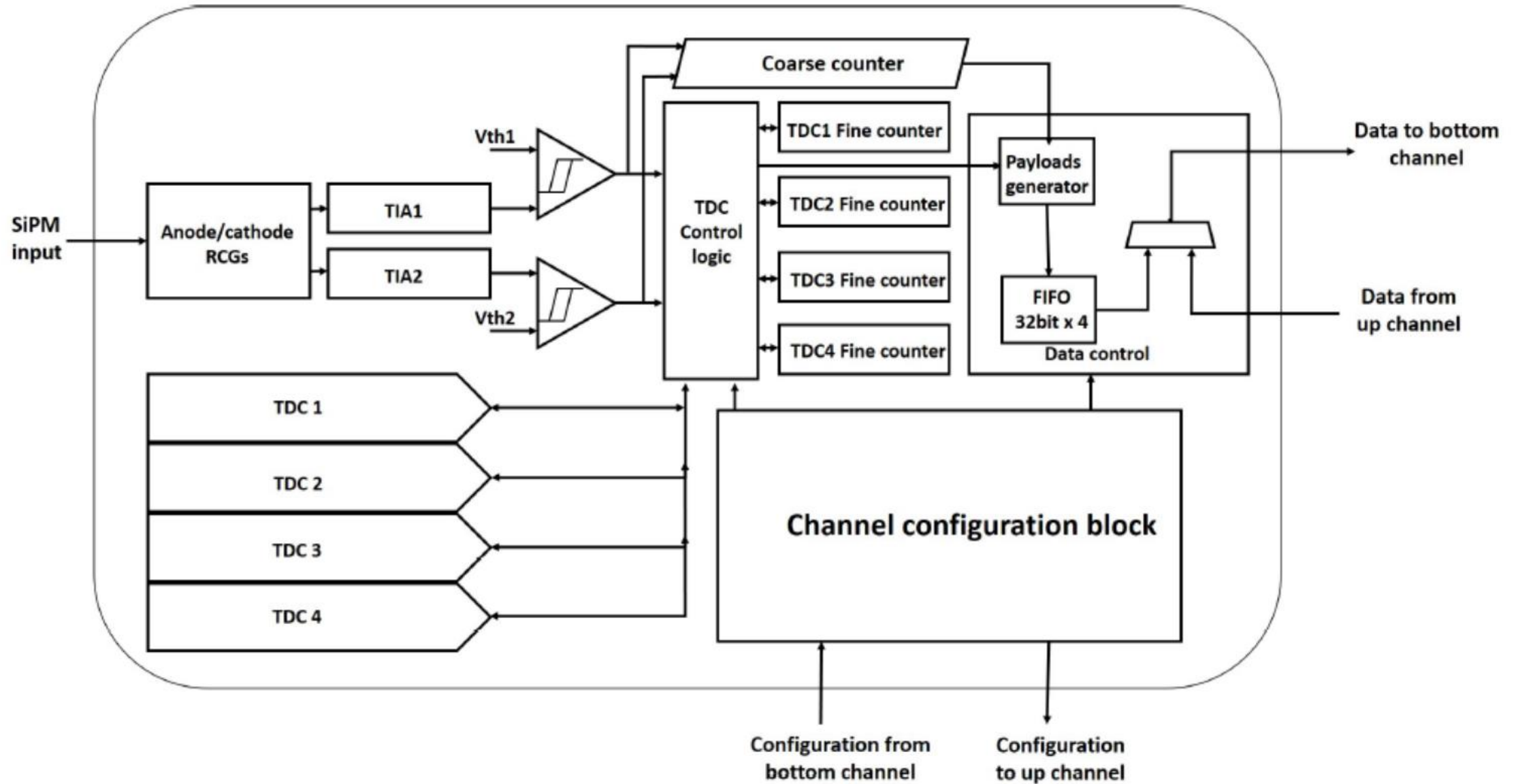
Sofia Blua, Valerio Pagliarino, Angelo Rivetti

# Specs Recap:

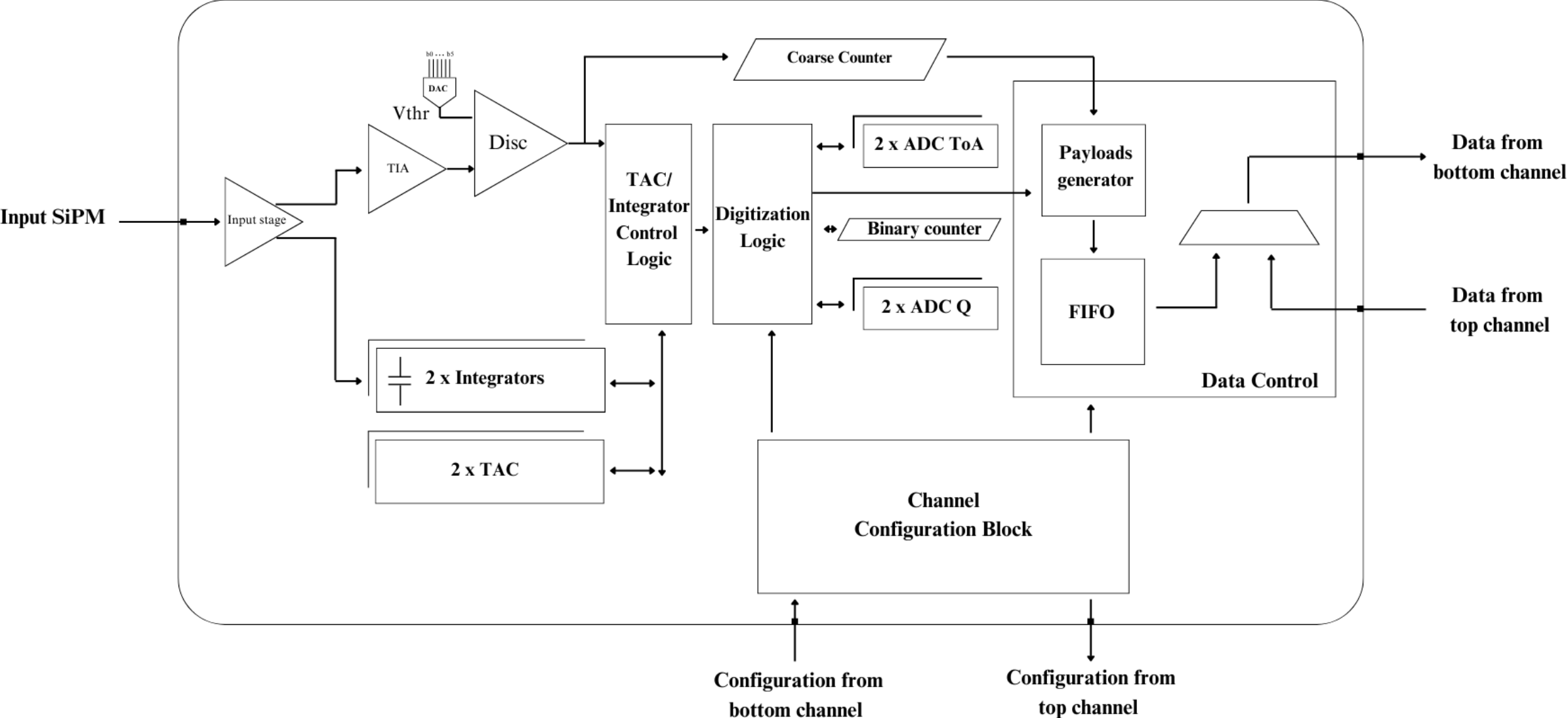
Parameter	Value
SiPM Size	2 mm x 2 mm (140 pF) 3 mm x 3 mm (500 pF)
# Channels/ASIC	1024
Operating Temperatures	300 K – 77 K
<Power Consumption>	5 W / ?
Max Chip Area	20x30mm <sup>2</sup>
Duty Cycle	1/1000: 9,6 $\mu$ s detection (50 $\mu$ s) < 0.1 s interspill
Measurements:	Q – ToA - ToT
Integrator Dynamic Range	100 PE
RMS <sub>ToA</sub> (first PE)	100 $\div$ 150 ps / 1PE
RMS <sub>ToT</sub>	$\approx$ 3 ns
Threshold SNR	0.5 x 1PE 30



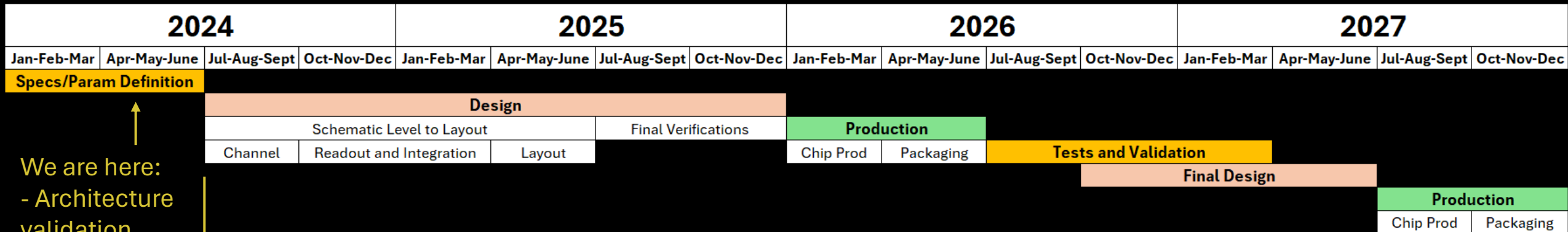
# ALCOR Pixel Scheme



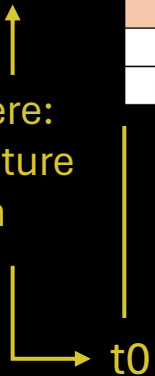
# GRAIN ASIC Pixel Scheme



# Demonstrator Submission: Dec 2025



We are here:  
- Architecture validation



t0