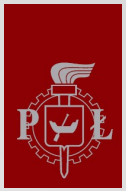

FW for main protection functionality and management

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About Us

Grzegorz Jabłoński

Ph.D. in Electrical Engineering

Role

RFPI project contractor

FPGA/software engineer

Hardware designer

Relevant experience

FLASH/XFEL LLRF Systems (2003-2012): HW/FW designer

ITER: FPGA/software engineer, system analyst (since 2010)

ESS-ERIC: FPGA/software engineer (since 2018)

Agenda

- RFPI management firmware
- RFPI main functionality firmware

RFPI management firmware

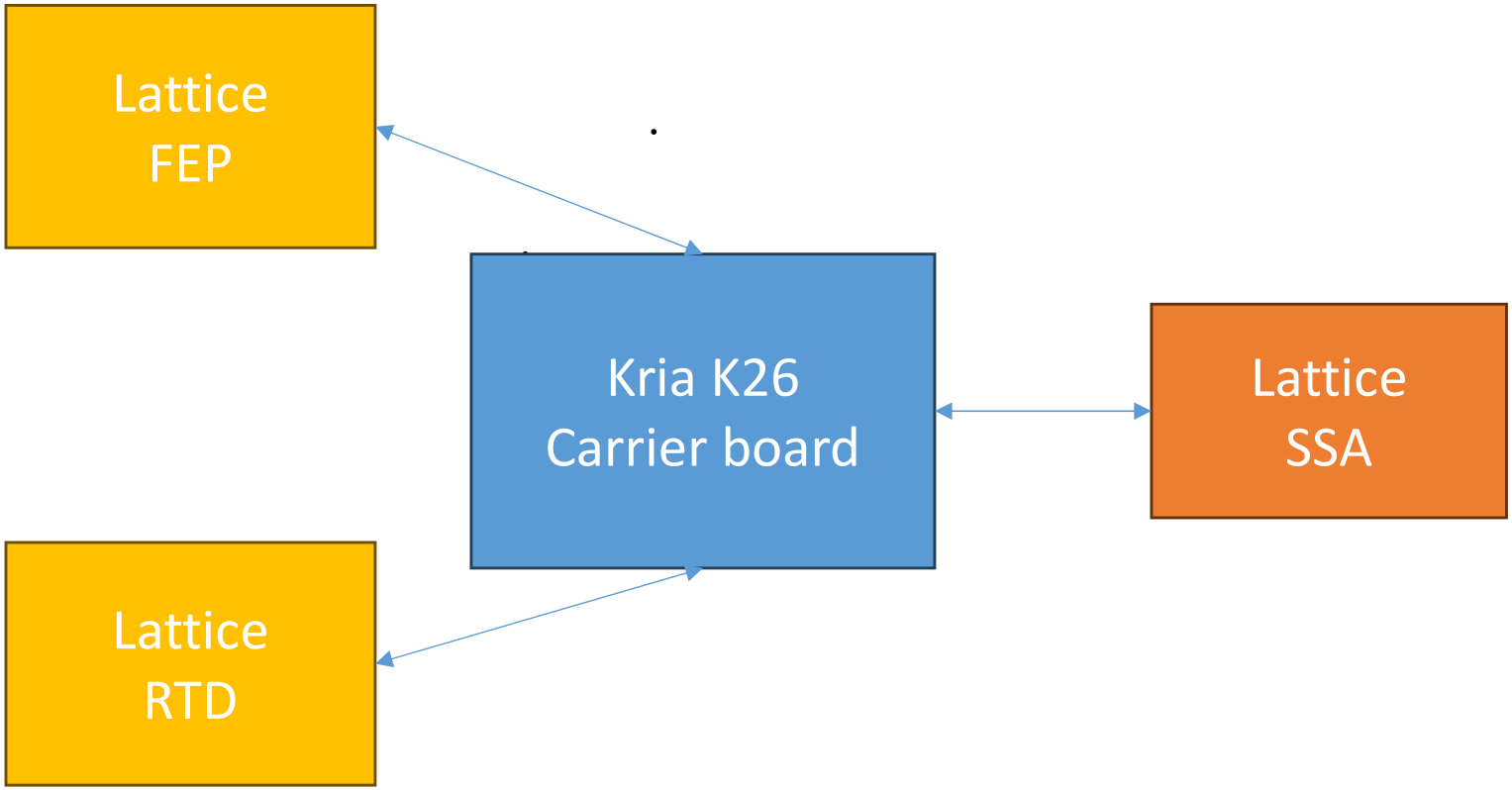
- The RFPI management processor is running under Linux operating system
  - Buildroot distribution supported by Microchip
- It has the following functions:
  - Management of power supply of individual system modules
    - Ensuring proper powerup and powerdown sequence
  - Monitoring voltages and current of individual system modules
  - Managing reset and boot mode of the Kria SOM
  - Allowing JTAG access to Kria SOM
    - Running Xilinx hw_manager under QEMU

RFPI management firmware

- The management processor is able to read and control individual digital signals by means of GPIO.
- It is also equipped with several I2C interfaces
  - To current and voltage monitoring integrated circuits
  - To Lattice FPGA serving as a JTAG multiplexer
- It is also equipped with the serial interface to Kria board.
- An EPICS IOC allowing external monitoring and control of the system is running on the management processor.

RFPI main functionality firmware

- The logic of the interlock system is divided into several FPGAs – main Zynq Ultrascale+ and several Lattice ICE40HX8K FPGAs on conditional boards.
- Lattice FPGAs on FEP and RTD boards are used only for configuration. Lattice FPGA on SSA board is a part of interlock logic.



RFPI main functionality firmware

- The main FPGA communicates with the Lattice FPGA using a simple serial protocol.
  - The protocol is register-based.
  - Main FPGA is an initiator of the transmission and sends a data packet consisting of and address, value and read/write flag.
  - The Lattice FPGA responds with a packet consisting of the value of a specific register (for the read operation) or the confirmation packet (for the write operation).
- Communication is protected by means of a CRC checksum.
- If the CRC of the response is not correct, or does not arrive within a set time limit, the main FPGA repeats the transmission.
- If the checksum of the request is not correct, Lattice sends back the error packet.

RFPI main functionality firmware

- Lattice FPGA on SSA board monitors “SSA ready” signal and sets four permit signals: “MPS permit”, “LLRF permit”, “SSA permit” and “SSA DC permit”.
- If wrong value of “SSA ready” signal or wrong state of any fuse is detected, the interrupt request is issued to the main FPGA.
  - The mask decides, which signals are taken into account
  - Main FPGA reads from Lattice the information about the detected event, decides which permits should be released and returns the command to release them to Lattice FPGA.
- External FPGA is used for SSA, because there are not enough signals available on the main FPGA.
- The signals from remaining conditioning boards are processed directly by the main FPGA.
- All the events are timestamped on main FPGA and Lattice FPGA.
- If an event triggers release of the permit signal, the order of events can be determined due to these timestamps.