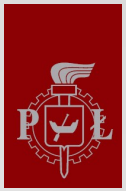


Quality Control

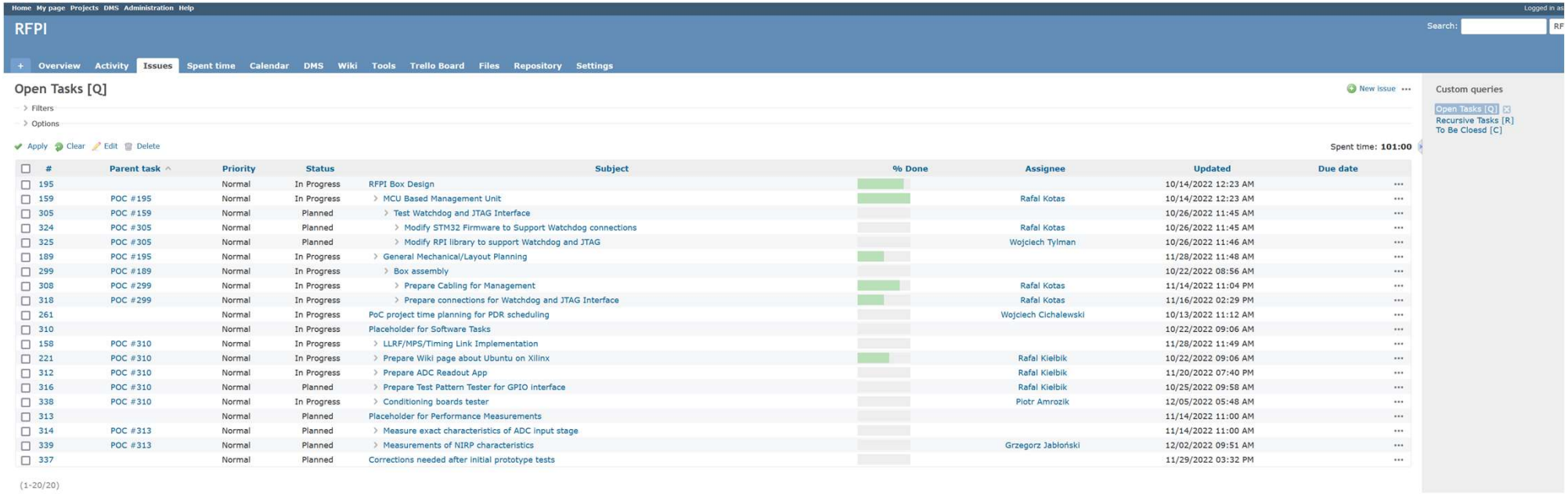
Wojciech Jałmużna

Agenda

- Project management and progress monitoring tool
- [Hardware] design workflow
- Data management
- [Hardware] Design documentation
- Summary

Project management and progress monitoring tool

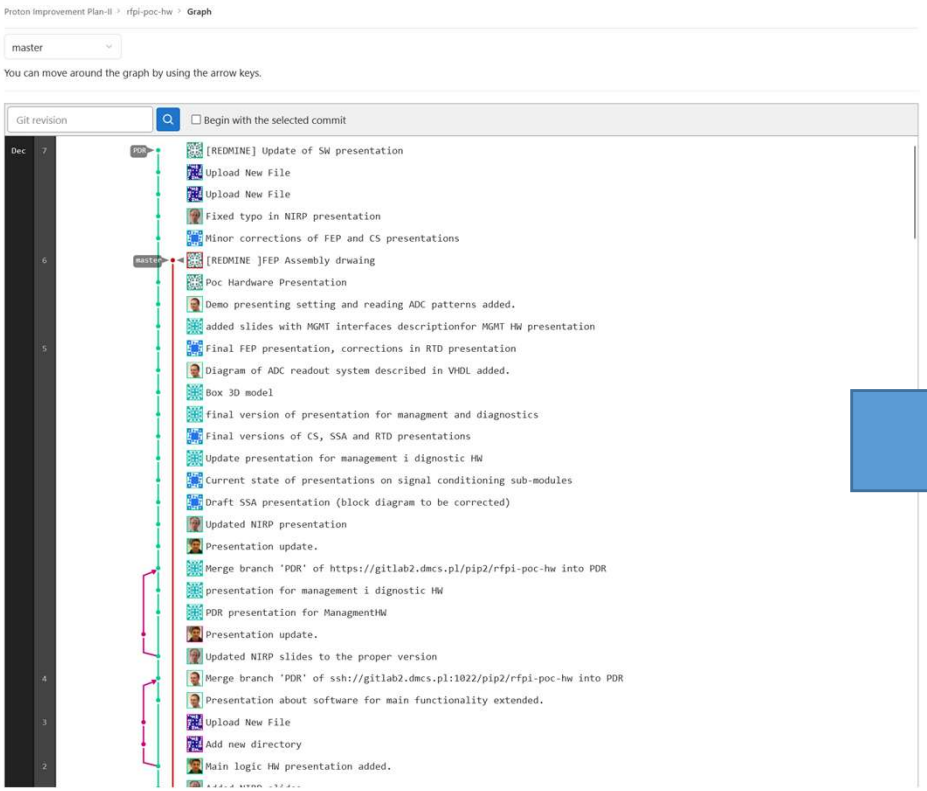
- REDMINE
  - Used for many project @ DMCS
  - Open-Source + Community
  - We manage our own installation (versions, plugins, configurations)
  - GIT integration

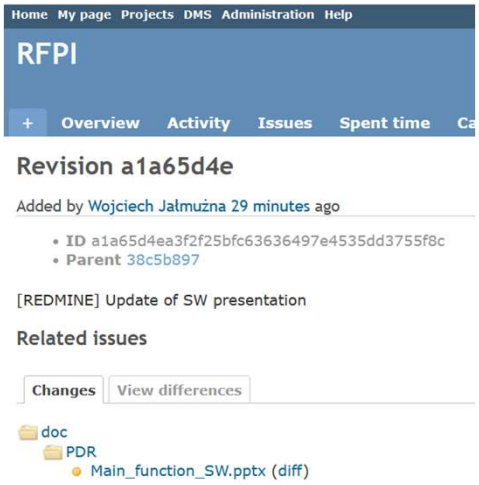


#	Parent task	Priority	Status	Subject	% Done	Assignee	Updated	Due date
195		Normal	In Progress	RFPI Box Design			10/14/2022 12:23 AM	
159	POC #195	Normal	In Progress	MCU Based Management Unit		Rafal Kotas	10/14/2022 12:23 AM	
305	POC #159	Normal	Planned	Test Watchdog and JTAG Interface			10/26/2022 11:45 AM	
324	POC #305	Normal	Planned	Modify STM32 Firmware to Support Watchdog connections		Rafal Kotas	10/26/2022 11:45 AM	
325	POC #305	Normal	Planned	Modify RPI library to support Watchdog and JTAG		Wojciech Tylman	10/26/2022 11:46 AM	
189	POC #195	Normal	In Progress	General Mechanical/Layout Planning			11/28/2022 11:48 AM	
299	POC #189	Normal	In Progress	Box assembly			10/22/2022 08:56 AM	
308	POC #299	Normal	In Progress	Prepare Cabling for Management		Rafal Kotas	11/14/2022 11:04 PM	
318	POC #299	Normal	In Progress	Prepare connections for Watchdog and JTAG Interface		Rafal Kotas	11/16/2022 02:29 PM	
261		Normal	In Progress	PoC project time planning for PDR scheduling		Wojciech Cichalewski	10/13/2022 11:12 AM	
310		Normal	In Progress	Placeholder for Software Tasks			10/22/2022 09:06 AM	
158	POC #310	Normal	In Progress	LLRF/MPS/Timing Link Implementation			11/28/2022 11:49 AM	
221	POC #310	Normal	In Progress	Prepare Wiki page about Ubuntu on Xilinx		Rafal Kielbik	10/22/2022 09:06 AM	
312	POC #310	Normal	In Progress	Prepare ADC Readout App		Rafal Kielbik	11/20/2022 07:40 PM	
316	POC #310	Normal	Planned	Prepare Test Pattern Tester for GPIO interface		Rafal Kielbik	10/25/2022 09:58 AM	
338	POC #310	Normal	In Progress	Conditioning boards tester		Piotr Amrozik	12/05/2022 05:48 AM	
313		Normal	Planned	Placeholder for Performance Measurements			11/14/2022 11:00 AM	
314	POC #313	Normal	Planned	Measure exact characteristics of ADC input stage			11/14/2022 11:00 AM	
339	POC #313	Normal	Planned	Measurements of NIRP characteristics		Grzegorz Jabłoński	12/02/2022 09:51 AM	
337		Normal	Planned	Corrections needed after initial prototype tests			11/29/2022 03:32 PM	

Project management and progress monitoring tool

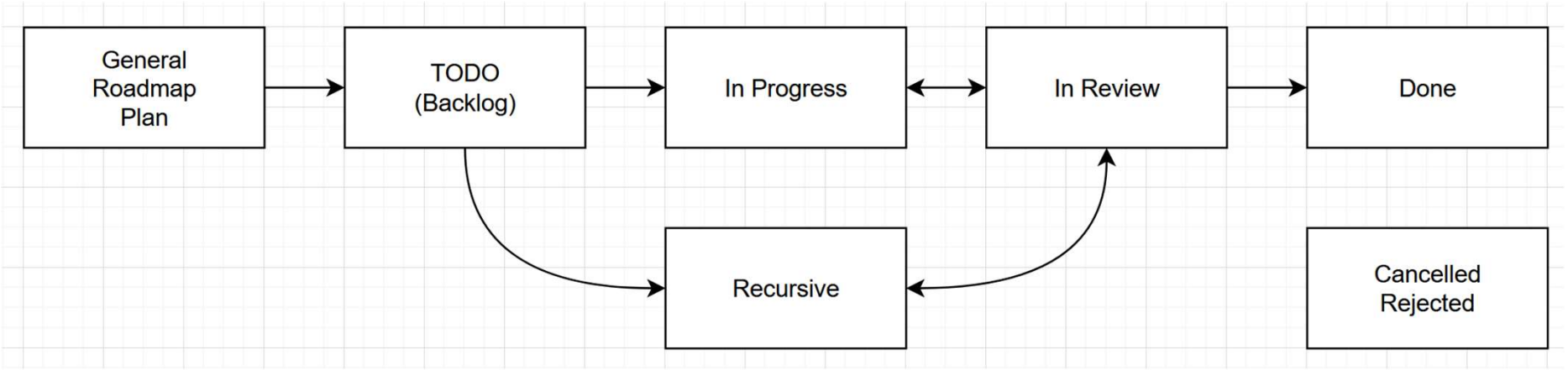
- REDMINE
  - Additional Extensions: Trello
  - GIT Integration





[Hardware] design workflow

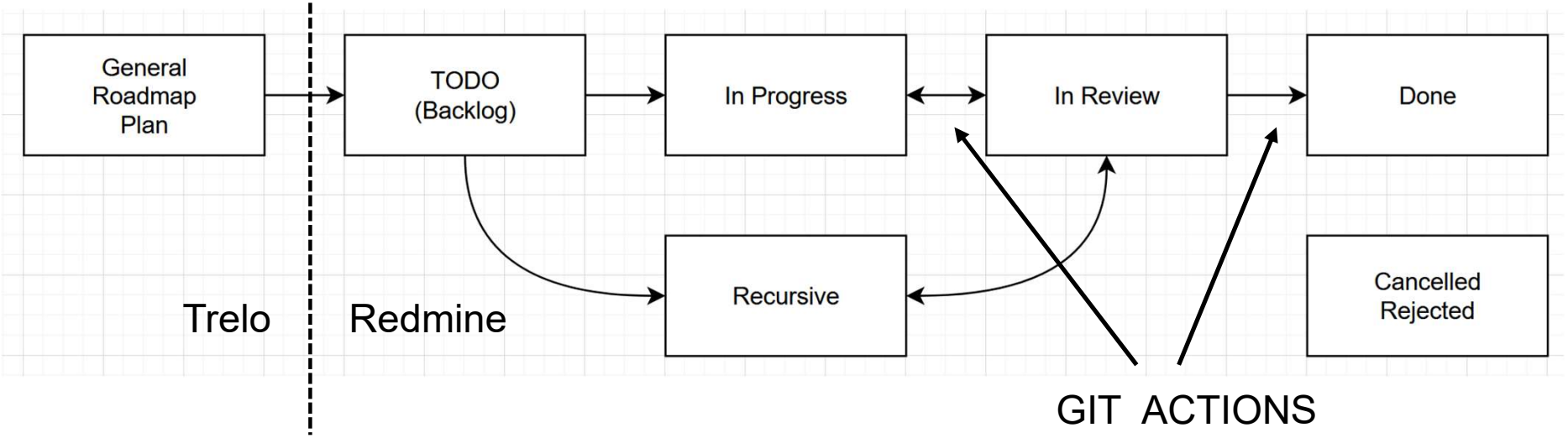
- In fact not only HW workflow, but general one



- one person to ensure workflow is kept
- configured on Redmine level
- permissions for different transitions

Hardware design workflow

- In fact not only HW workflow, but general one



- one person to ensure workflow is kept
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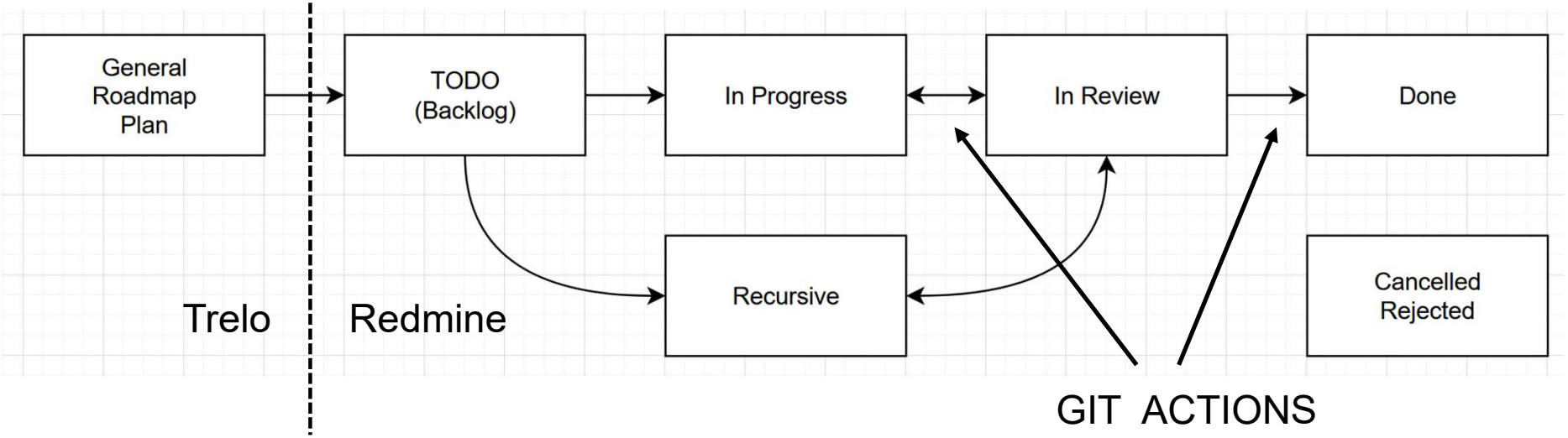
GIT ACTIONS

- Feature branches
- Review on redmine level
- Merge to master

Hardware design workflow

- In fact not only HW workflow, but general one



- one person to ensure workflow is kept
- configured on Redmine level
- permissions for different transitions

GIT ACTIONS
- Feature branches
- Review on redmine level
- Merge to master

BAD THINGS HAPPEN
when stuff is done outside of this diagram

Data Management

- GIT as main data repository and data exchange medium
  - if something is not on GIT, it does not exist
  - Exception: some temporary docs exist in form of Redmine Wiki pages with intention to submit them to repository when they are complete
- GITLAB used as web interface, but issue tracking and feedback features are not used there
- One repository manager responsible for merges and data/history consistency

[Hardware] Design Checklists

- Main Carrier board (most complex device) checklist has ~400 items
- No critical faults present in the design

				Schematic Approved by WJ as part of REDMINE #498	
Status	What was checked ?	What actions were taken ?	What additional actions must be taken ?	Actions done after review !	STATUS
OK	The synchronization of ports in Altium.				OK
OK	The connection of supplies on the schematic.				OK
OK	The connectivity of harnesses on the schematic using Altium connectivity insight tool.				OK
					intentionally empty
					intentionally empty
OK	Checked to see if the part number is in Digi-key database and if it points to correct part.				OK
OK	The pinout is checked with the datasheet.				OK
OK	The OE functionality is checked with the datasheet.				OK
OK	The footprint is checked with the datasheet.				OK
OK	The power supply levels are checked with the datasheet.				OK
OK	The decoupling recommendation is checked with the datasheet.	Added 10nF decoupling capacitor.			OK
FAIL	There is no termination and coupling on output clocks.		Decide where to add termination and coupling.	Added 10nF caps on Kria Sch	OK
FAIL			Define the use case.	Default intended usage is ETH - 125 MHz clock required. Item approved	OK
					intentionally empty
OK	Checked to see if the part number is in Digi-key database and if it points to correct part.				OK
OK	The pinout is checked with the datasheet.				OK