The PIP-II RFPI Project – Signal Conditioning Modules

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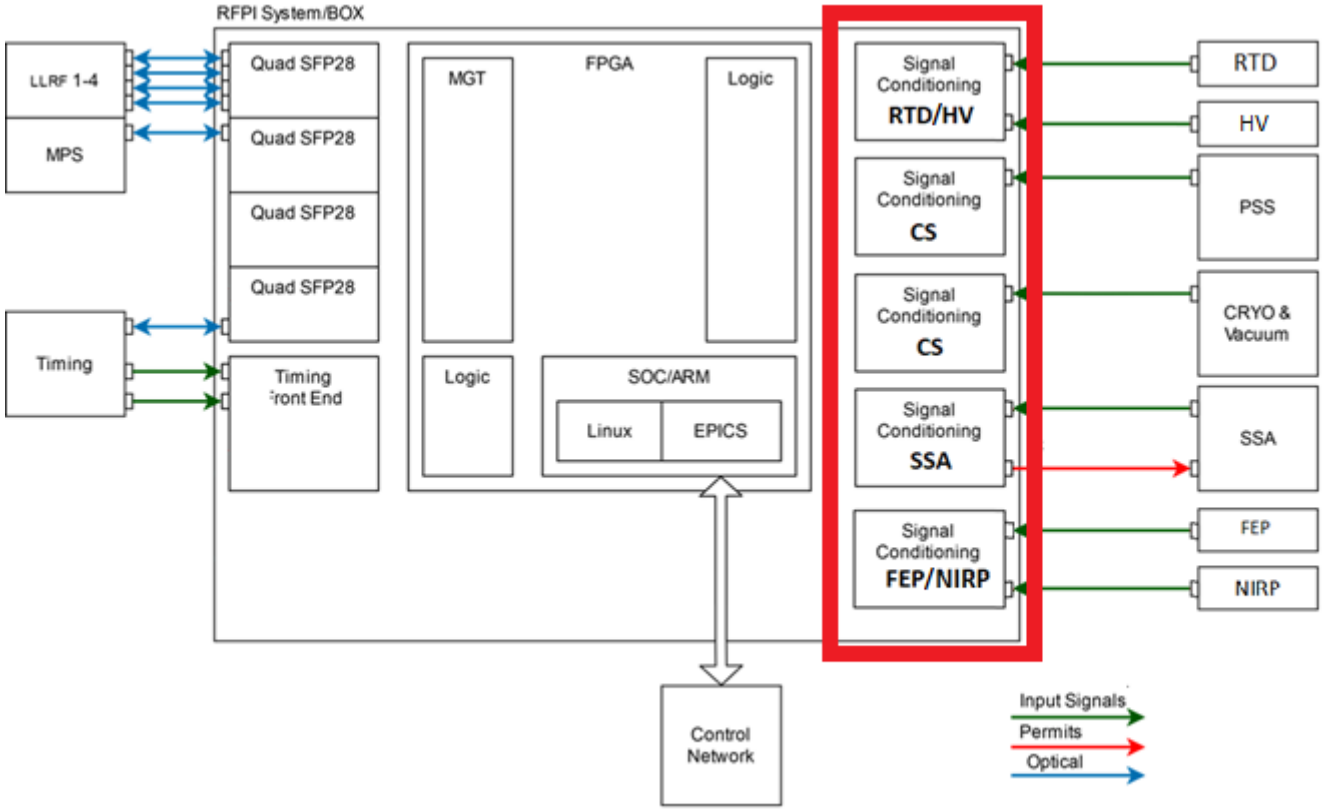
Agenda

- Signal Conditioning Boards (SSA, RTD, CS, FEP)
  - Module requirements
  - FDR specification and scope
  - Module design
  - Implementation
  - Test results discussion
- Summary

RFPI System – Signal Conditioning Boards



- 8 signals groups:
  - **Output permission signals (Solid State Ampliefiers)**
  - Clock/synchronization signals
  - **RTD temperature measurement**
  - Optical signals from LLRF
  - **Input enable signals (Contact Switches)**
  - NIRP (RF antennas)
  - **FEP (Field Emission Probe)**
  - Measurement of signals from "Coupler"

SSA Signal Conditioning Board

SSA Signal Conditioning Board - Requirements

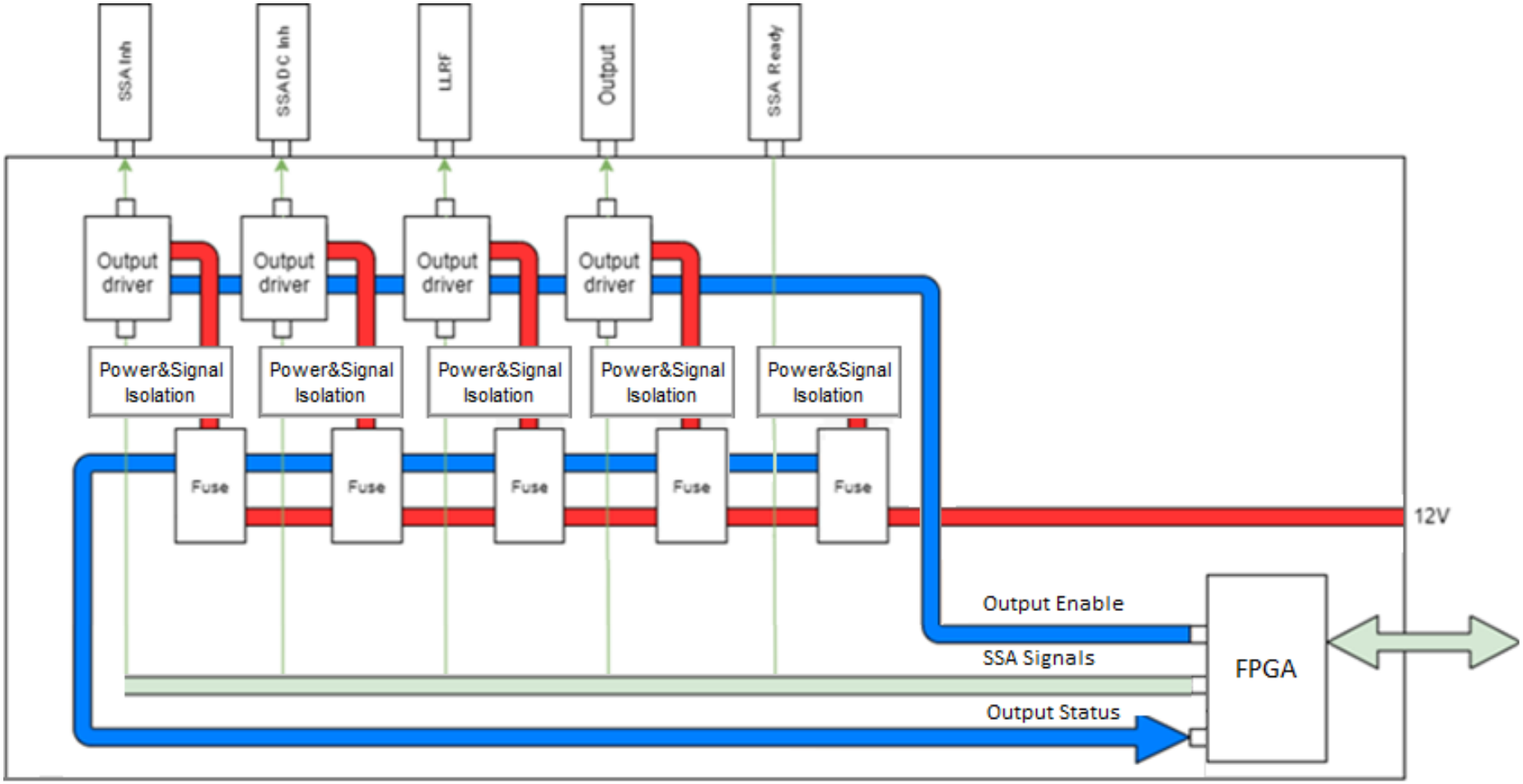
- The SSA (Solid State Amplifiers) signals group:
  - Ouputs:
    - SSA Inhibit
    - SSA DC Inhibit
    - LLRF Inhibit
    - Output #4
  - Inputs
    - SSA Ready
- TTL Voltage Levels
- Maximum output current at least 100 mA
- RFPI response time below 1 µs
- Overload (short-circuit) protection with fault signalling
- Isolation between RFPI system and SSA IOs

SSA Signal Conditioning Board – FDR Specification and Scope

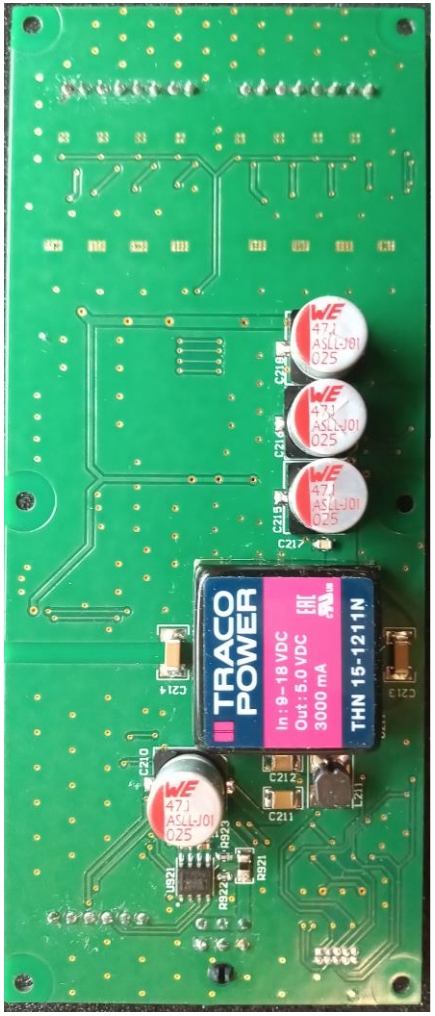
- **FDR vs PoC version**
  - Number of channels: 24 in FDR vs 8 in PoC
  - Hardware configurable direction of each channel
  - Isolation between channels
  - Separate channel power control for each cavity
  - Separate overload protection in each channel
  - Output load current up to:

    400 mA per channel in FDR vs 50 and 400 mA in PoC
  - Configurable logic (FPGA)
  - EEPROM for board identification
  - Use of smaller sized components (0402, QFN packages)

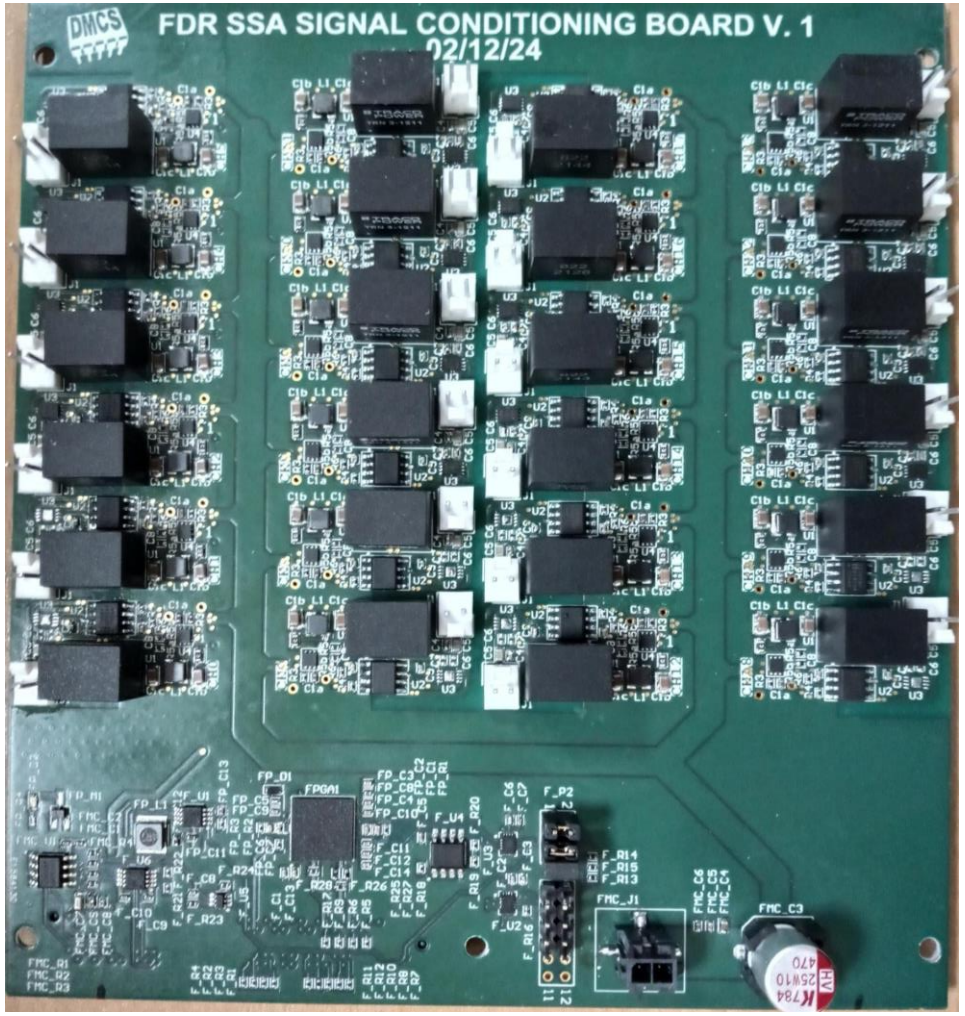
SSA Signal Conditioning Board – Block Diagram



SSA Signal Conditioning Board – PoC and FDR Versions

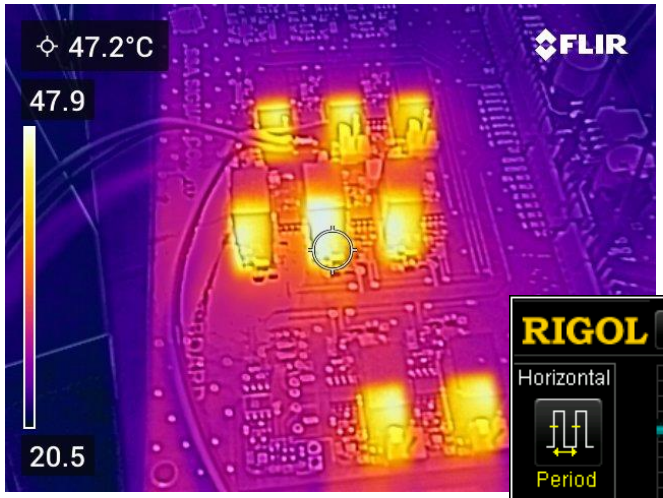


PoC Version

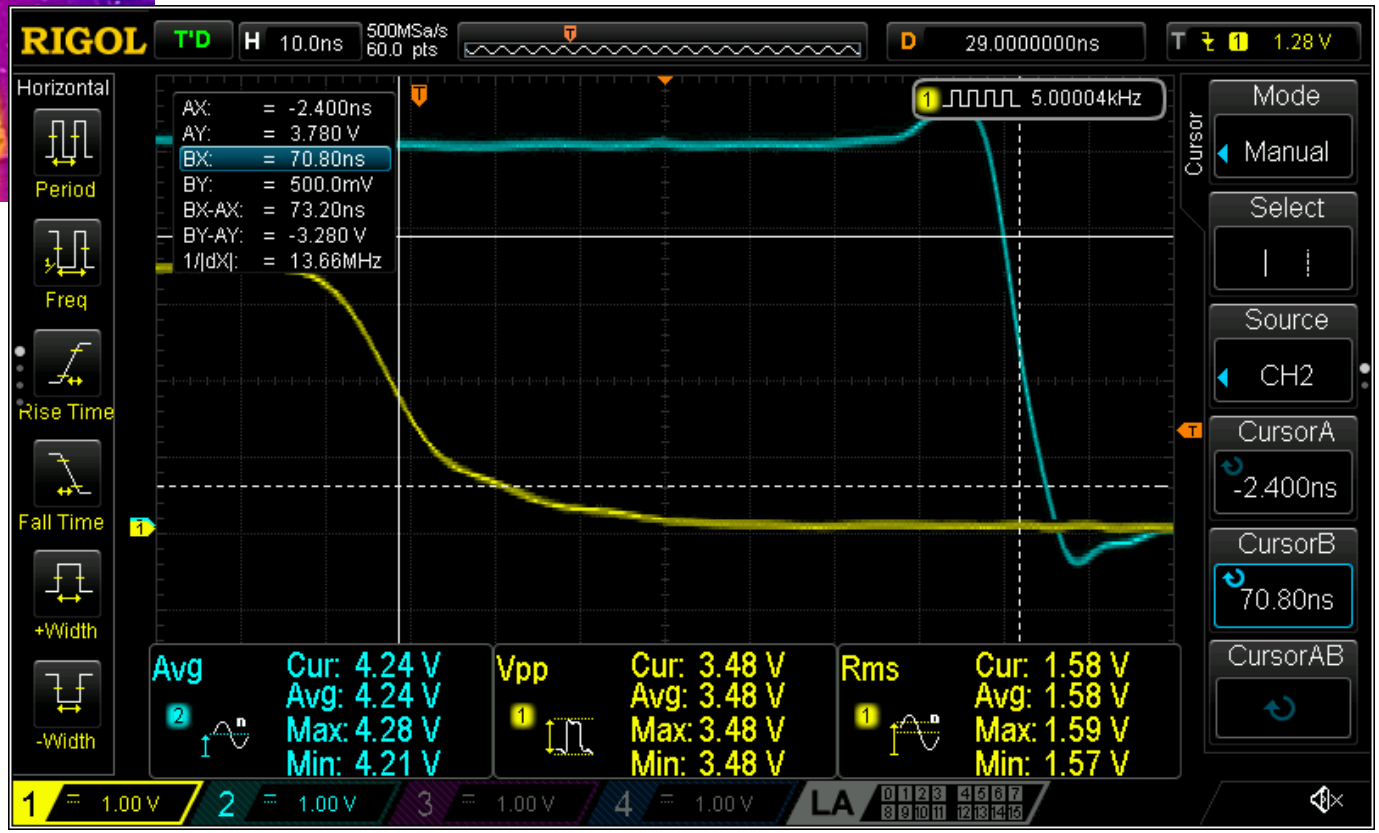


FDR Version

SSA Signal Conditioning Board - Results



Output signal delay: ~75 ns



RTD Signal Conditioning Board

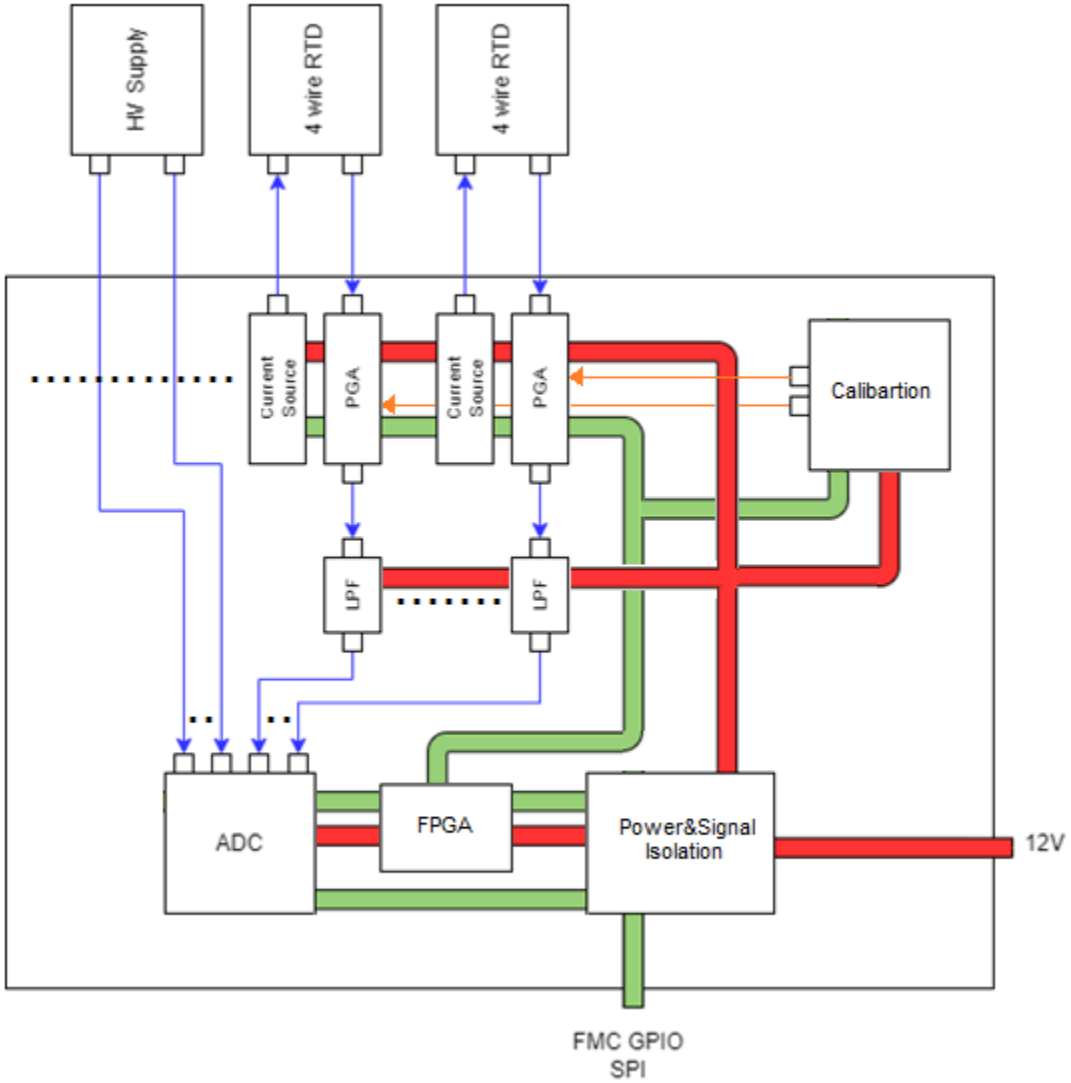
RTD Signal Conditioning Board - Requirements

- The RTD signals group: RTD 1, RTD 2, high voltage & current monitoring
- Temperature measurement redundancy based on PT-103 sensor
- Accuracy: 1 K
- Resolution: 100 mK
- Range: 275 ÷ 300 K
- Sensor current: up to 1 mA excitation, configurable (0 ÷ 1 mA)
- Radio-Frequency Interference (RFI) Immunity (4-wire sensing)
- Isolation between RFPI system and RTD IOs

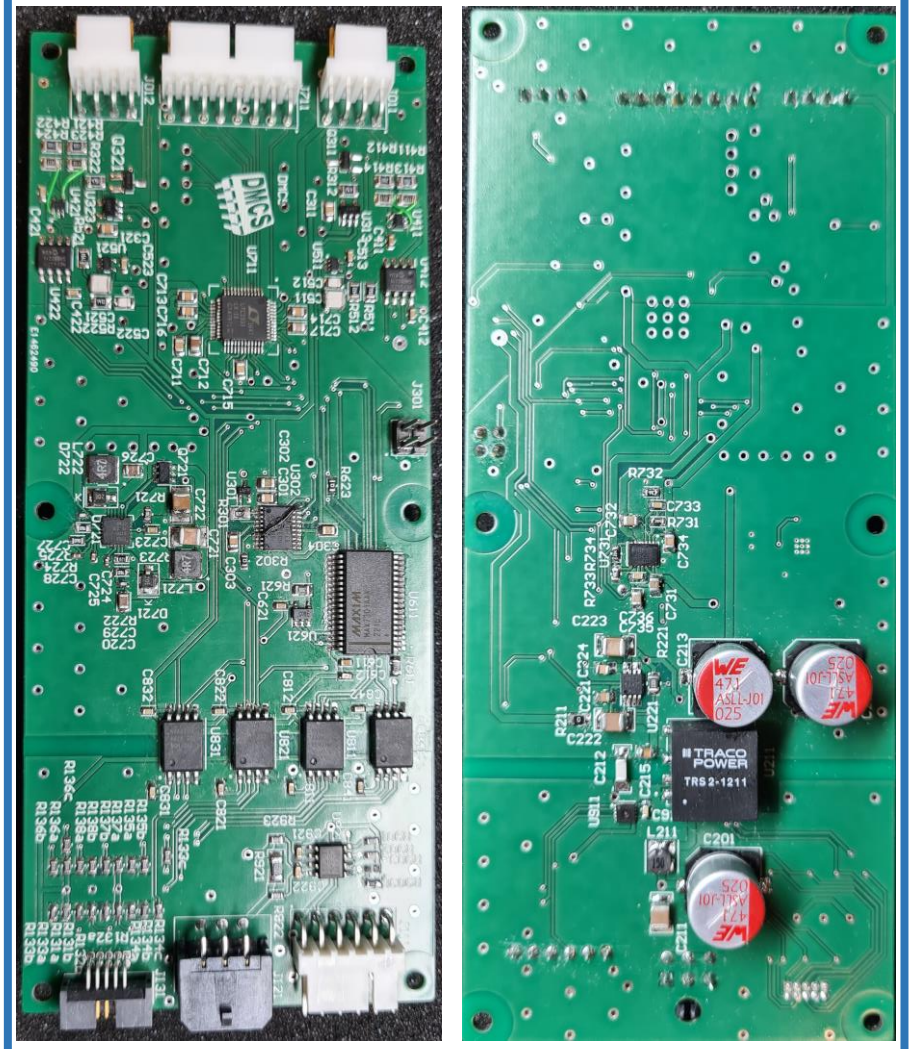
RTD Signal Conditioning Board – FDR Specification and Scope

- **FDR vs PoC version**
  - Number of channels: 8 in FDR vs 4 in PoC
  - Power good signal for isolated power supply:
    - Overcurrent protection
    - Undervoltage and overvoltage monitoring
  - Separate calibration for each channel
    - Four high precision resistors
    - Analog switches controlled with common calibration signals
  - Configurable logic (FPGA)
  - EEPROM for board identification
  - Use of smaller sized components (0402, QFN packages)

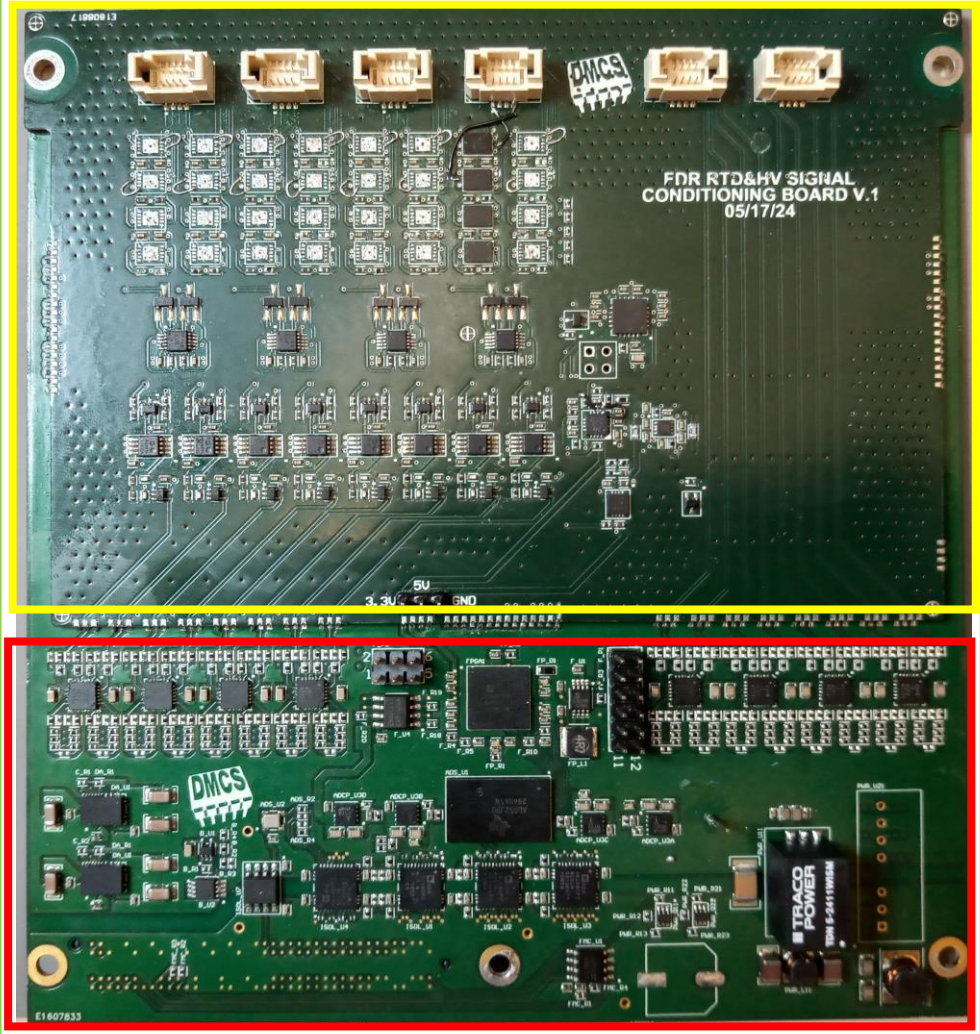
RTD Signal Conditioning Board – Module Design



RTD Signal Conditioning Board - PoC and FDR Versions



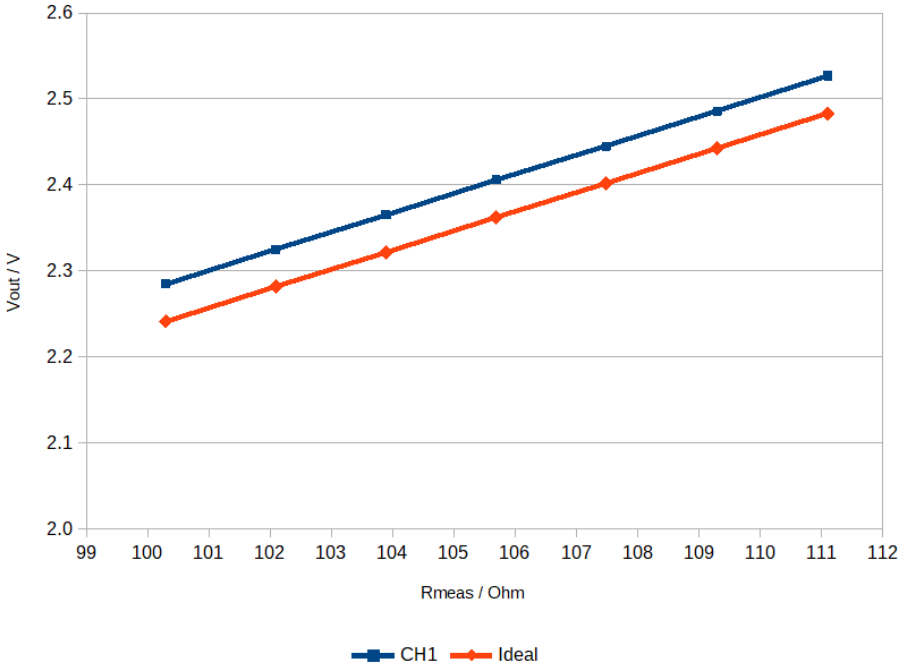
PoC Version

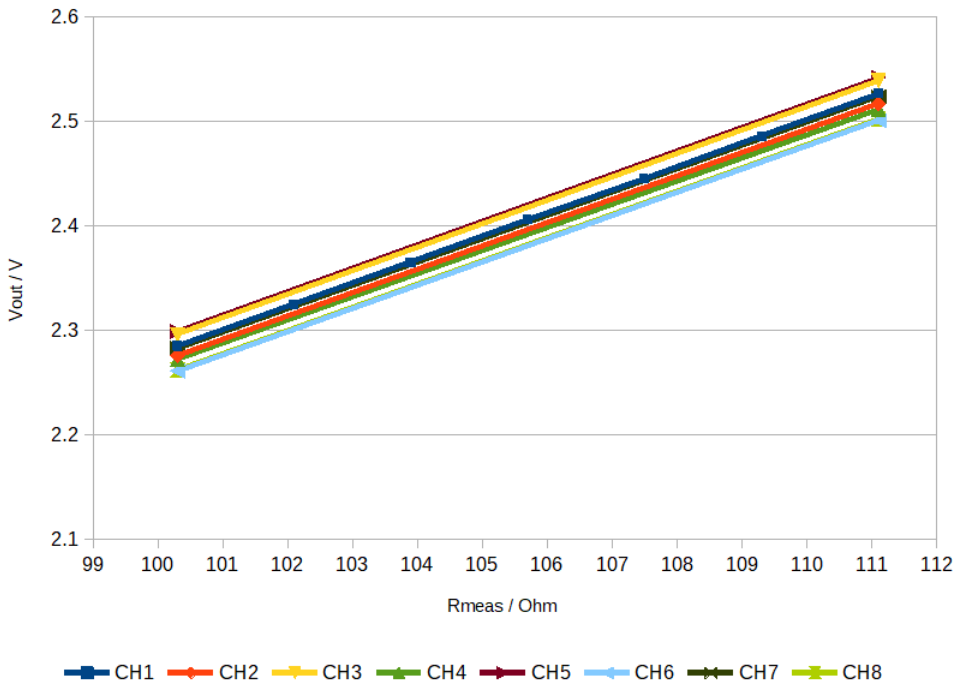


FDR Version

RTD Signal Conditioning Board - Results

Output voltage measurement for a given resistance





- Average error for raw data without callibration: 1,84%
- Gain as expected (30 V/V)
- Voltage offset error - to be easily compensated in software

- Repeatable gain in all channels (parallel characteristics)
- Spread of voltage offsets and output currents

CS Signal Conditioning Board

CS Signal Conditioning Board - Requirements

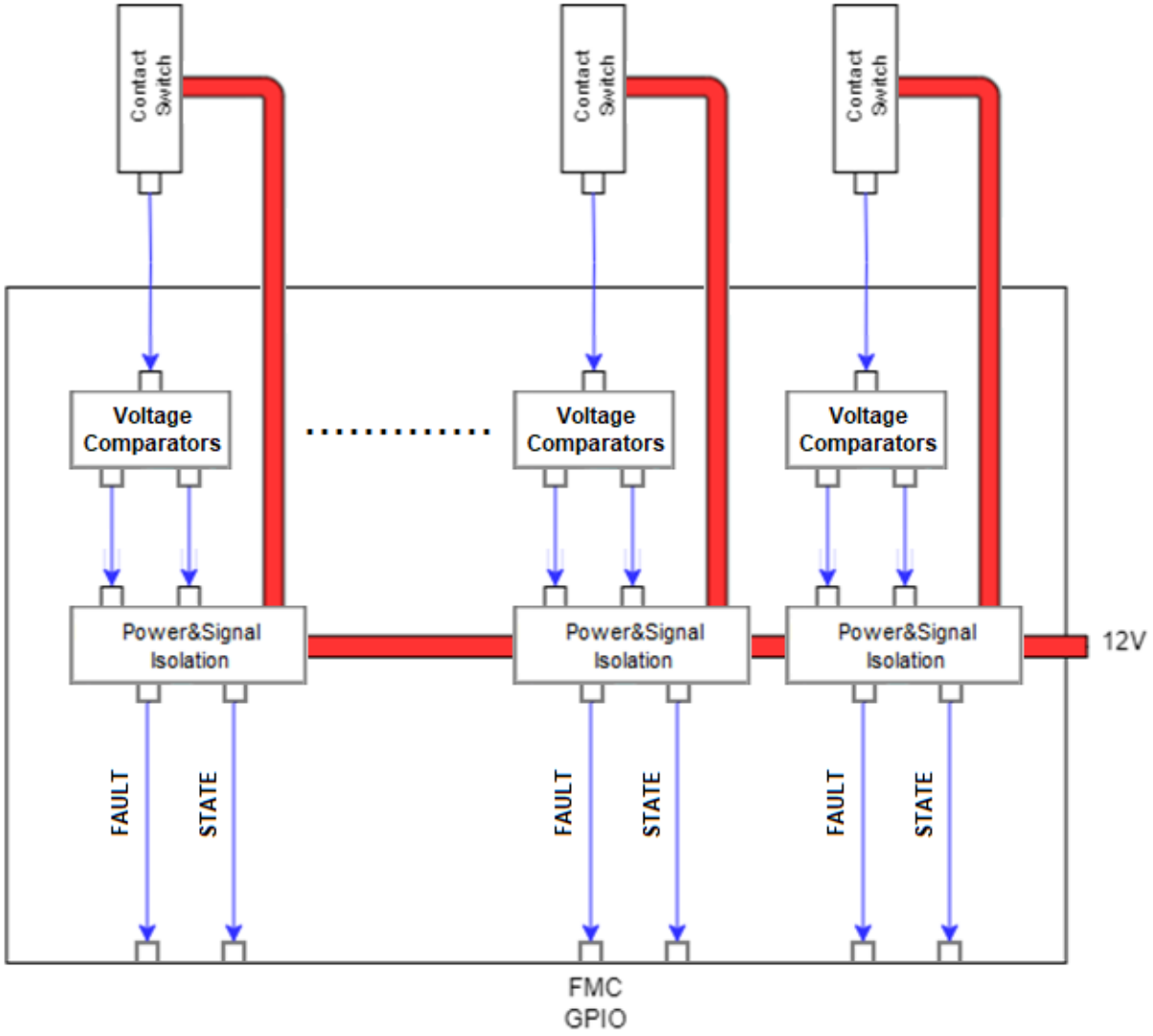
- The CS (Contact Switches) NC signals group:
  - Cryo (2 per RFPI system), 12 VDC, min. 100 mA (100 ÷ 120 mA)
  - Beam (2 per RFPI system), 12 VDC, min. 100 mA (100 ÷ 120 mA)
  - Fluid (4 per RFPI system), 12 VDC, min. 10 mA (40 ÷ 43 mA)
  - Vacuum (4 per RFPI system), 12 VDC, min. 10 mA (40 ÷ 43 mA)
  - PS (4 per RFPI system), 24 VDC, min. 8 mA (8.5 mA)
- RFPI response time below 10 μs
- Isolation between RFPI system and CS IOs
- Cable diagnostics (detection of short-circuits and open-circuits)

Cryo = He Pressure and Level
Beam = Beam Vacuum Permit
Fluid = Coupler Window Cooling Airflow Permit
Vacuum = Coupler Vacuum Permit
PS = Personal Safety

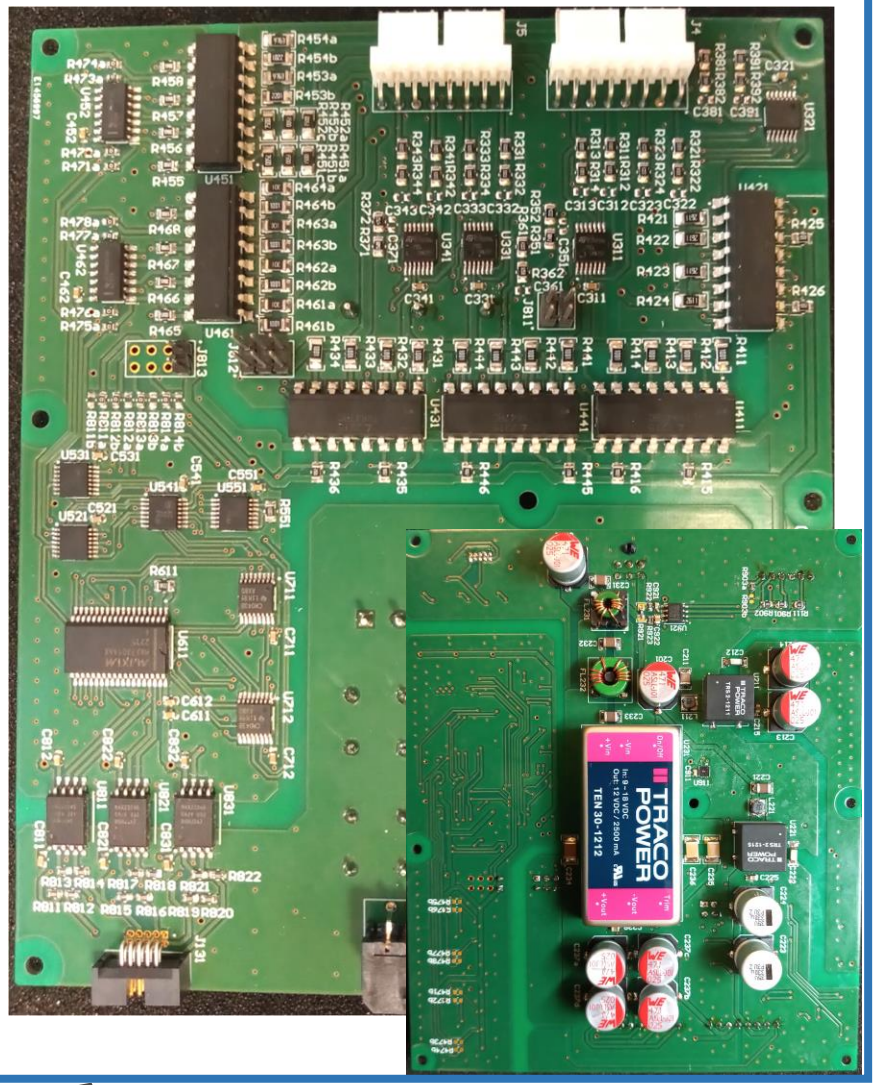
CS Signal Conditioning Board – FDR Specification and Scope

- **FDR vs PoC version**
  - Number of channels: 16 (8 per board) in FDR vs 8 in PoC
  - Isolation between channels
  - Hardware configurable channels (output voltage and current)
  - Separate power control for each channel
  - Low side switching in FDR vs high side switching in PoC
  - Improved heat dissipation
  - EEPROM for board identification
  - Use of smaller sized components (0402, QFN packages)

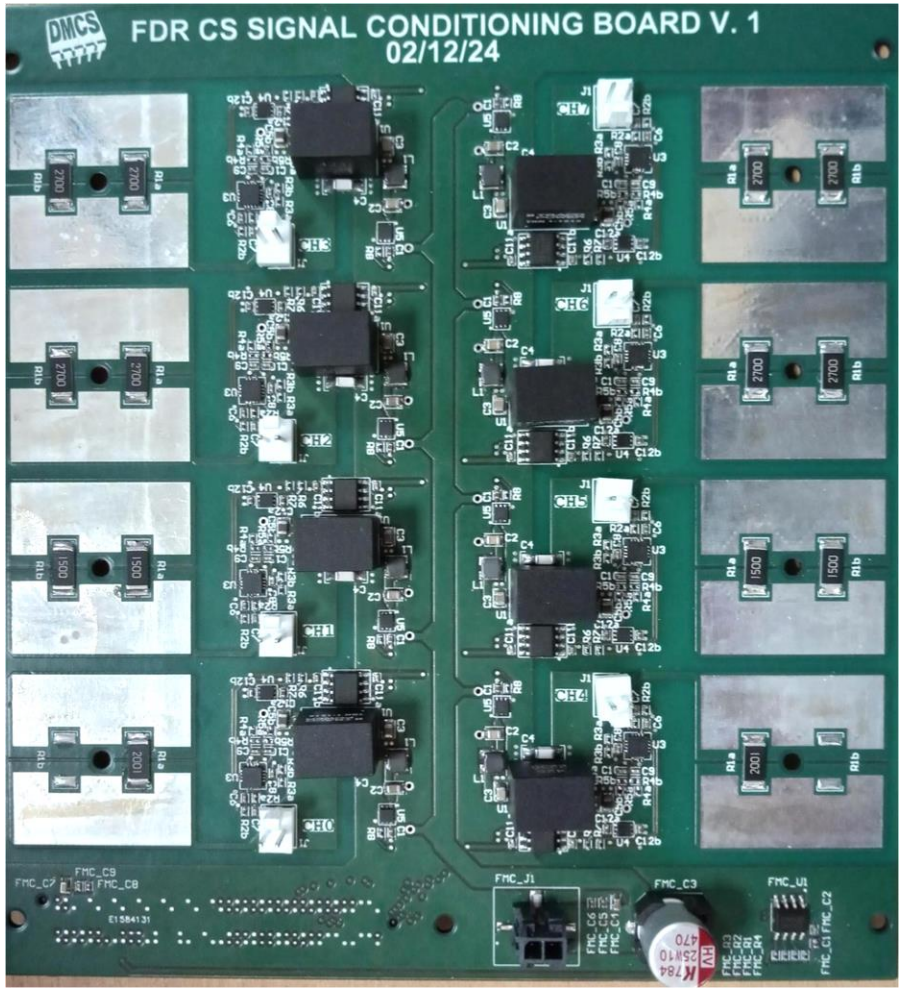
CS Signal Conditioning Board – Block Diagram



CS Signal Conditioning Board – PoC and FDR Versions

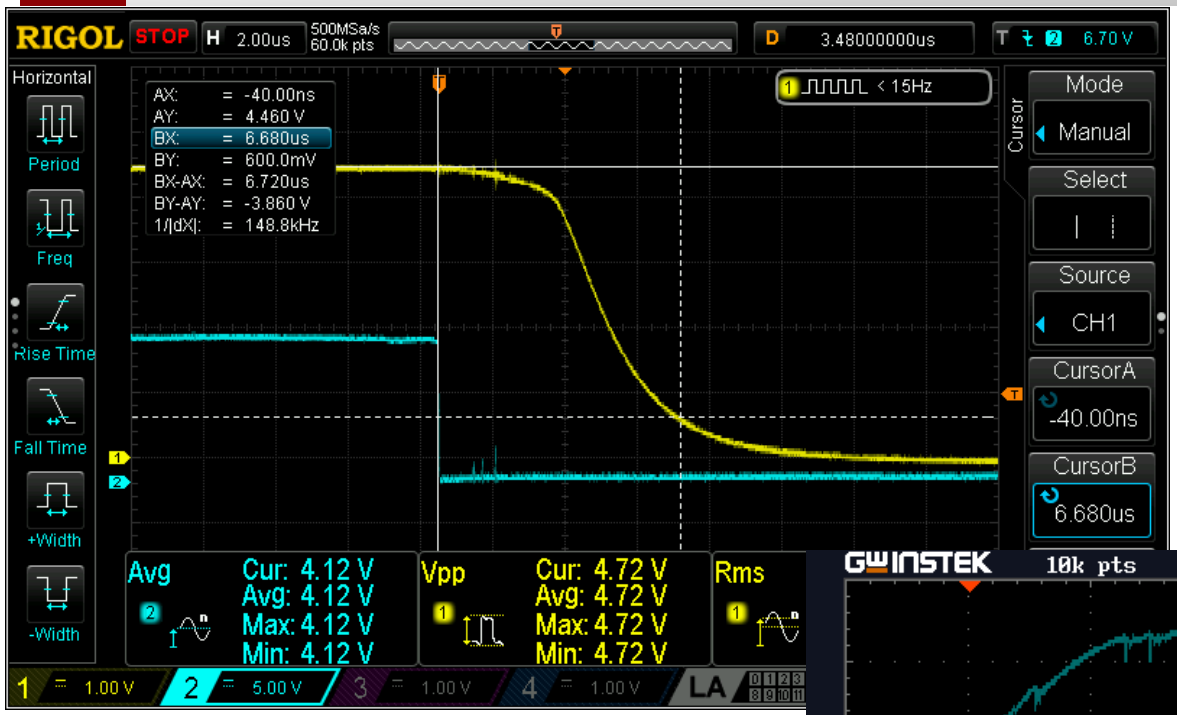


PoC Version

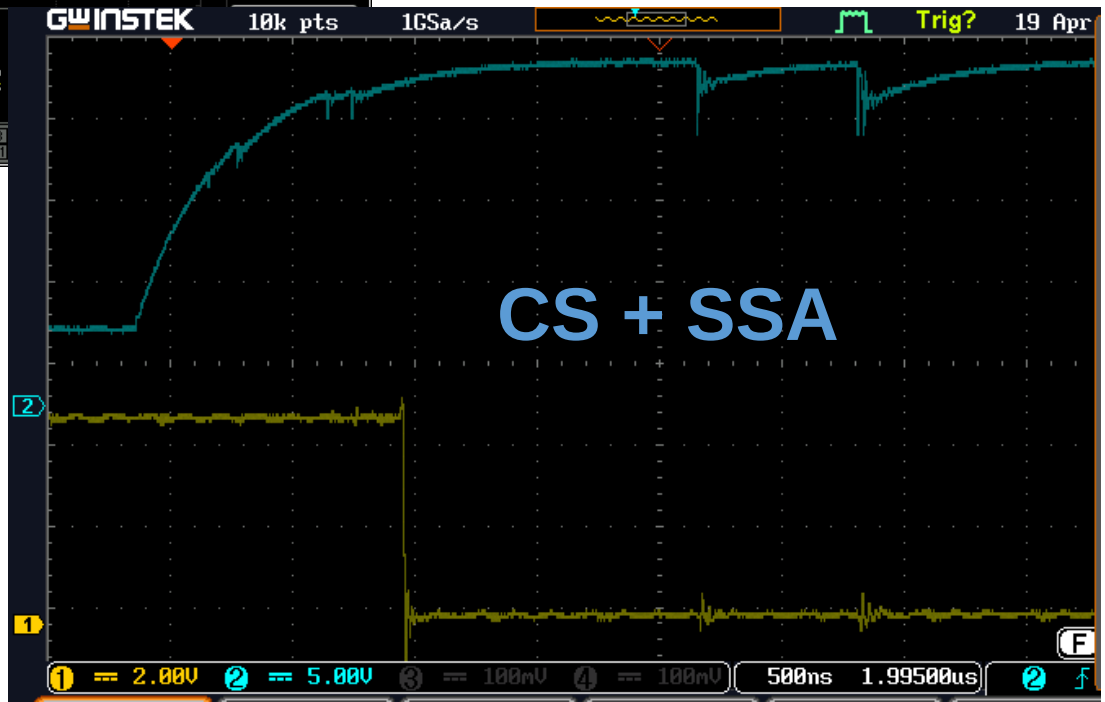


FDR Version

CS Signal Conditioning Board - Results



POC:
3.2 ÷ 9.7 µs

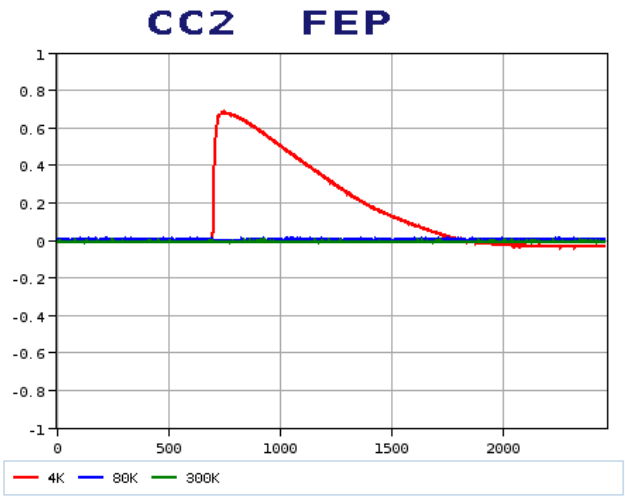


FDR:
0.28 ÷ 0.56 µs

FEP Signal Conditioning Board

FEP Signal Conditioning Board - Requirements

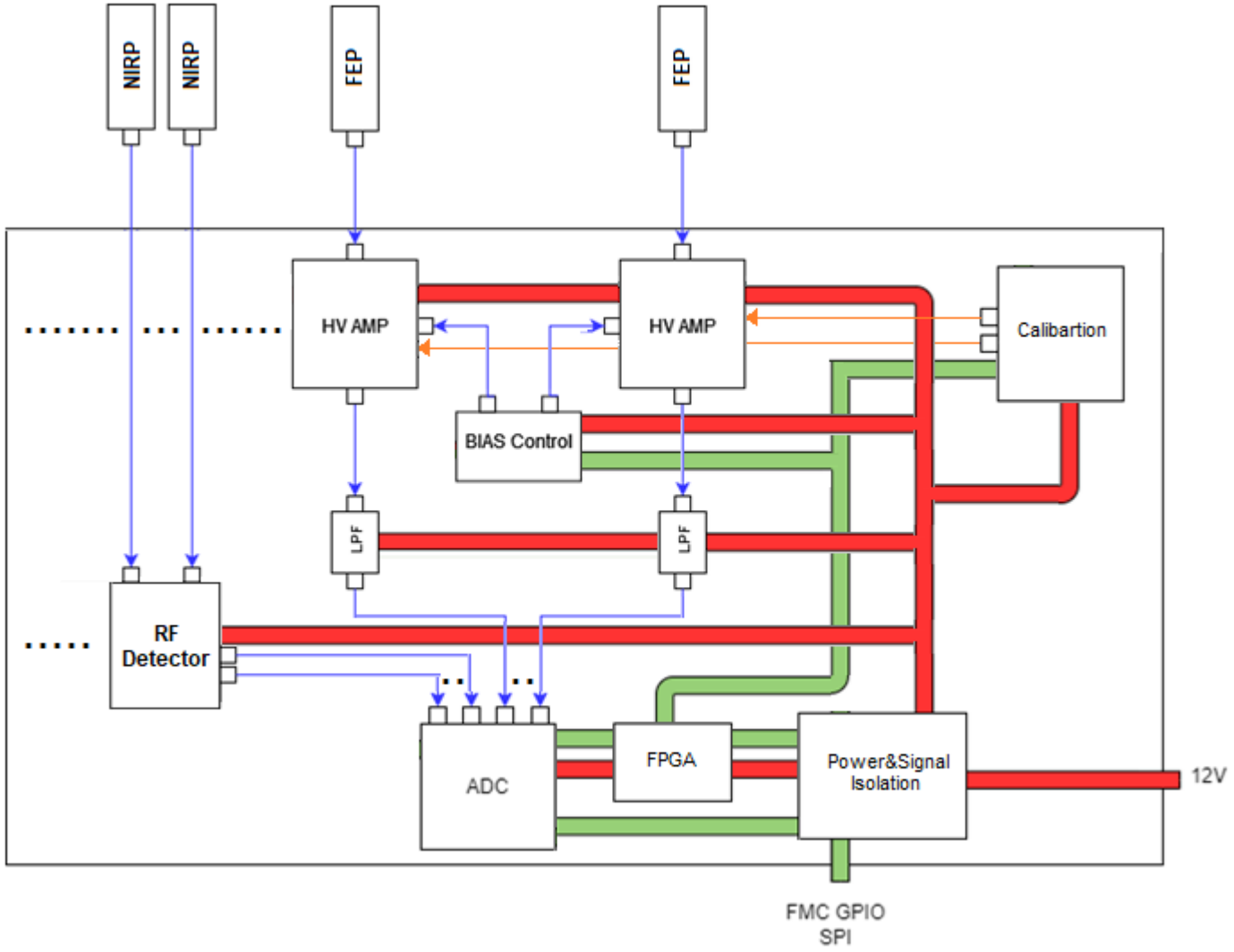
- One probe per cavity/coupler (previously 3 per cavity/coupler),
- Bias voltage settable from **35 V up to 40 V** (previously 0 ÷ 45 V)
- Bias regulation rage 0.1 V (previously undefined)
- Current detection resolution below 10 nA (previously below 10 μA)
- Current detection range up to 100 μA (previously up to 10 mA)
- Trip (threshold) levels set under software control
- Threshold regulation **range** from **100 nA to 100 μA** (previously undefined)
- Threshold regulation **accuracy below 50 nA** (previously undefined)
- RFPI **response time below 100 μs** (previously below 1 μs)
- Isolation between RFPI system and FEP inputs



FEP Signal Conditioning Board – FDR Specification and Scope

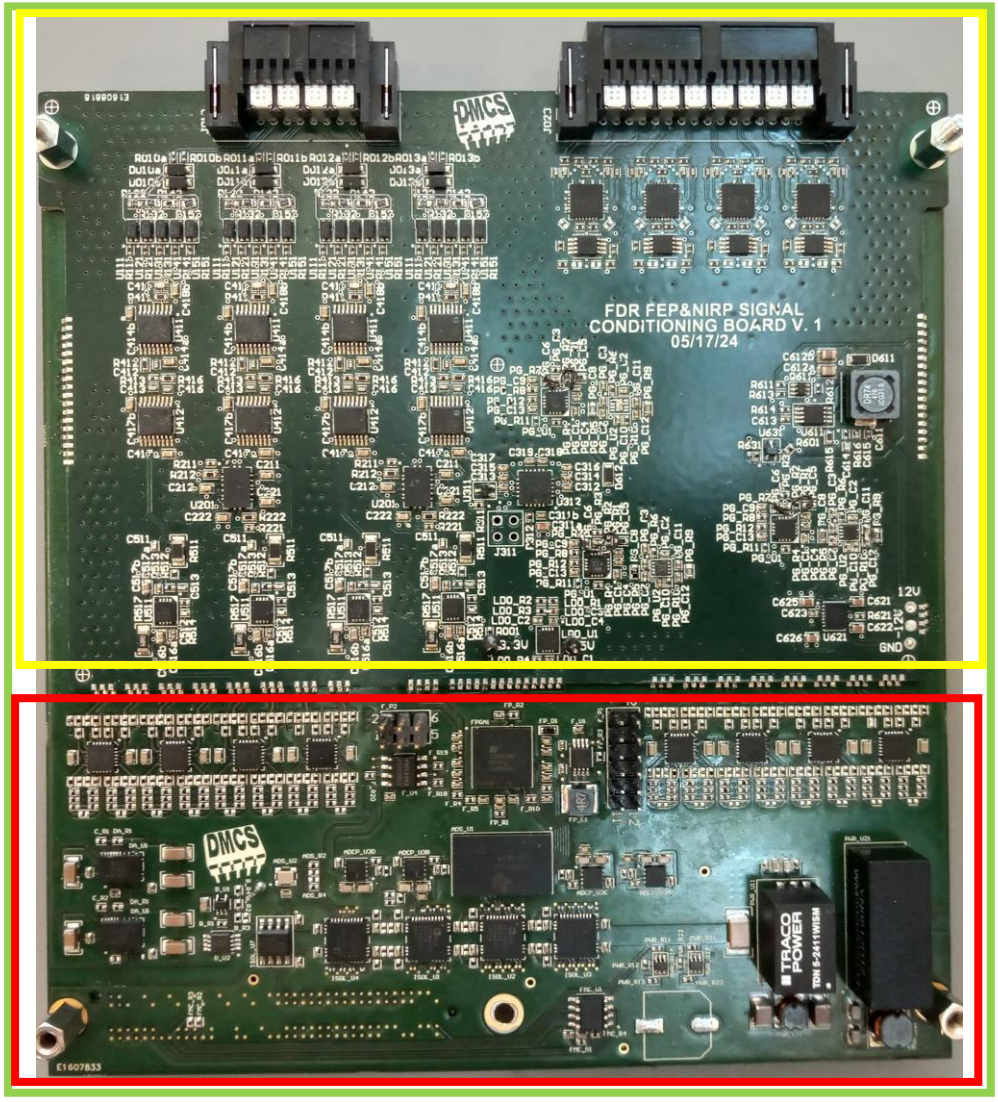
- **FDR vs PoC version**
  - Number of channels: 4 in FDR vs 2 in PoC
  - Power good signals for isolated power supply:
    - Overcurrent protection
    - Undervoltage and overvoltage monitoring
  - Overtemperature signal for HV amplifiers
  - Guard rings for inputs
  - Separate calibration for each channel
    - Four high precision resistors
    - Analog switches controlled with common calibration signals
  - ADC integrated FMC board
  - Configurable logic (FPGA)
  - EEPROM for board identification
  - Use of smaller sized components (0402, QFN packages)

FEP Signal Conditioning Board – Block Diagram



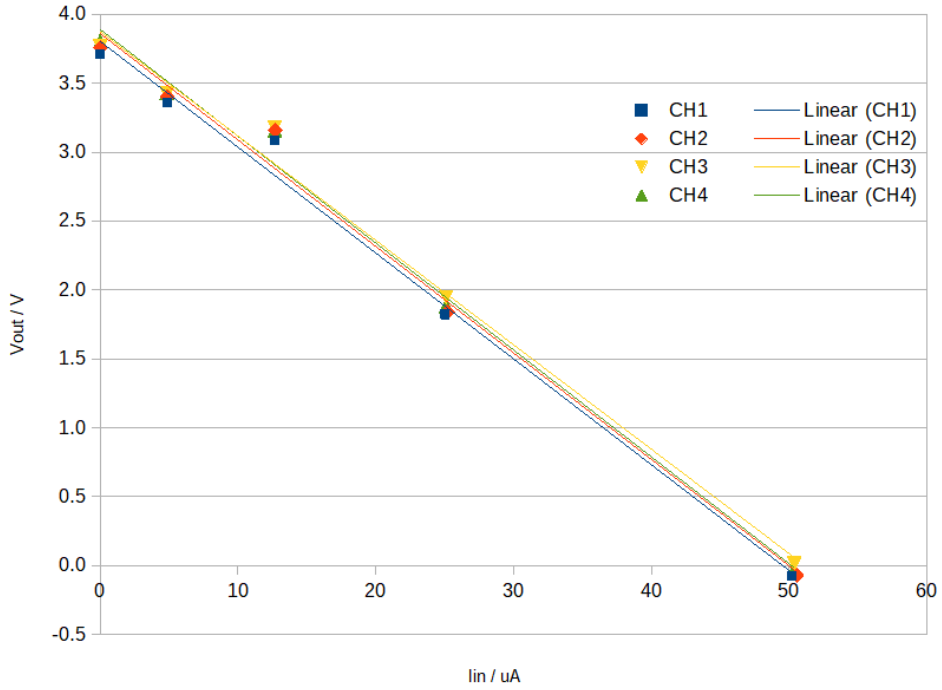
FEP Signal Conditioning Board – PoC and FDR Versions

PoC Version



FDR Version

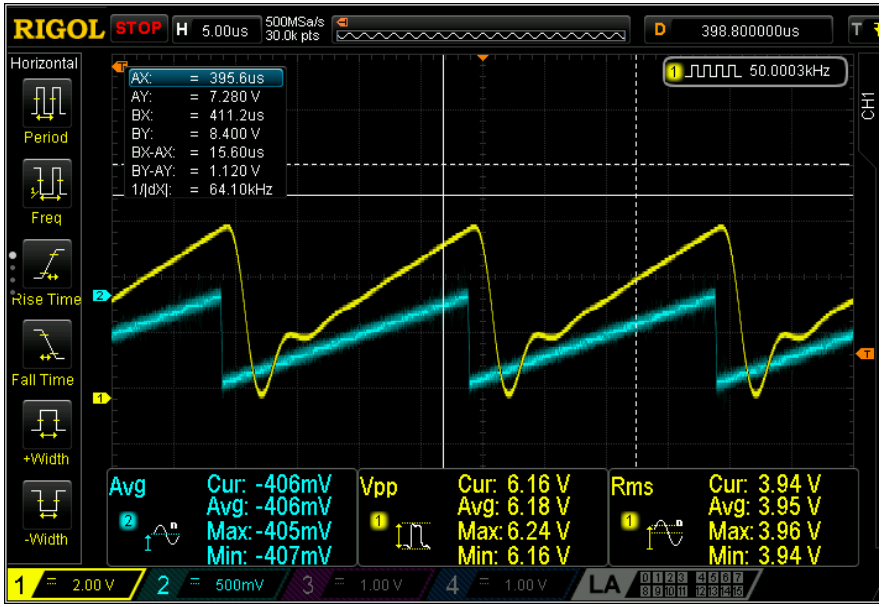
FEP Signal Conditioning Board - Results



Average gain: 64 kV/A

Output voltage ripple: 2.6 ÷ 3.8 mV

Output signal delay: 2 µs



RFPI Signal Conditioning Circuits - Summary

- All signal conditioning boards assembled and tested in laboratory conditions:
  - SSA
    - Power supply, output drivers, overcurrent protecion, digital signal isolators, communication, FPGA
  - RTD
    - Power supply, output current control, analog signal processing
  - CS
    - Power supply, voltage comparators (cable fault and CS state), digital signal isolators, communication
  - FEP
    - Power supply, bias voltage control, calibration, analog signal processing