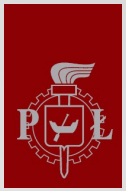


# RFPI Full Scale Prototype Hardware Overview

Wojciech Jałmużna

# Agenda

- POC Hardware and Conclusions,
- First Plan for Full Scale Prototype,
- Full Scale Prototype
- Summary

# POC Hardware and Conclusions

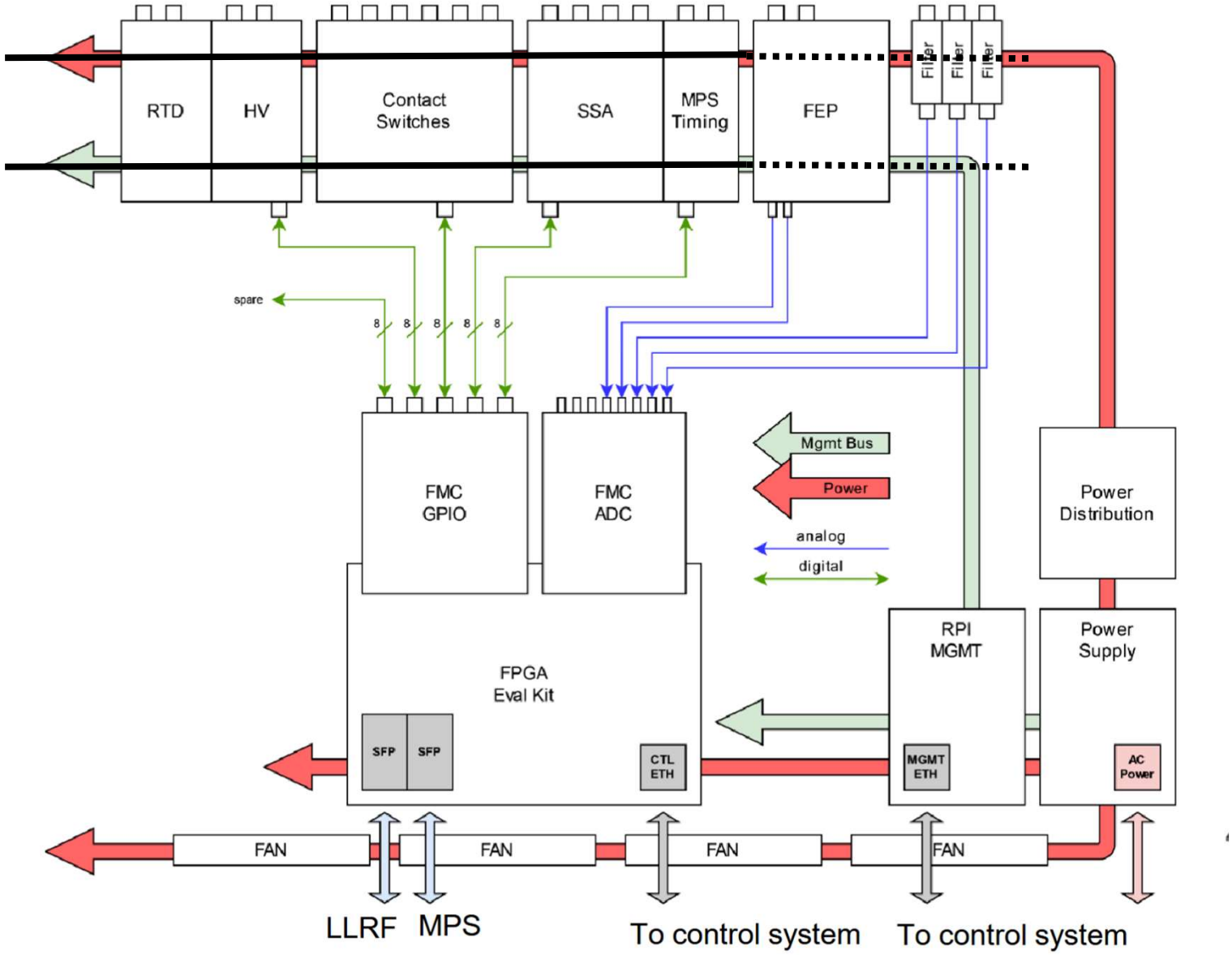
*PoC - specification and scope*

- Most important part of POC is to check:
  - analog front-ends
  - data flow concept
  - integration of various parts on all levels
  - hardware/software workflows
- There was no focus to include final number of channels
- We decided to use as many off-the-shelf components as possible
- Since the system will work in distributed environment with many connections, we tried to provide electrically isolated interfaces to the outside

# POC Hardware and Conclusions

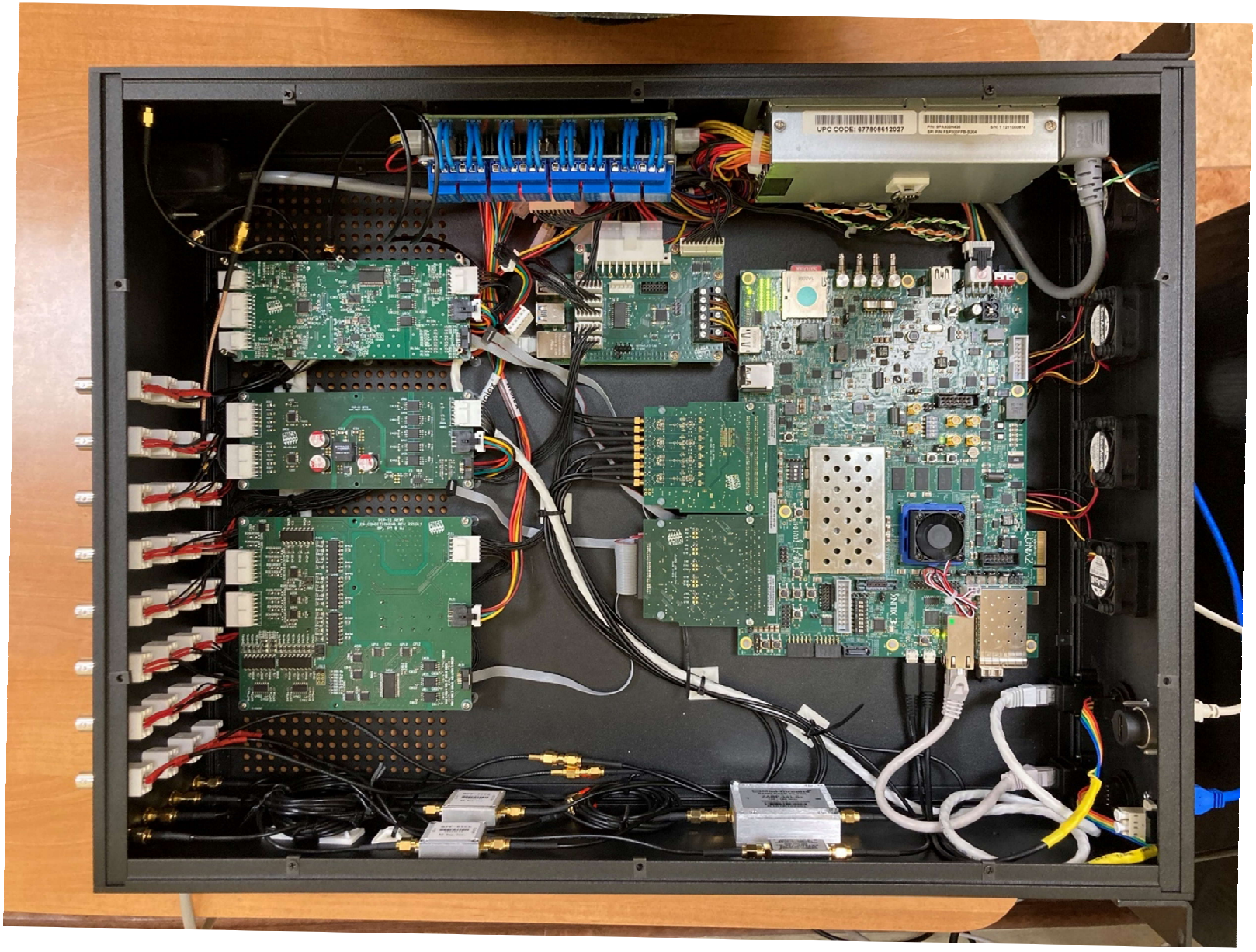
*The functionality and design details*

Isolation lines



# POC Hardware and Conclusions

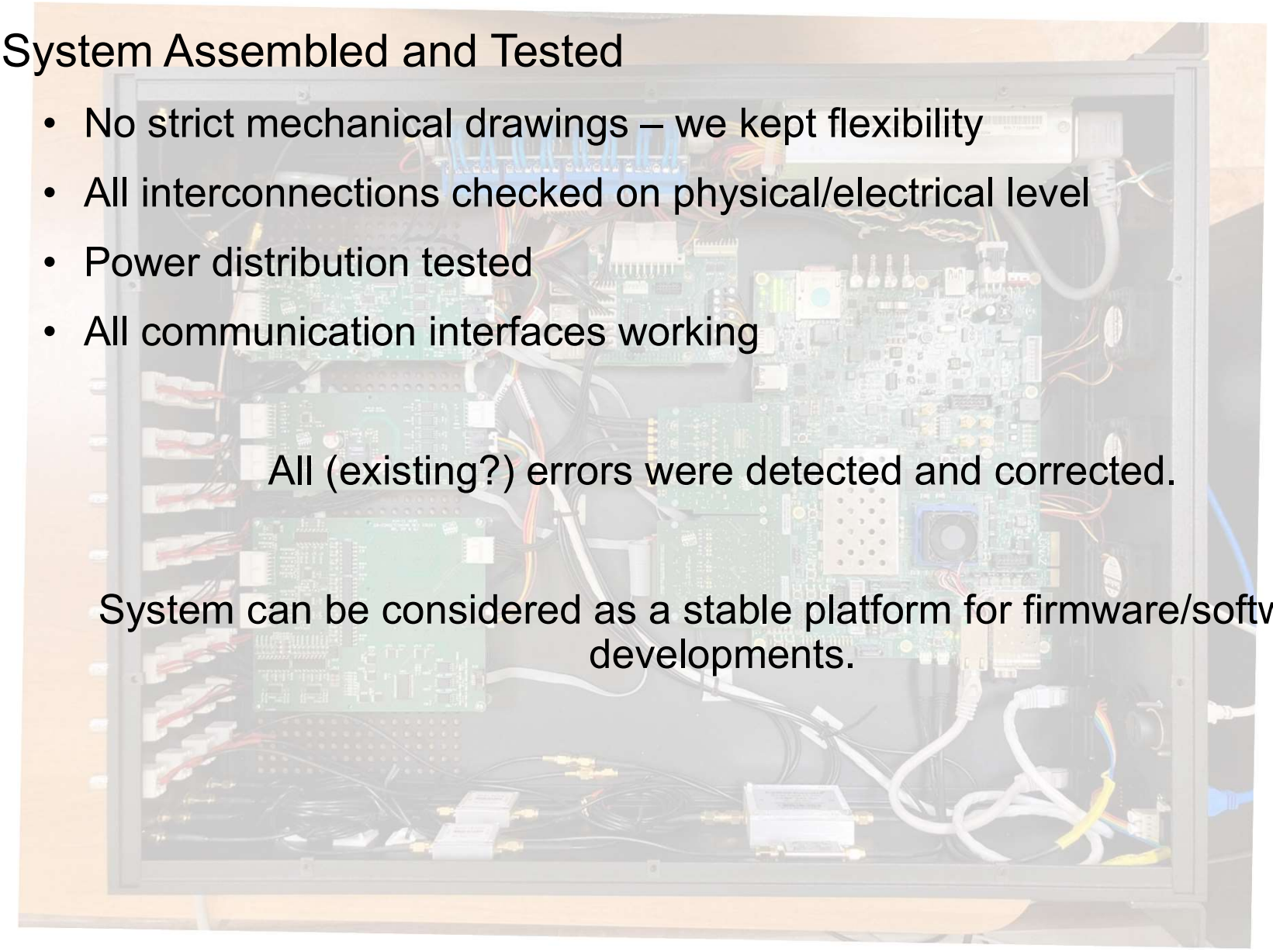
## *Implementation*



# POC Hardware and Conclusions

*Test results discussion*

- System Assembled and Tested
  - No strict mechanical drawings – we kept flexibility
  - All interconnections checked on physical/electrical level
  - Power distribution tested
  - All communication interfaces working



All (existing?) errors were detected and corrected.

System can be considered as a stable platform for firmware/software developments.

# First Plan for Full Scale Prototype

*Full scale design plans*

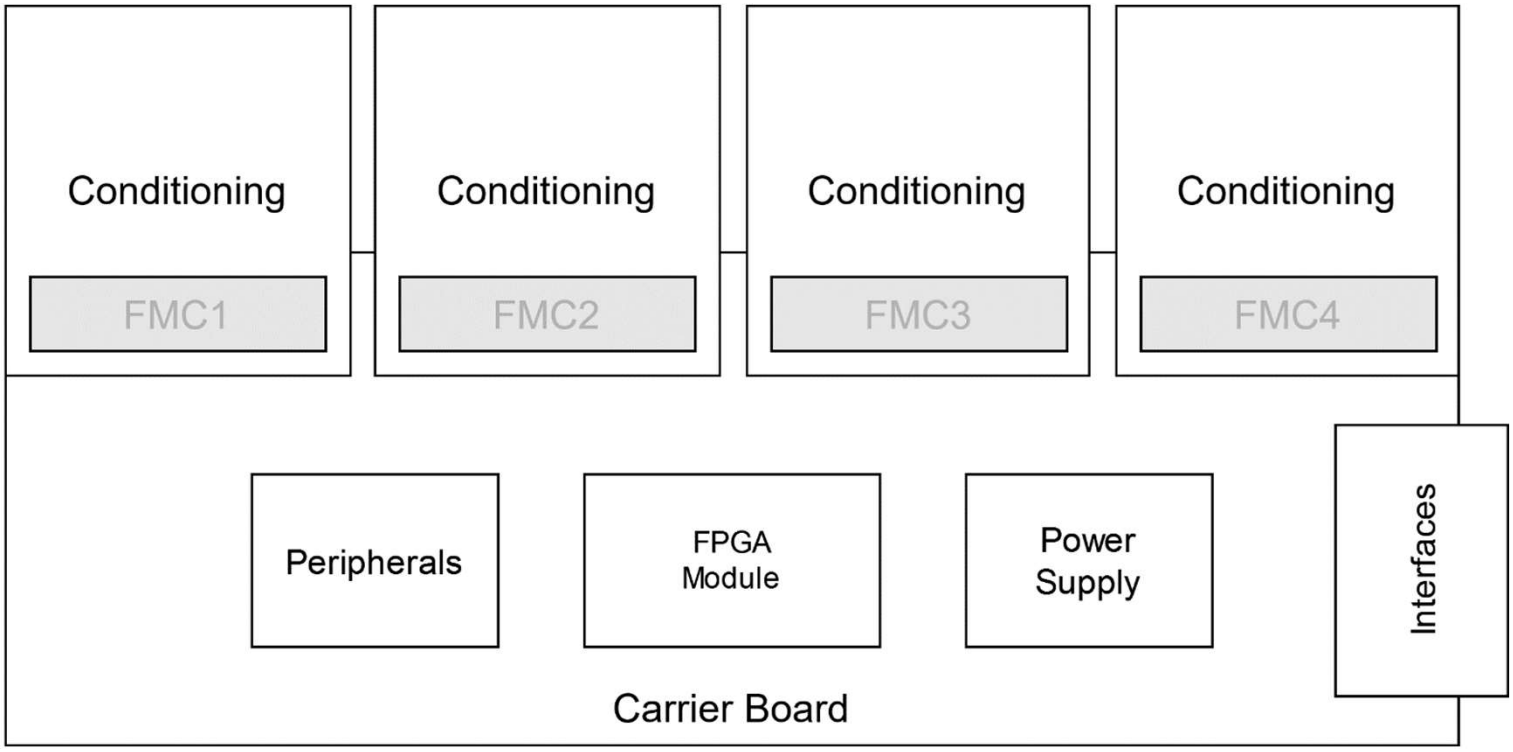
## Final Solution Possibilities:

- Xilinx FPGA Module (off-the-shelf, for example Xilinx Kria)
- Custom Carrier Board treated as base for pluggable modules
- Conditioning modules in standardized form factor (for example FMC)
  - Electrical specification kept (limited number of IOs but still more than now)
  - Mechanical Specification treated only as guidelines
  - ADVANTAGE: modules can be tested and developed using any FMC carrier
- Size of the box matches the system
- We keep “patch panel” option

Some Mechanical Details must be clarified before making final proposal

# First Plan for Full Scale Prototype

*Full scale design plans*



# First Plan for Full Scale Prototype

*Full scale design plans*

| Module | Fast IOs | Slow IOs |
|---|---|---|
| CS (split channel count /2) | 16 + 16 | 0 |
| SSA | 21 | 0 |
| Fast ADC | 24 | 5 |
| Slow ADC | 10 | 0 |
| Additional | 4 | 4 |
| **TOTAL** | **91** | **9** |

| Name | Quantity | Count |
|---|---|---|
| MGT to LLRF | 1 per 2 cavities | 2 |
| MGT to MPS | 1 per rfpi | 1 |
| ETH | 1 per rfpi | 1 |

# First Plan for Full Scale Prototype

*Full scale design plans*


Ready to use module

- 4 GB DDR4 Memory (x64 1200 MHz)
- 16 GB eMMC
- 116 HP IOs + 69 HD IOs **(91 used)**
- 4x GTH (16 Gbps)
- 4x GTR (up to 5 Gbps ) ETH dedicated
- 49 “slow” ARM pins **(9 used)**

**Kria Module** still has some **spare pins** – we can increase pin allocation for each module to provide space for **future improvements and scaling**. Taking the **same amount of pins** for each module will make them **compatible** and **allow** easy **position exchange**

# First Plan for Full Scale Prototype

## *Full scale design plans*

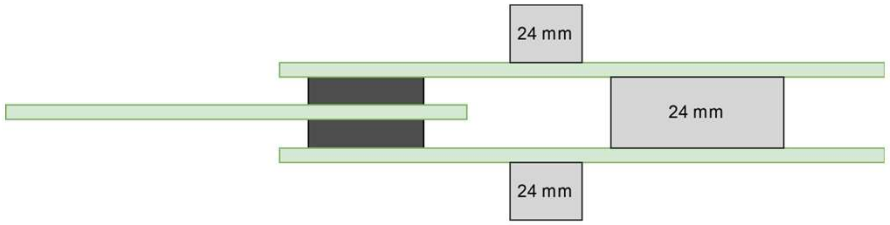
**FPGA Mezzanine Card** (**FMC**) is an ANSI/VITA (VMEbus International Trade Association) 57.1 standard that defines I/O mezzanine modules with connection to an FPGA or other device with re-configurable I/O capability.[1][2] It specifies a low profile connector and compact board size for compatibility with several industry standard slot card, blade, low profile motherboard, and mezzanine form factors.

High-pin count (HPC), 400 I/O FPGA Mezzanine Card (FMC) connectors
Top: mezzanine card side
Bottom: baseboard side

### Specifications [ edit ]

The FMC specification defines:[3]

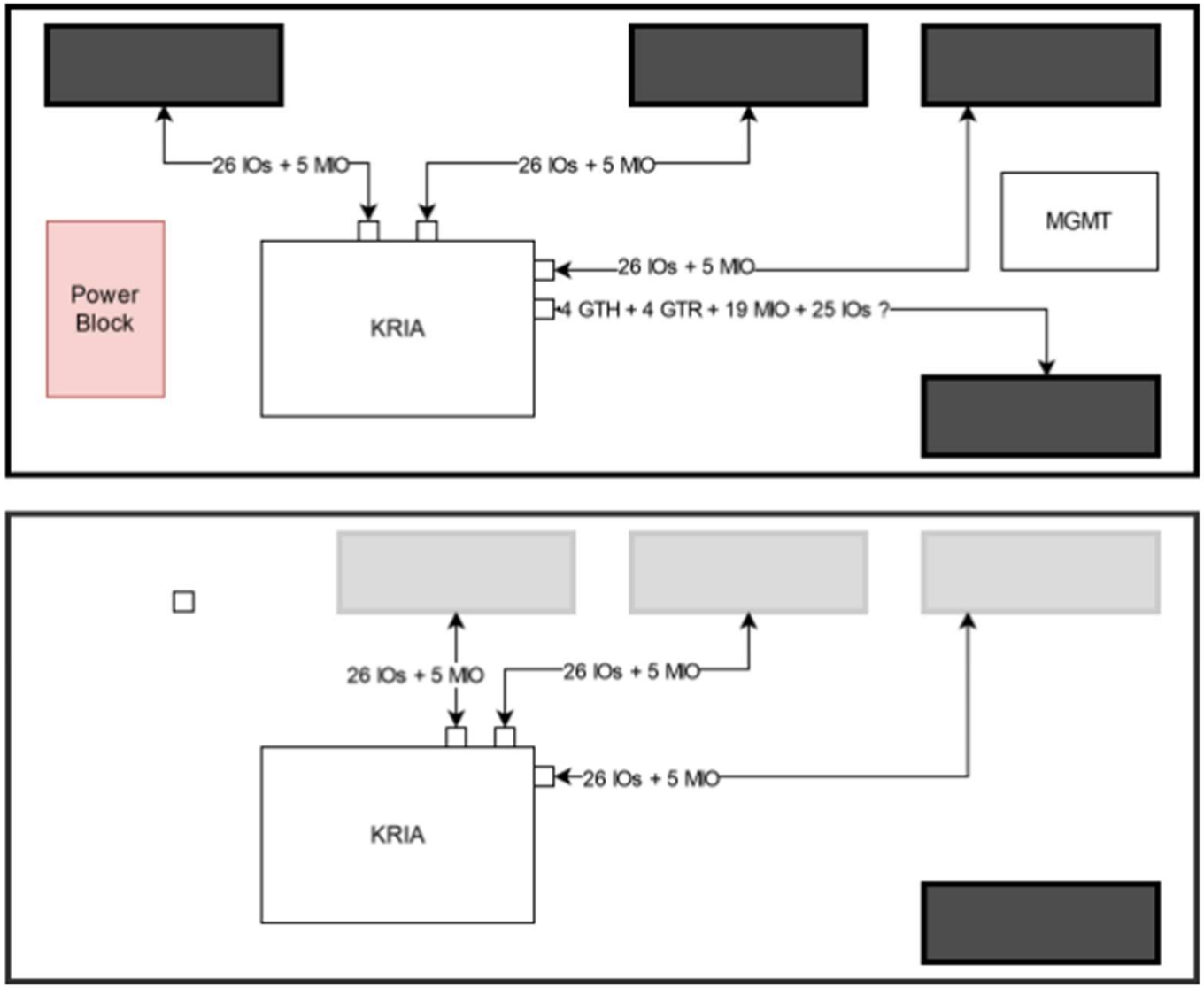
- I/O mezzanine modules, which connect to carrier cards
- A high-speed connector family of connectors for I/O mezzanine modules
  - Supporting up to 10 Gbit/s transmission with adaptively equalized I/O
  - Supporting single ended and differential signaling up to 2 Gbit/s
  - Numerous I/O available
- The electrical connectivity of the I/O mezzanine module high-speed connector
  - Supporting a wide range of signaling standards
  - System configurable I/O functionality
  - FPGA intimacy
- The mechanical properties of the I/O mezzanine module
  - Minimal size
  - Scalable from low end to high performance applications
  - Conduction and ruggedized support




The FMC specification has two defined sizes: single width (69 mm) and double width (139 mm). The depth of both is about 76.5 mm.[4] The FMC mezzanine module uses a high-pin count 400 pin high-speed array connector. A mechanically compatible low pin count connector with 160 pins can also be used with any of the form factors in the standard.

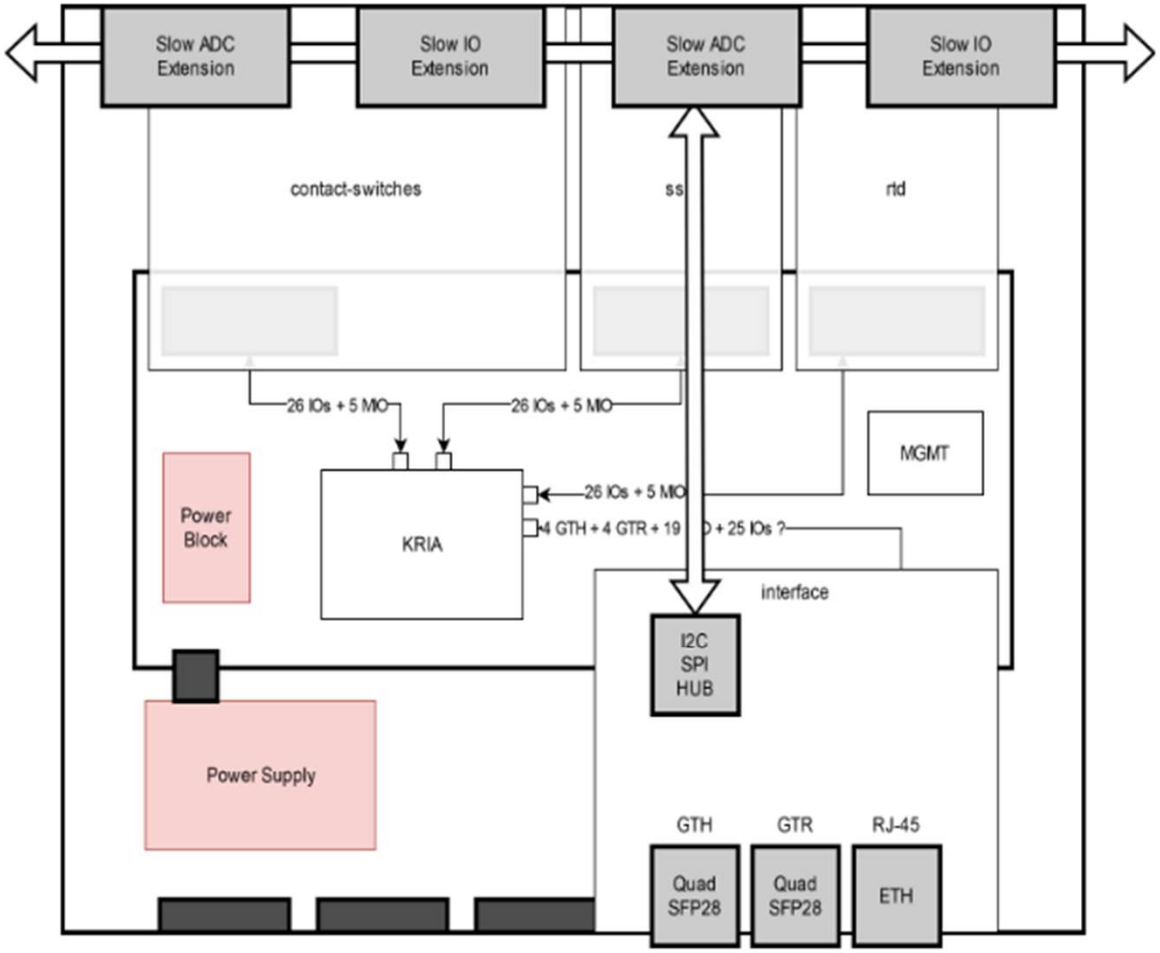
# First Plan for Full Scale Prototype

*Full scale design plans*



# First Plan for Full Scale Prototype

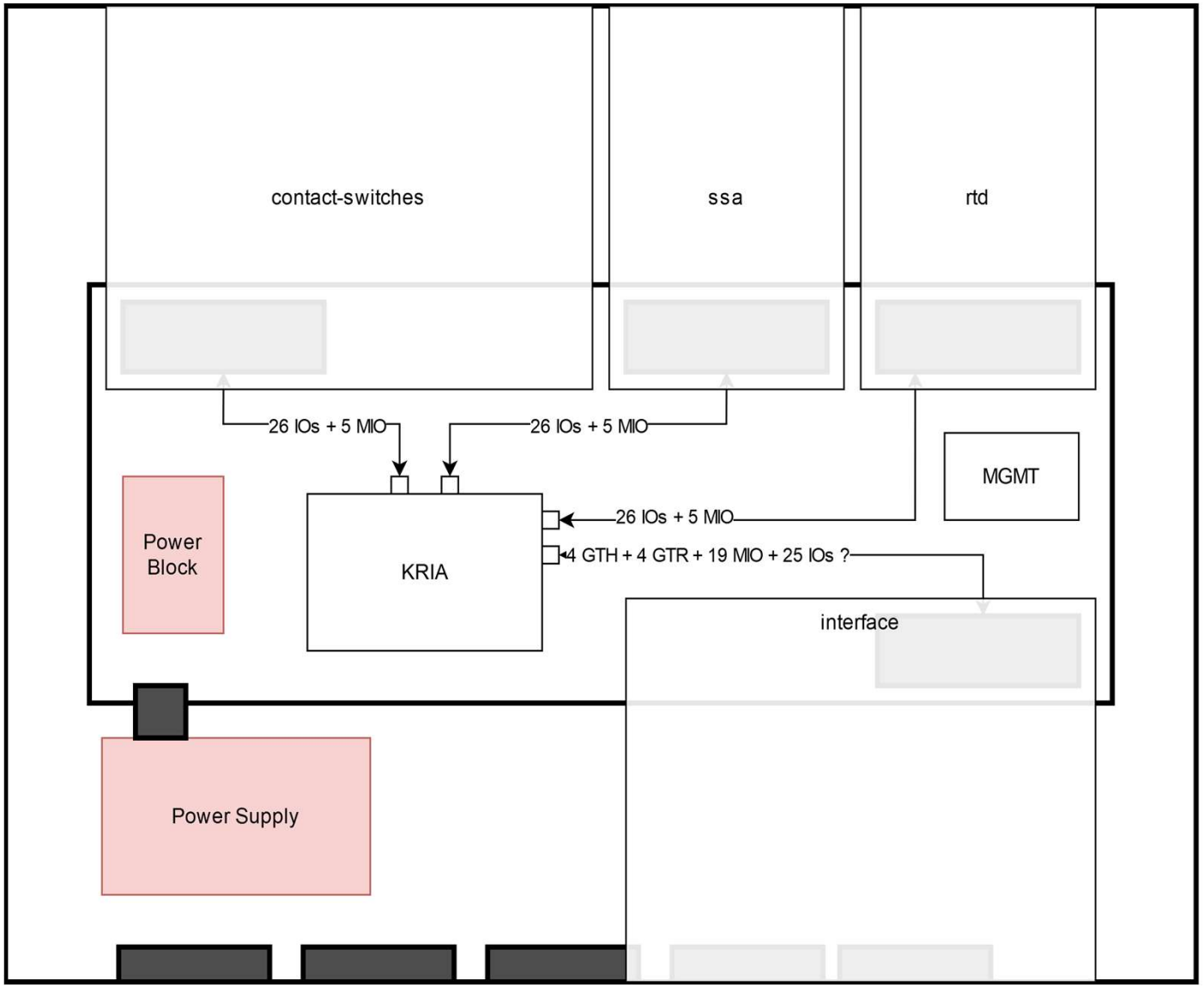
*Full scale design plans*



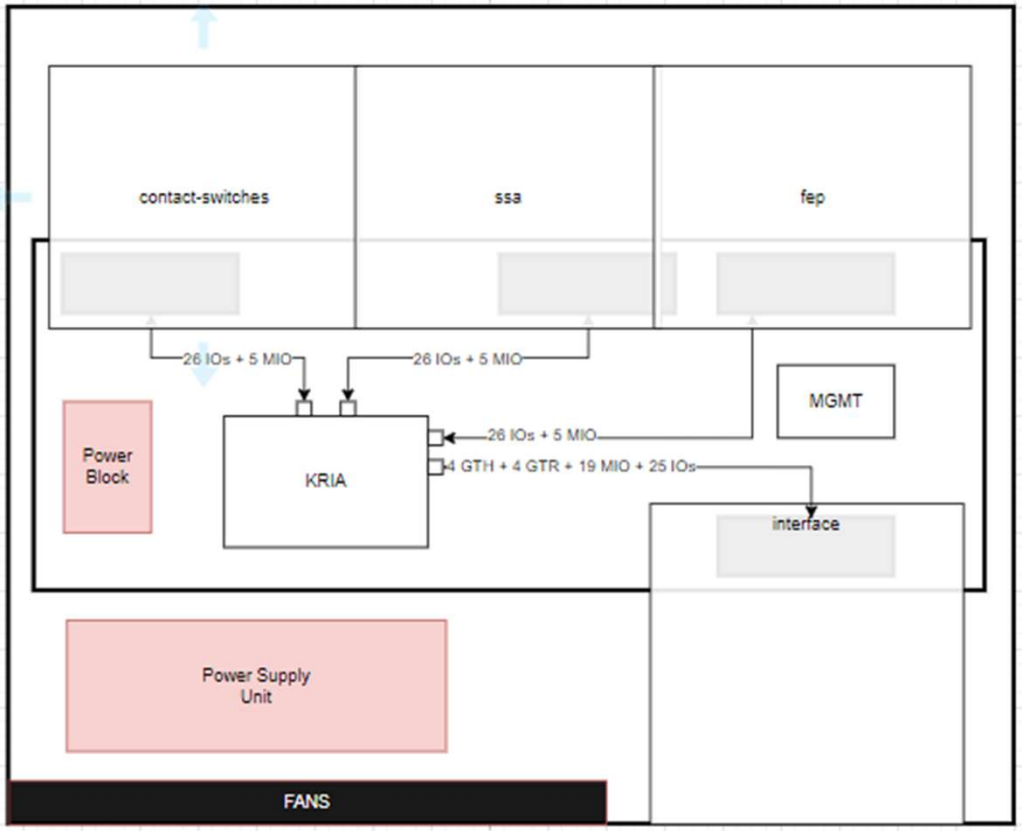

- Kria Carrier Board will be designed based on previous projects we did with Kria Module
- Conditioning Boards will be ported to FMC modules (and simplified)
  - Removal of expanders
  - Removal of one level of isolation
- Interface board will be designed as simple link pass-through module. No logic and/or complexty for first design
- Box power supply will be COTS in industiral standard

# Full Scale Prototype

*Initial view*



# Full Scale Prototype
## *Changes*




- Equal size of all boards
- Double FMC width of PCBs
- No direct connections of PCBs to Back panel – additional patch cables inside the box
- 6 FMC slots for conditioning boards
- 1 FMC slot for Interfaces

# Full Scale Prototype

## *Smart Units*


Ready to use module

- 4 GB DDR4 Memory (x64 1200 MHz)
- 16 GB eMMC
- 116 HP IOs + 69 HD IOs **(91 used)**
- 4x GTH (16 Gbps)
- 4x GTR (up to 5 Gbps ) ETH dedicated
- 49 “slow” ARM pins **(9 used)**

**Kria Module** still has some **spare pins** – we can increase pin allocation for each module to provide space for **future improvements and scaling**. Taking the **same amount of pins** for each module will make them **compatible** and **allow** easy **position exchange**

# Full Scale Prototype

*Smart Units*

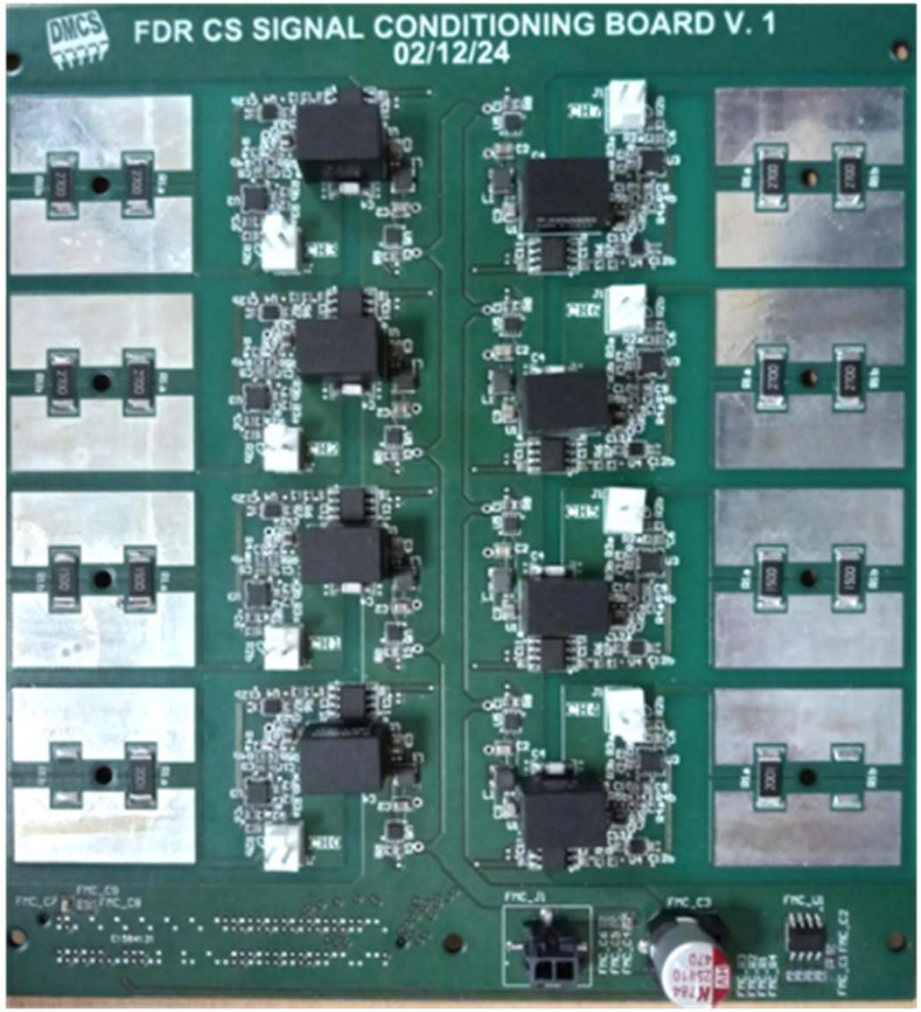
- Slow Management of the system
- Replaces Raspberry PI unit from POC
- Build Root Linux + Epics + IOC



- Easy to use – 1 power supply (+IO Supplies)
- Additional IO Capabilities
- Level Shifting
- Glue Logic
- Realtime functions
- Extends both management part and protection function parts`

# Full Scale Prototype

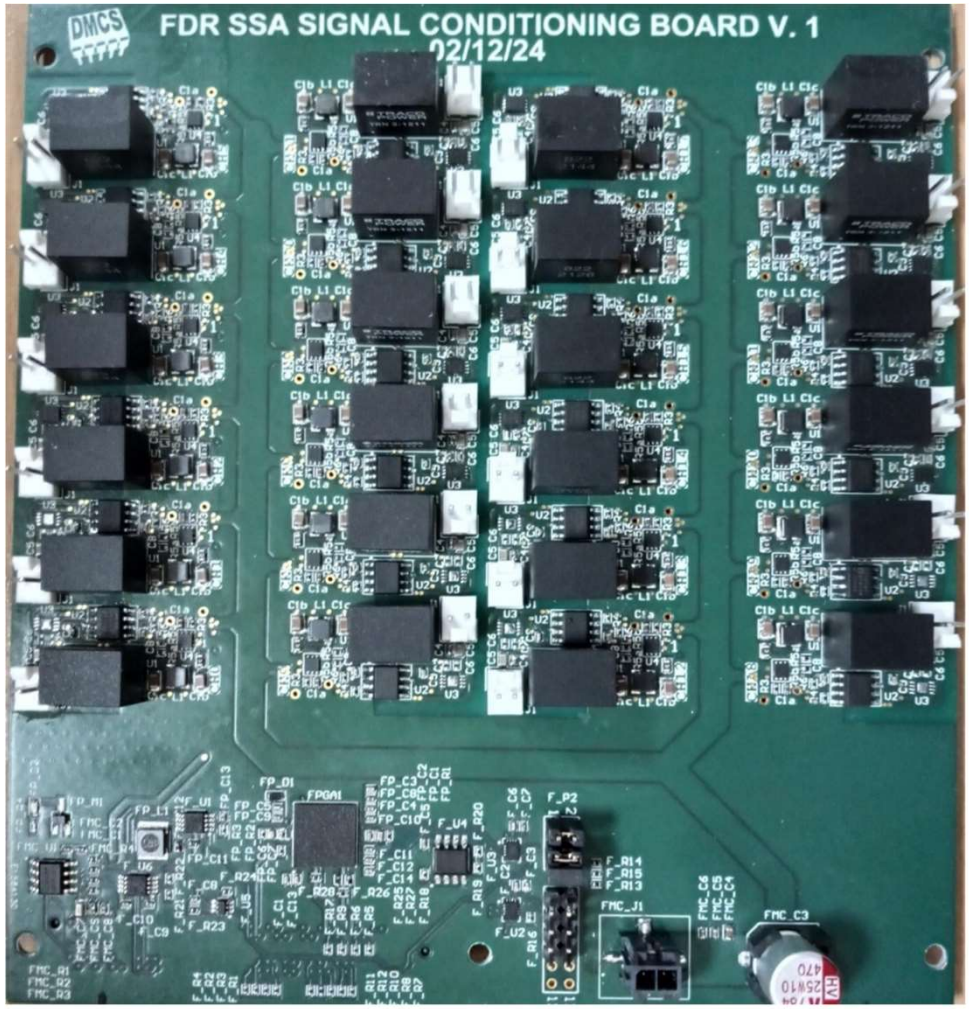
## *Contact Switch Conditioning Board*




- 8 channels for contact switches
- Built in diagnostics
- Channel to channel isolation
- Assembly Variants to use 12/24V outputs
- Individual Channels can be powered off when needed

# Full Scale Prototype

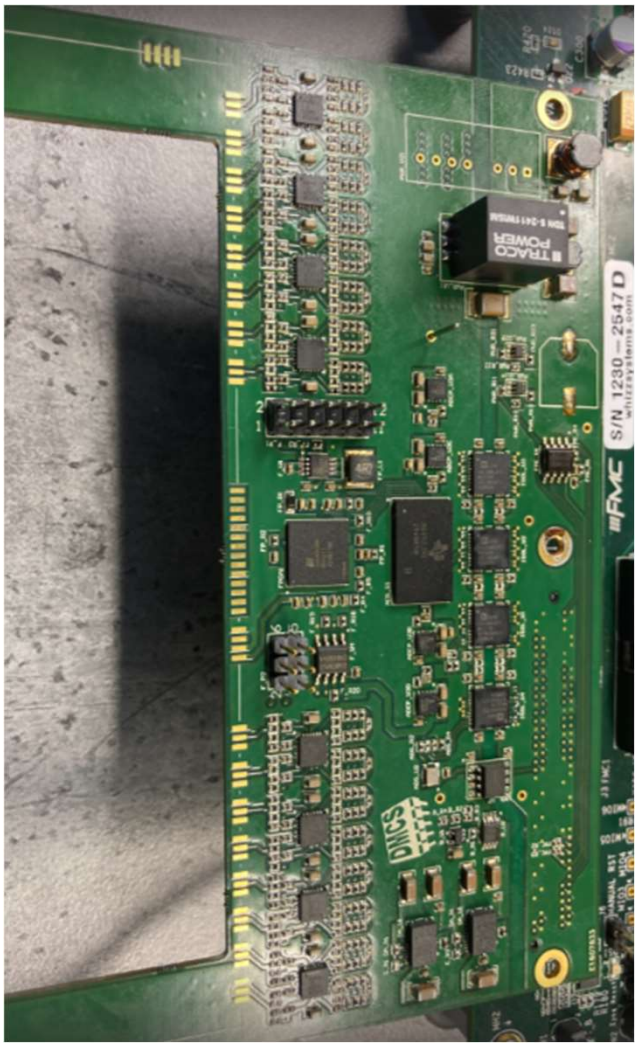
## *SSA Conditioning Board*




- 24 digital channels (5V – capable of driving 50R loads)
- Channel to channel isolation
- Assembly Variants to configure each channel as in or out
- Built in fuses and diagnostics
- Individual Channels can be powered off when needed
- Lattice FPGA used as IO expander

# Full Scale Prototype

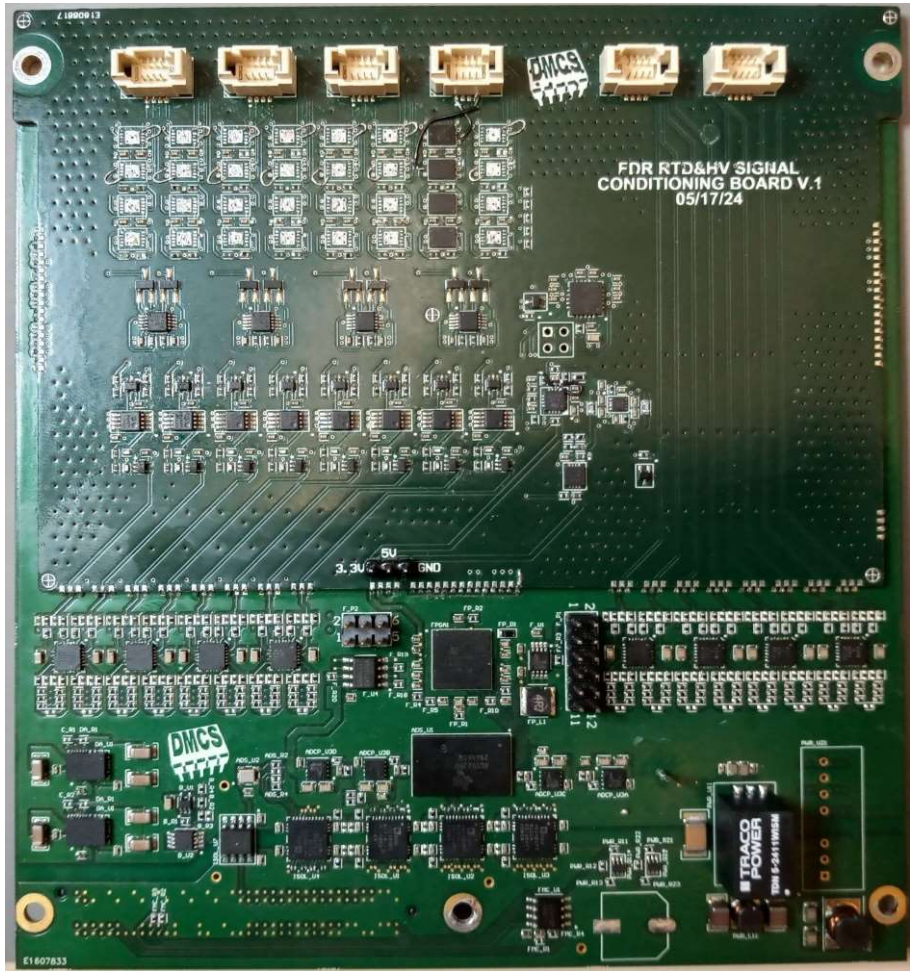
*ADC module*



- 16 analog input channels (14 bits – 30 MHz max for each)
- Isolated inputs
- Assembly Variants to configure voltage span and bandwith per channel
- Lattice FPGA used as IO expander and manager

# Full Scale Prototype

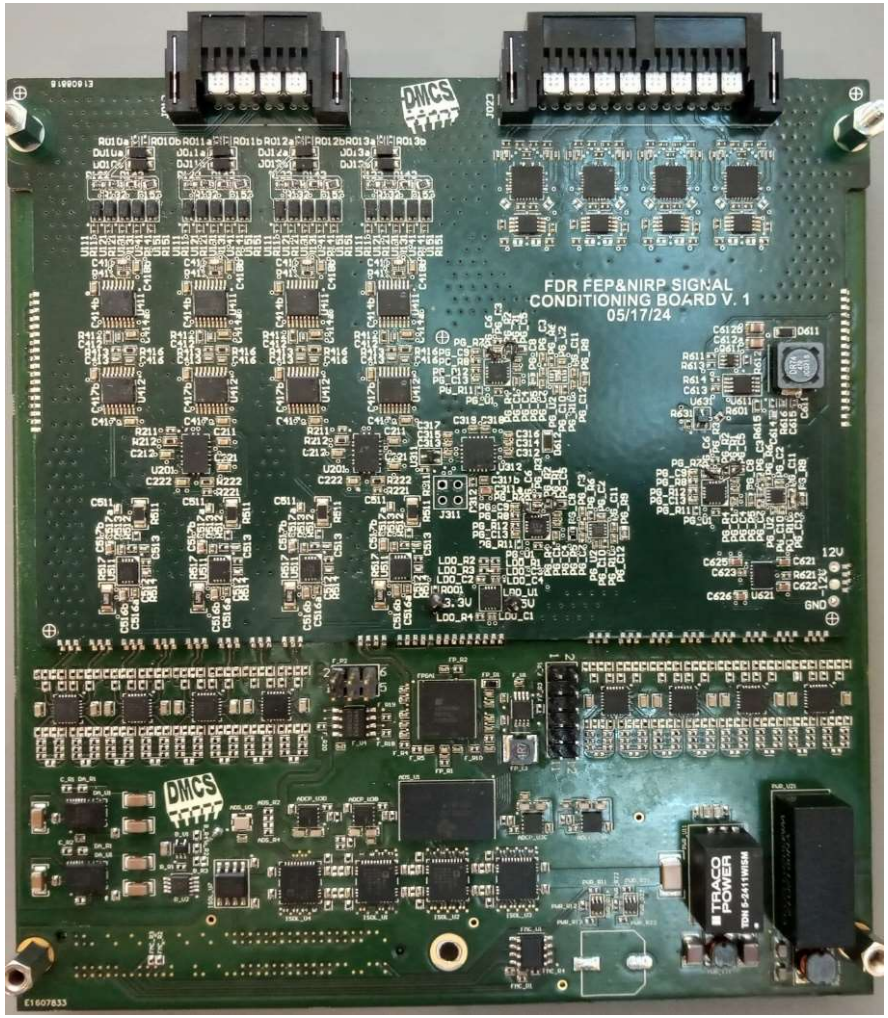
## *RTD/General Purpose*




- 8 RTD dedicated channels
- 8 general purpose channels (dedicated for HV monitoring and all others)
- Built in calibration and diagnostics
- Managed from ADC board

# Full Scale Prototype

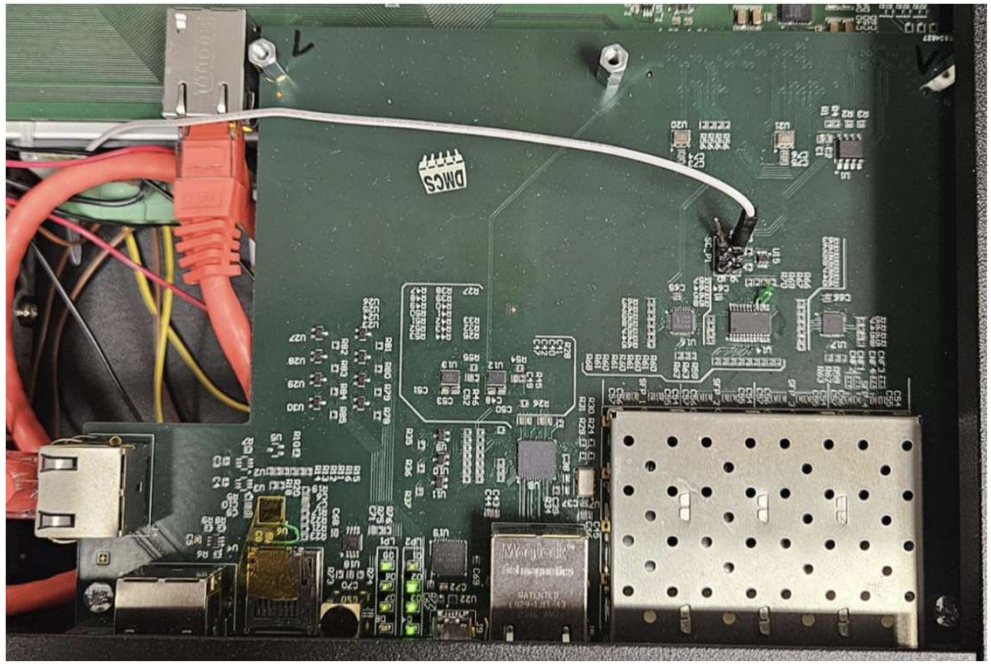
## *FEP/NIRP Board*




- 8 FEP dedicated channels with bias
- 8 RF power detector channels (for NIRP/all other RFs needed)
- Built in calibration and diagnostics
- Managed from ADC board

# Full Scale Prototype

*Interface Board*



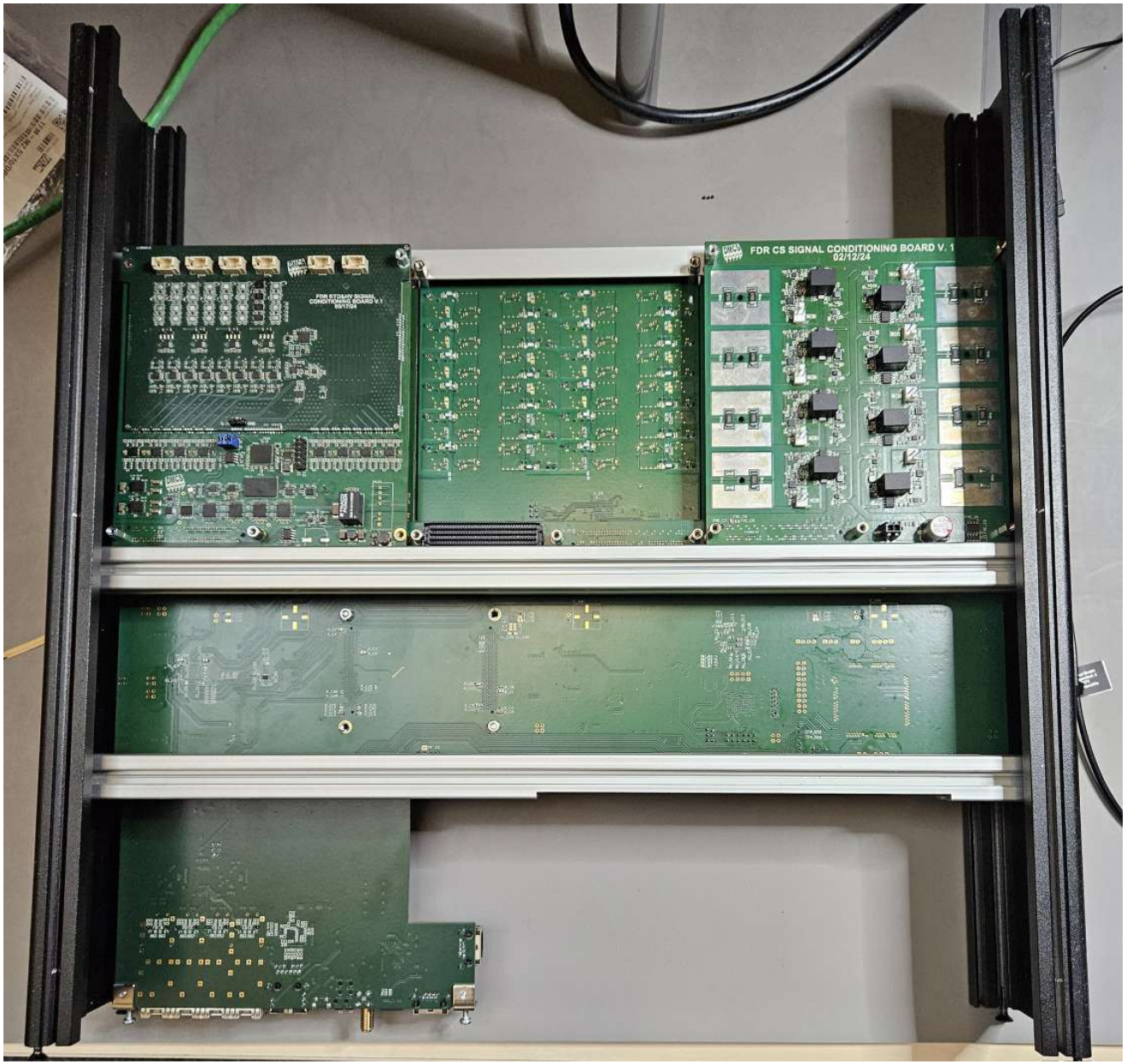
- Ethernet for K26 and management SOM
- 4 SFP+ modules for links to external systems
- Clock input
- LEDs + UART

# Full Scale Prototype

## *Top View*

# Full Scale Prototype

*Bottom View*



# Summary

*What was done and what is needed*

- Concept
- Specification
- Design
- Prototype production
- First batch production

Identified some problems on different levels, but they are minor ones with limited influence on performance. Each of them will be addressed in next revision of the system

# Thank You !

*Thank You !*