Main logic realization/execution HW

Piotr Amrozik

About Us

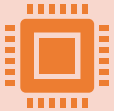
Piotr Amrozik

Ph.D. in Electrical Engineering

Role

RFPI project contractor

Hardware engineer



Relevant experience

FastLogic Sp. z o.o.: FPGA prototyping, timing and synchronization, cryptography and hash algorithms (2020-2021)

ARUZ Large-scale, FPGA-based Analyzer of Real Complex Systems: project contractor

ASIC/FPGA/hardware engineer (since 2007)

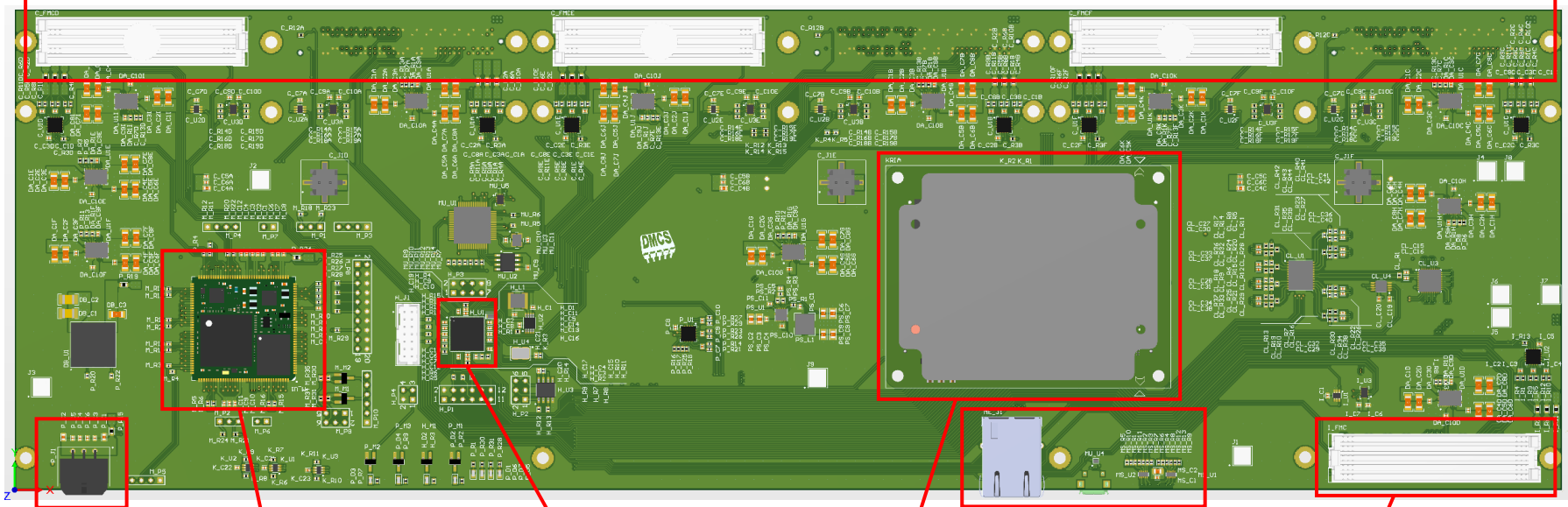
Agenda

- The main Kria based carrier module
  - Overview
  - The main logic components
- The Kria interface FMC module
  - Requirements
  - Design
  - Block diagram
  - Interface distribution
  - Manufacturing and postproduction testing

The main Kria based carrier module overview

Board dimensions:
419 x 130 mm

LPC FMC Connectors 3x top side, 3x bottom side for 6x double-sized FMC modules



Main power input (12V)

MGMT SOM (SAM9X60D1G-I/LZB)

FPGA Lattice (ICE40HX8K-BG121)

Kria K26 SOM

MGMT SOM Ethernet and SD card connectors

HPC FMC Connector for interface module

The main logic components roles (in brief)

- MGMT SOM role:
  - Management of:
    - system health
    - system status
    - control of FMC modules and Kria power supplies with their measurements (realized with INA3221AIRGVR chip)
  - Kria K26 SOM configuration and UART access (realized with FTDI chip)
- Kria K26 SOM role:
  - Data acquisition and processing from all FMC conditioning modules
- Lattice FPGA role:
  - JTAG hub to all FMC modules and Kria K26 SOM

MGMT SOM (SAM9X60D1G-I/LZB)

System-In-Package including:

- ARM926EJ-S Arm Thumb processor running up to 600 MHz
- 1-Gbit DDR2-SDRAM
- 4-Gbit NAND Flash Memory
- On-Board Power Management Unit (MCP16501TA-E/RMB)
- 1-Kbit Serial EEPROM with EUI-48™ Node Identity (24AA025E48T-I/OT)
- 10Base-T/100Base-TX Ethernet PHY (KSZ8081RNAIA-TR)
- One High-Speed USB Device, Three High-Speed USB Hosts with Dedicated On-Chip Transceivers
- 85 I/Os
- 28 x 28 mm Module, 0.65-mm Pitch, Manually Solderable for Prototyping

FPGA Lattice ICE40HX8K-BG121

- FPGA Lattice ICE40 family

Part Number	LP384	LP640	LP1K	LP4K	LP8K	HX1K	HX4K	HX8K
Logic Cells (LUT + Flip-Flop)	**384**	**640**	**1,280**	**3,520**	**7,680**	**1,280**	**3,520**	**7,680**
RAM4K Memory Blocks	0	8	16	20	32	16	20	32
RAM4K RAM bits	0	32K	64K	80K	128K	64K	80K	128K
Phase-Locked Loops (PLLs)	0	0	1[1]	2[2]	2[2]	1[1]	2	2
Maximum Programmable I/O Pins	63	25	95	167	178	95	95	206
Maximum Differential Input Pairs	8	3	12	20	23	11	12	26

Source: FPGA-DS-02029-4-2-iCE40-LP-HX-Family-Data-Sheet.pdf
https://www.latticesemi.com/view_document?document_id=49312

The Kria interface FMC module - requirements

- 1GB/s Ethernet for Kria with SGMII
- SD card for Kria
- 4xSFP cage for Kria GTH/GTR
- Two clock generators for GTH and GTR 125MHz reference clocks
- External clock input for Kria via SMA connector
- 8 status LEDs driven by Kria GPIOs
- Debug UART for MGMT
- MGMT SOM Ethernet panel interface

The Kria interface FMC module - design

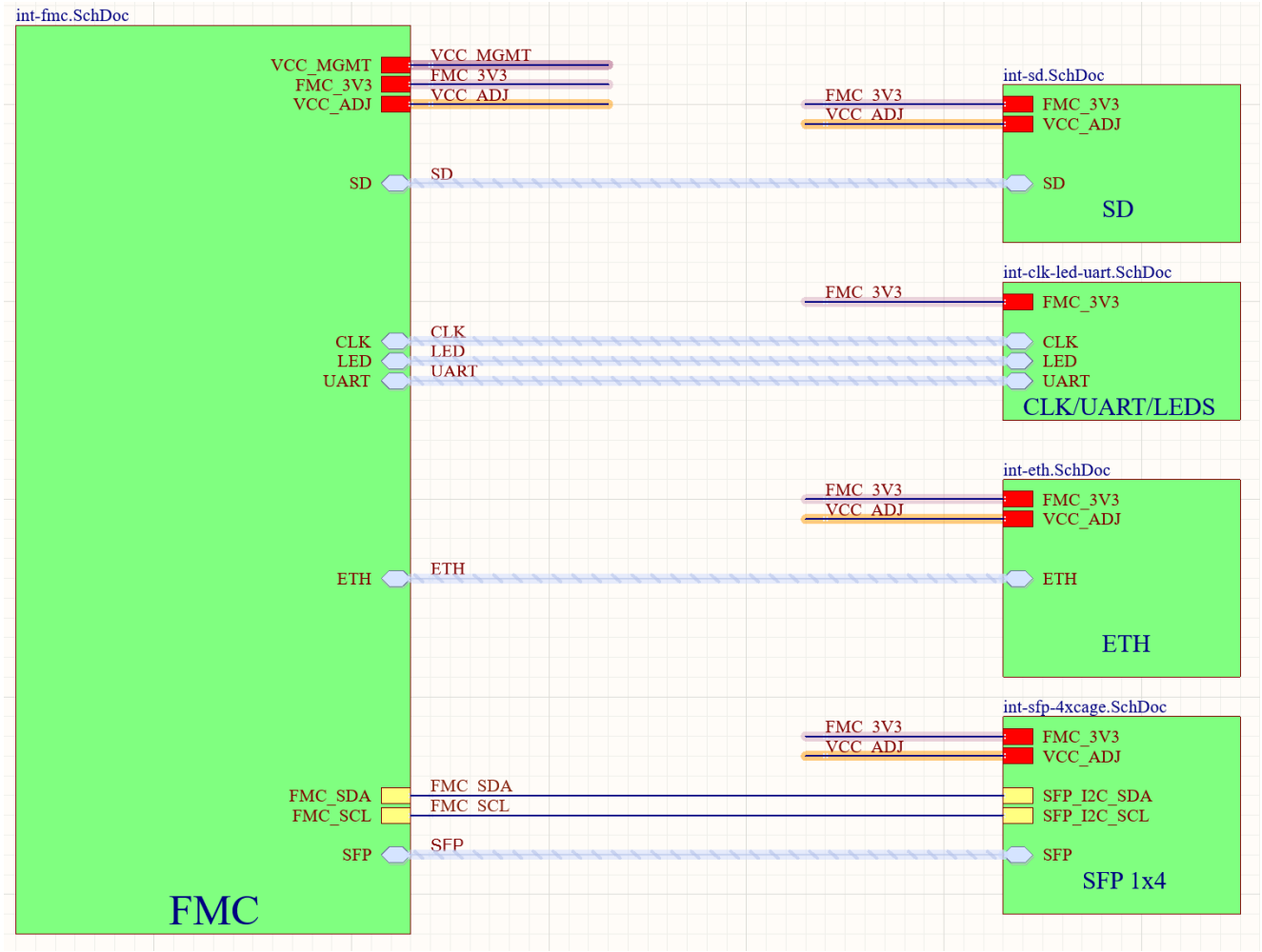
Components decision:

- HPC FMC Mezzanine connector (ASP-134602-01)
- SGMII Ethernet PHY (TI DP83867CSRGZT) for Kria (1xGTR)
- MicroSD card connector for KRIA
- 4xSFP cage (3xGTH; 1xGTH with option to substitute with 1xGTR)
- GTH/GTR 125MHz reference clocks (NX33C5008Q)
- Clock input: CLK0_M2C driven externally via SMA connector
- 8 status LEDs: 2x 4xLIGHTPIPE (utilizes 8 KRIA GPIOs)
- Micro USB connector: MGMT debug UART (Maxlinear XR21B1422)
- 100MB/s Ethernet RJ-45 connector for MGMT SOM

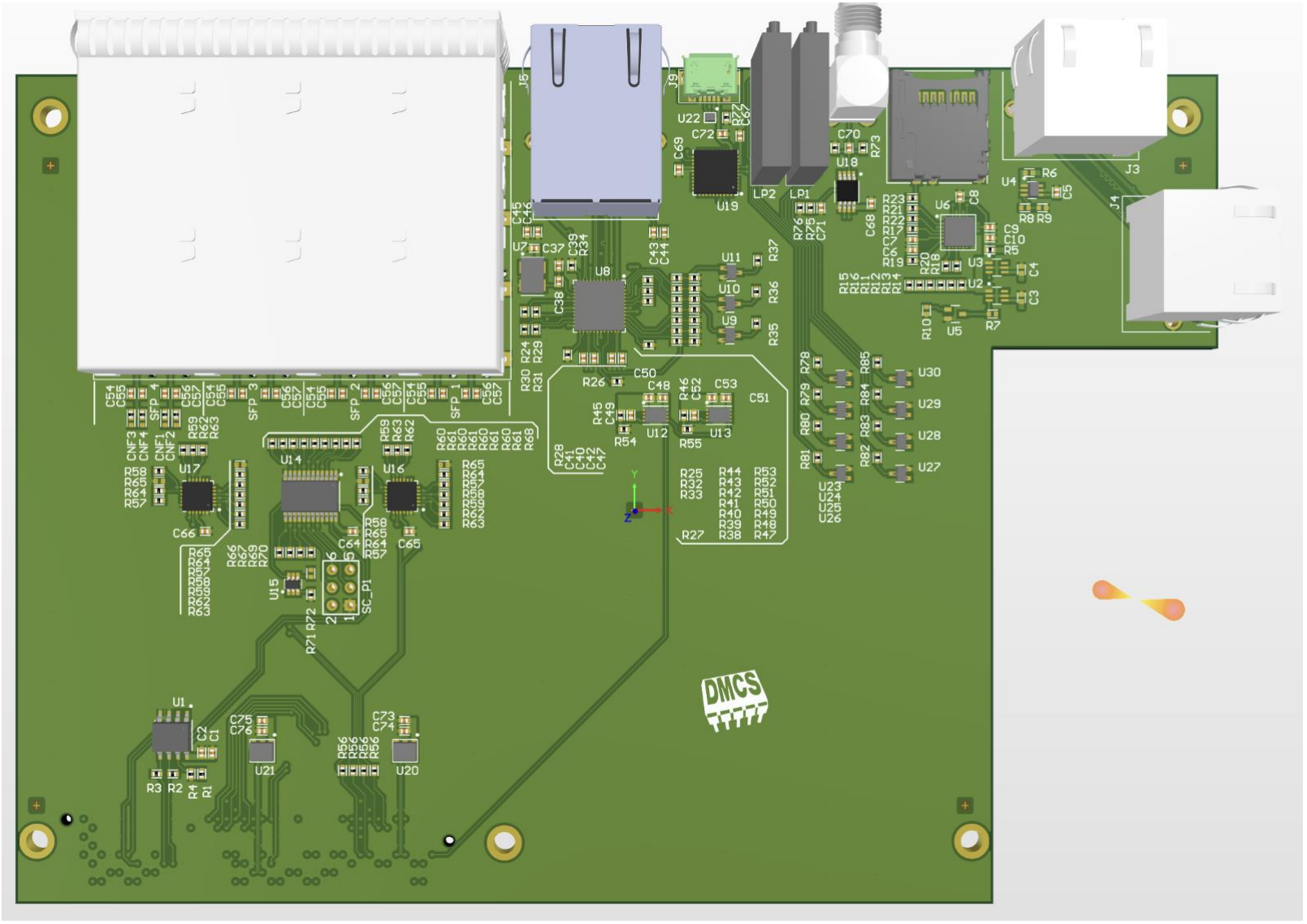
Mechanics:

- 2x FMC module with modified shape (to simplify MGMT SOM Ethernet interfacing to front-panel)

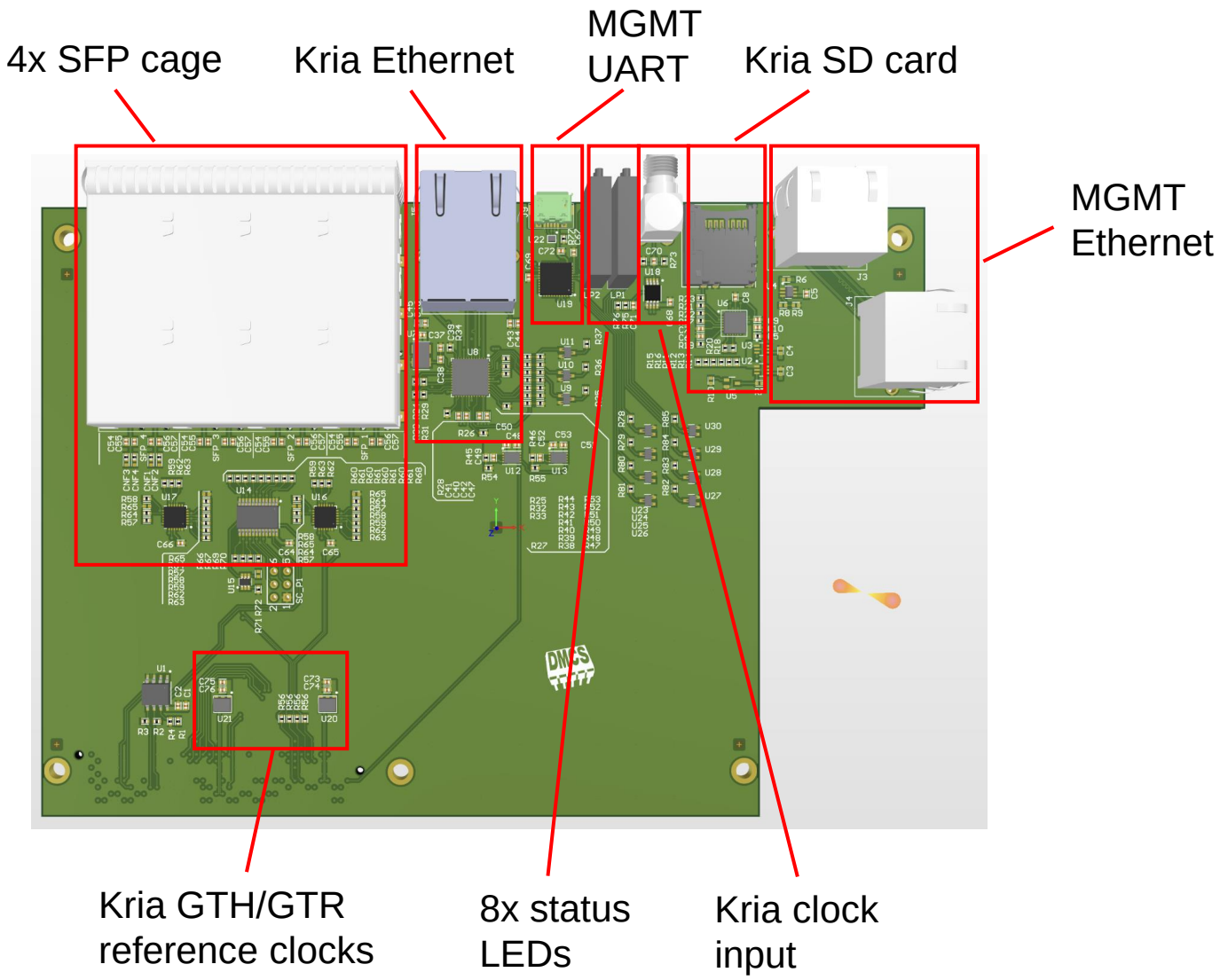
The Kria interface FMC module – block diagram



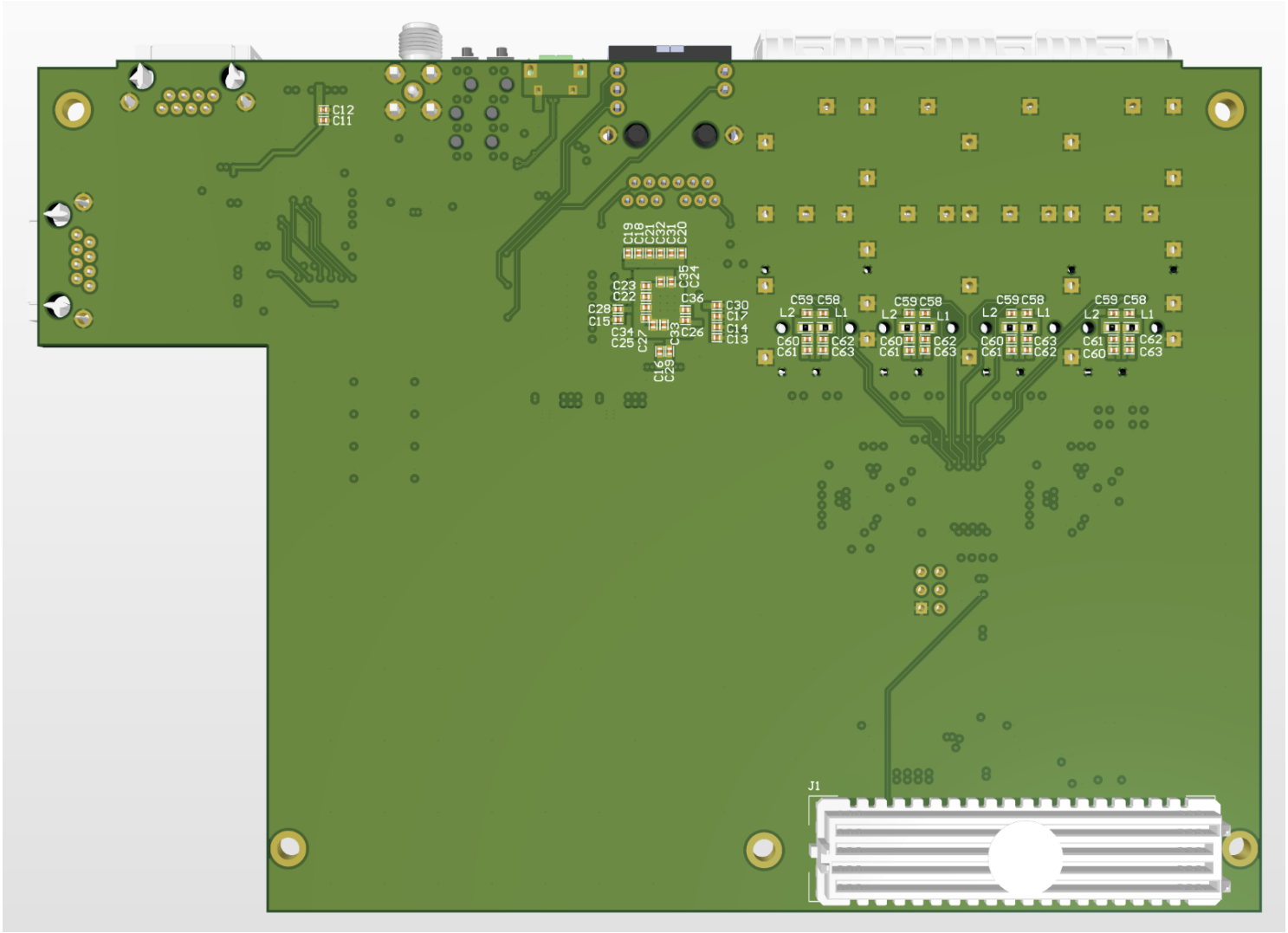
The Kria interface FMC module – 3D model (top)



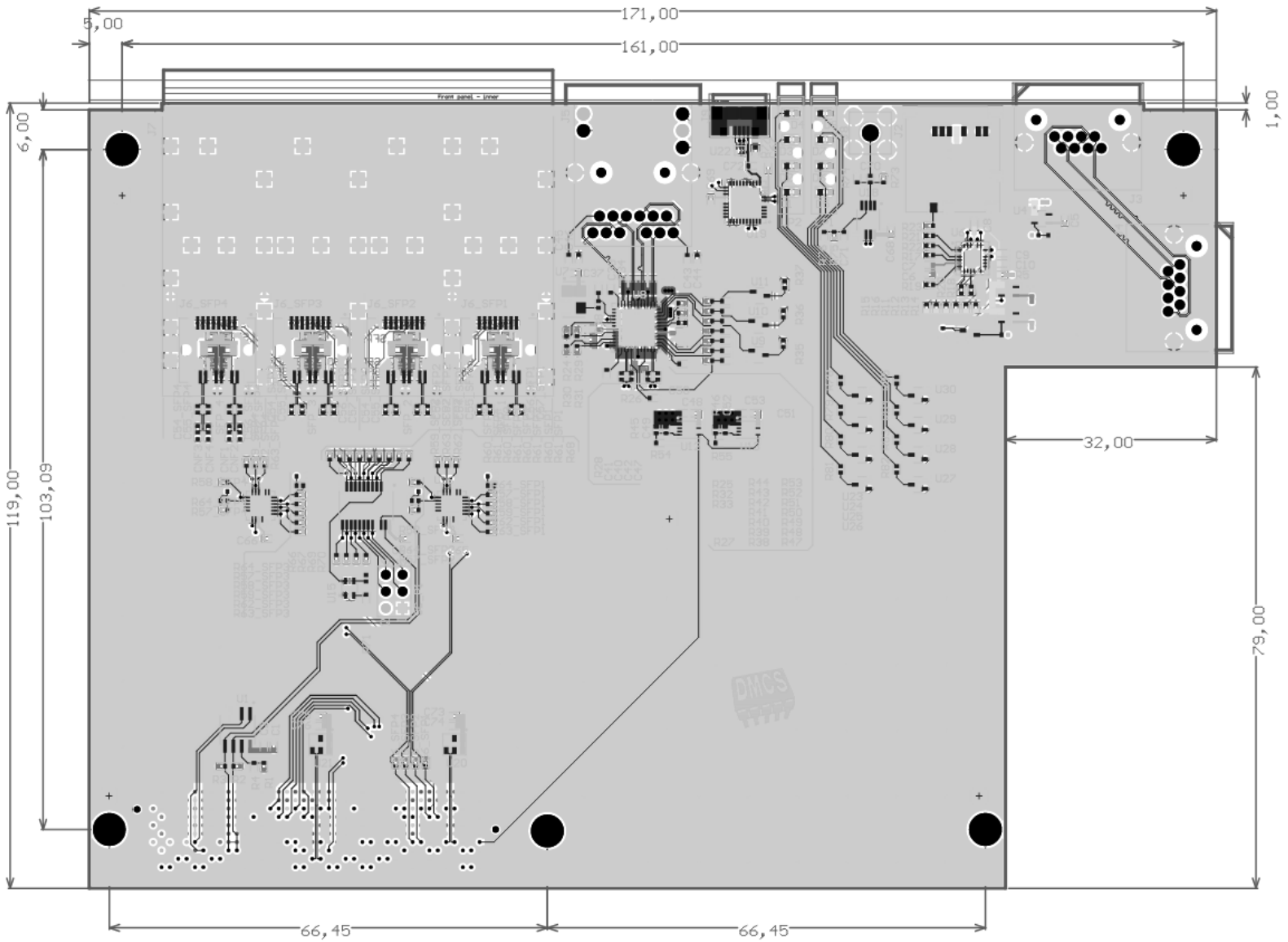
The Kria interface FMC module – 3D model (top)



The Kria interface FMC module – 3D model (bottom)

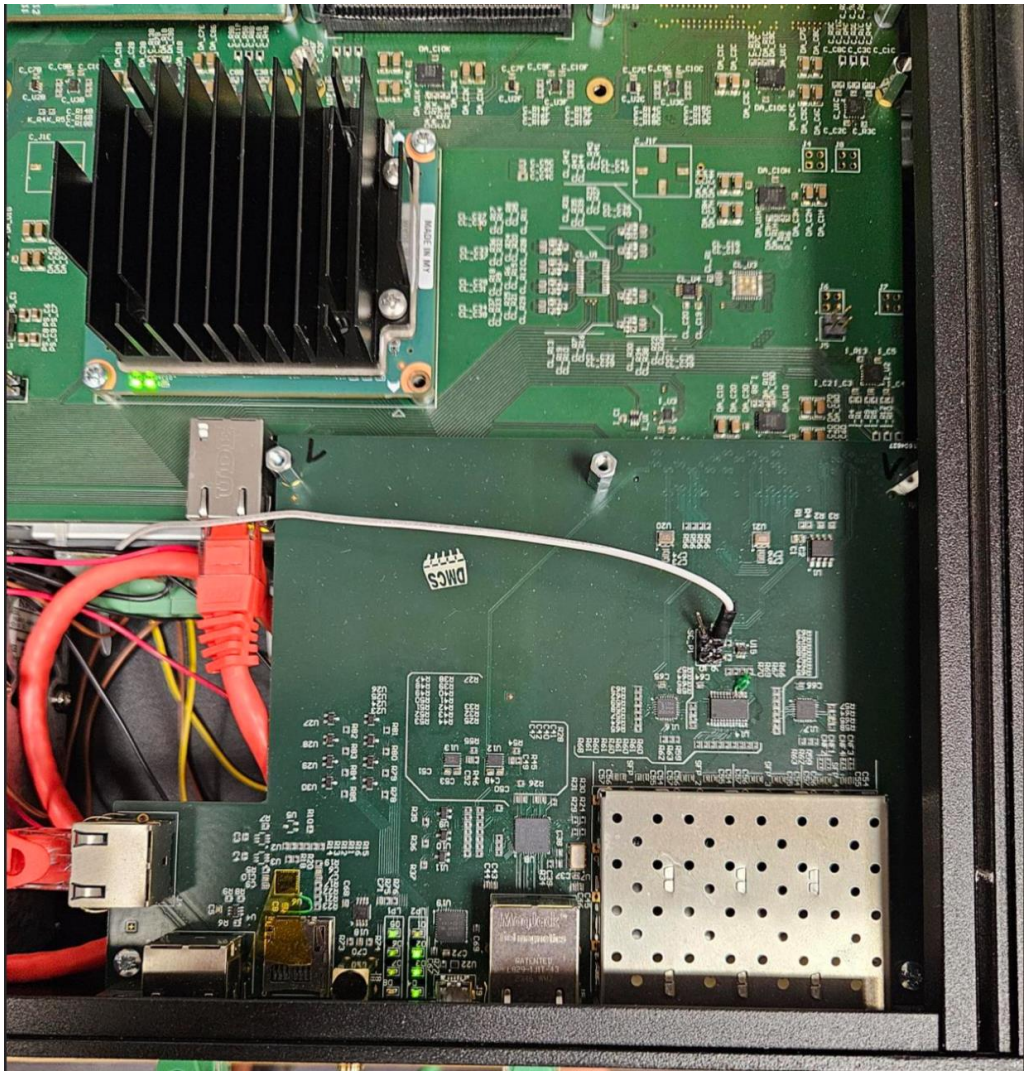


The Kria interface FMC module – board mechanics



The Kria interface FMC module – manufacturing

- 2 modules assembled in-house



The Kria interface FMC module – postproduction testing

- 1GB/s Ethernet for Kria with SGMII
- SD card for Kria
- 4xSFP cage for Kria GTH/GTR
- External clock input for Kria via SMA connector
- Two clock generators for GTH and GTR 125MHz reference clocks
- 8 status LEDs driven by Kria GPIOs
- Debug UART for MGMT
- MGMT SOM Ethernet front-panel interface

Thank you for your attention