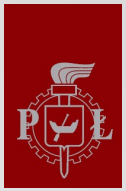


# RFPI System Design overview

Wojciech CICHALEWSKI on behalf of DMCS team

# About us

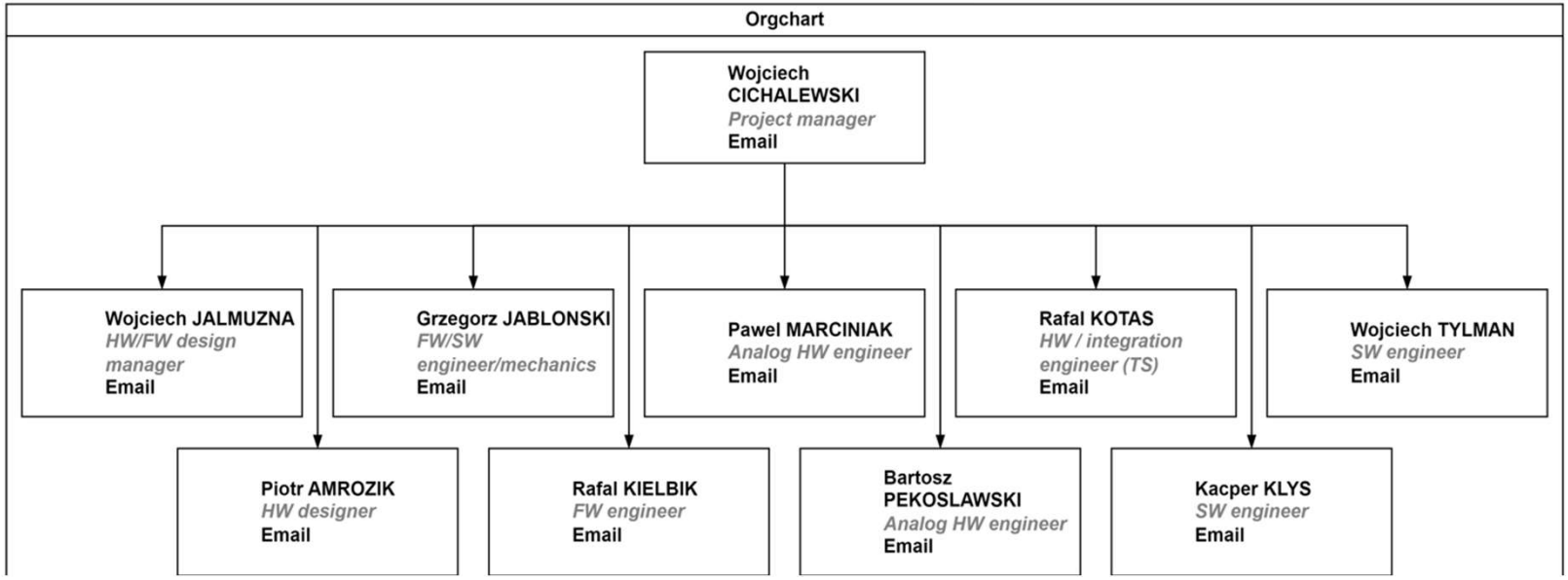
## Wojciech CICHALEWSKI

Ph.D. in Electrical Engineering

**Role**:

- TUL in-kind for PIP-II technical coordinator,
- Local RFPI project Manager.

**Organization**:

# About me

**Wojciech CICHALEWSKI**

Ph.D. in Electrical Engineering

## Role:

- TUL in-kind for PIP-II technical coordinator,
- Local RFPI project Manager.

## Relevant Experience:

LLRF: FLASH, E-XFEL, ESS-ERIC (elliptical cavities), PolFEL

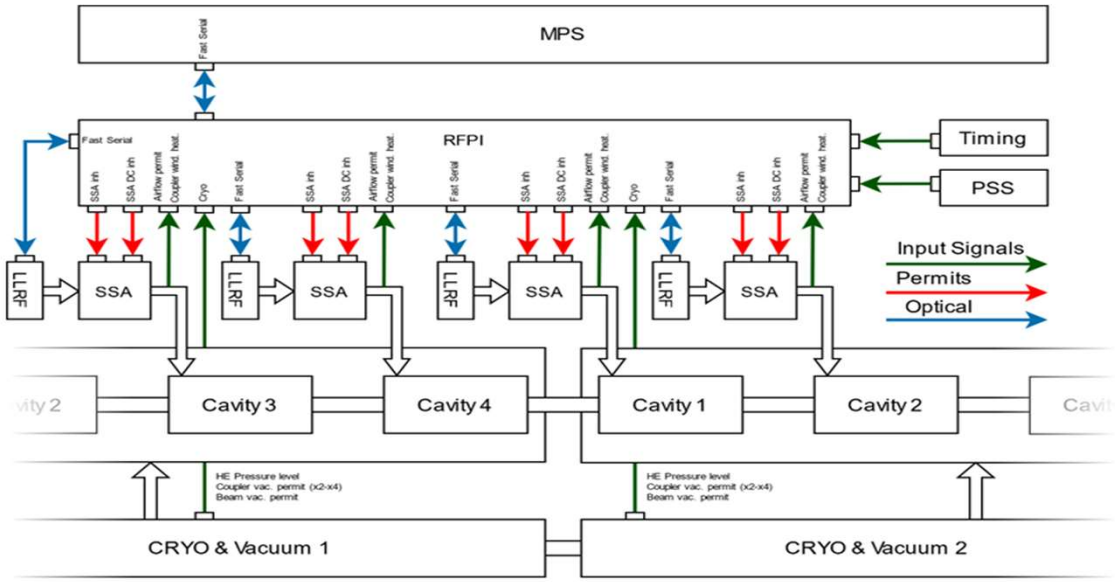
Technical coordinator of the DMCS- TUL accelerator related projects as LLRF Group leader (2010 – present)

DESY: Automation and software engineer in LLRF system development (2002-2019),

ESS-ERIC: PEG project „LLRF systems” manager deputy, System engineer – local LLRF system test-stand preparation, operation and updates (2016-present),

# The RFPI system design - requirements

| Signal Name | Quantity |
|---|---|
| Field Emission Probe (FEP) | 1 per cavity/coupler |
| Coupler Bias Current (A) | 1 per cavity/coupler |
| Coupler Bias Voltage (V) | 1 per cavity/coupler |
| RF antenna (NIRP) | 1 per cavity/coupler + 1 per CRYOMODULE |
| Cryo (He Pressure & Level) Permit | 1 per CRYOMODULE |
| Coupler Airflow Permit | 1 per cavity/coupler |
| Coupler Vacuum Permit | 1 per cavity/coupler |
| Beam Vacuum Permit | 1 per CRYOMODULE |
| Personnel Safety Permit | 1 per cavity/coupler |
| Coupler Temperature Probe RTD 1 | 1 per cavity/coupler |
| Coupler Temperature Probe RTD 2 | 1 per cavity/coupler |
| LLRF Ready (RF level status, Ready status, quench) | 1 per cavity/coupler |
| SSA Ready | 1 per cavity/coupler |
| SSA Permit Out | 1 per cavity/coupler |
| SSA DC Permit Out | 1 per cavity/coupler |
| LLRF Permit Out | 1 per cavity/coupler |
| MPS Permit Out | 1 per cavity/coupler |




| | Output Permits from RFPI (LB/HB) | | | |
|---|---|---|---|---|
| Inputs to RFPI | LLRF permit | SSA Permit | SSA_DC Permit | MPS |
| FEP | x | | | x |
| RF antenna (NIRP) | x | x | | x |
| Personnel Safety Permit | x | x | | x |
| Vacuum Status | x | x | | x |
| Coupler Vacuum Permit (Multipacting) | | | | x |
| He Level & Pressure (Cryo) | x | x | | x |
| Temperature Sensors (RTD 1& 2) | x | x | | x |
| Coupler Airflow Sensor | x | x | | x |
| HV Coupler Bias voltage | x | x | | x |
| HV Coupler Bias current | x | x | | x |
| SSA Ready | x | | | x |

# The RFPI system design - requirements

| Source | Signal | Function | Specifications |
|---|---|---|---|
| FEP | analog | limit for coupler field emissions | TTL into 50 ohms |
| Stray RF Detection (NIRP) | analog RF/162.5-1300 MHz | Limit for non-ionizing radiation | Sine, 0 dBm into 50 ohms |
| Personnel Safety Permit | contact switch | Personnel safety system permit | Permit drops when metal contact switch is open |
| Vacuum Status | contact switch | Vacuum permit | Permit drops when metal contact switch is open |
| Coupler Vacuum gauge | contact switch | Vacuum permit | Permit drops when metal contact switch is open |
| Cryogenics Status | contact switch | Cryogenics permit | Permit drops when metal contact switch is open |
| Temperature Sensors (RTD 1 & 2) | Analog | Window temperature | 0-10V |
| Coupler Airflow Sensor | contact switch | Coupler airflow permit | Permit drops when metal contact switch is open |
| HV Coupler Bias voltage | analog | Limit for power supply levels | 0-10V signal |
| HV Coupler Bias current | analog | Limit for power supply levels | 0-10V signal |
| SSA Ready | digital | HLRF permit | TTL into 50 ohms |
| LLRF Status | digital | LLRF system permit | High-speed serial link |

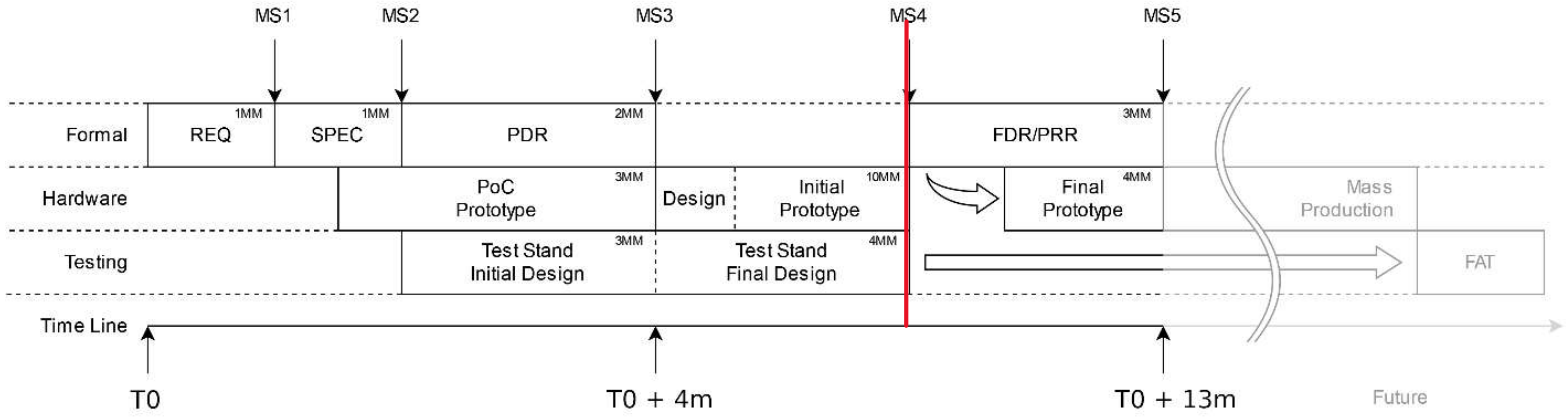
| Destination | Signal | Function | Specifications |
|---|---|---|---|
| SSA | digital output | Permit | TTL into 50 ohms |
| SSA DC | digital output | Permit | TTL into 50 ohms |
| LLRF System | digital output | Permit | TTL into 50 ohms |
| MPS System | digital output | Permit | TTL into 50 ohms |

# RFPI system design flow

New design of the RFPI system.

Three system prototypes version before mass production:

- **Proof of Concept prototype,**
- Initial Prototype – Full Scale Prototype (current version),
- Final Prototype,



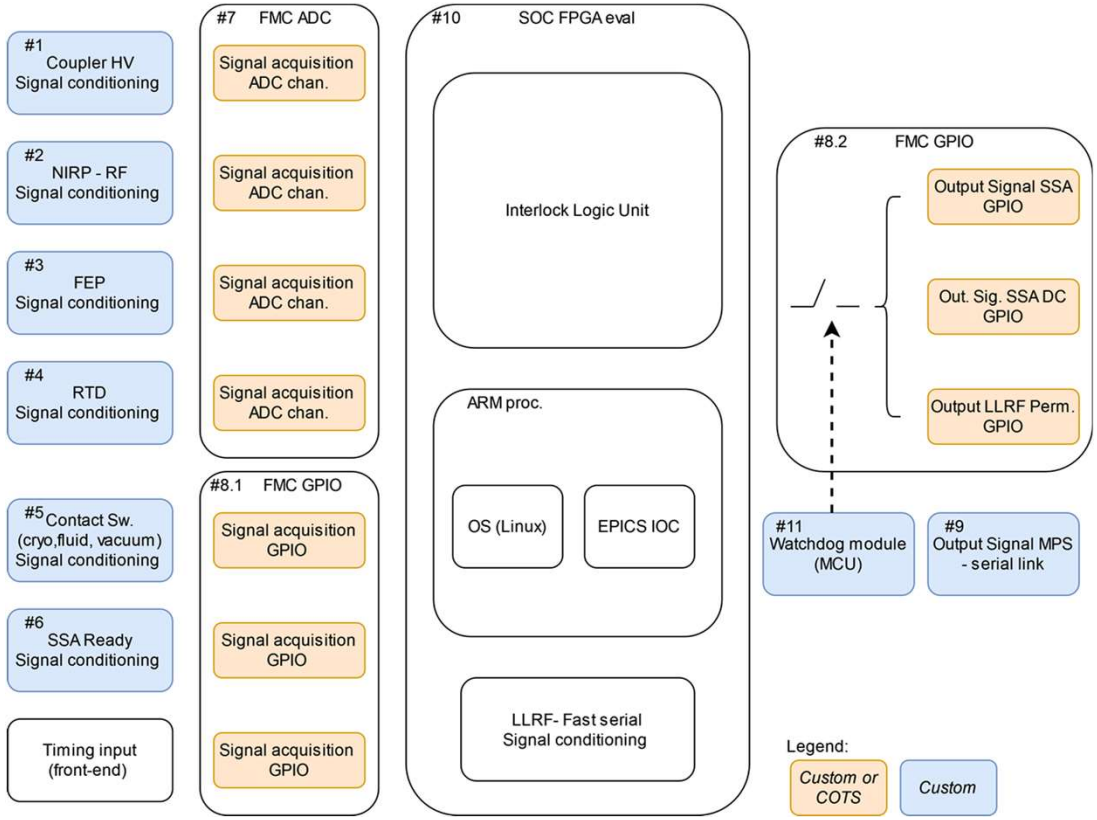
# The Proof of Concept prototype

PoC **scope (**according **to SOW)**:

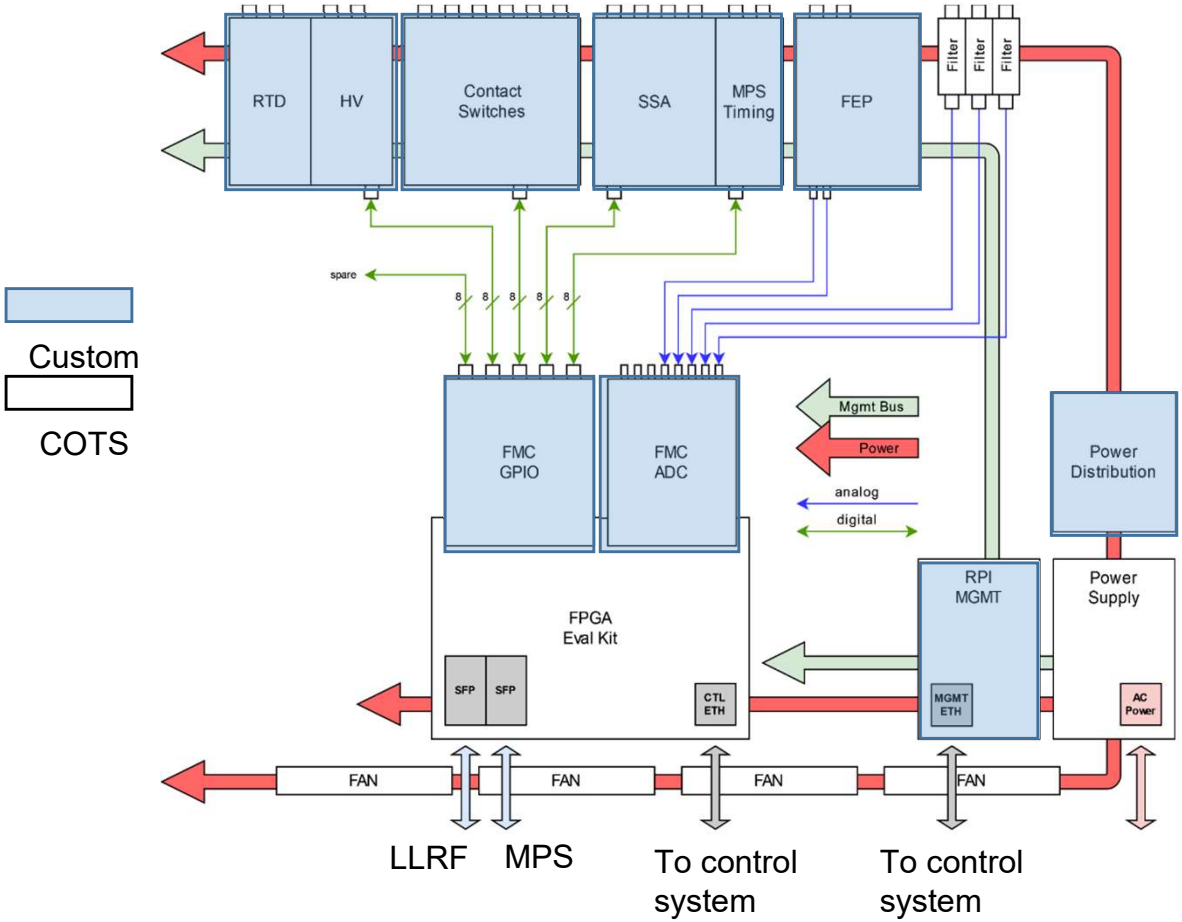
- Design and Production of Test Board for each type of external interface present in the system.
- Design and Production of Test Board for selected internal features, which will be identified as requiring detailed verification.
- Implementation of dedicated system logic (e.g. firmware blocks) to interface with the Test Boards.
- Preparation of dedicated test and measurement plans for each element of the PoC.
- Execution of measurement plans to verify electrical properties, delays, and limitations of each element.

# The PoC structure – and Full Scale design Prototype

- Dedicated signal conditioning modules for each logical signal type,
- Main logic realized by the reprogrammable logic unit (FPGA unit),
- Modular system design to allow flexibility of functionality and signals quantity configuration,
- Integrated management and diagnostics for system reliability monitoring and instant malfunction diagnosis,



# The PoC structure overview




# The Full Scale Prototype – Initial prototype scope

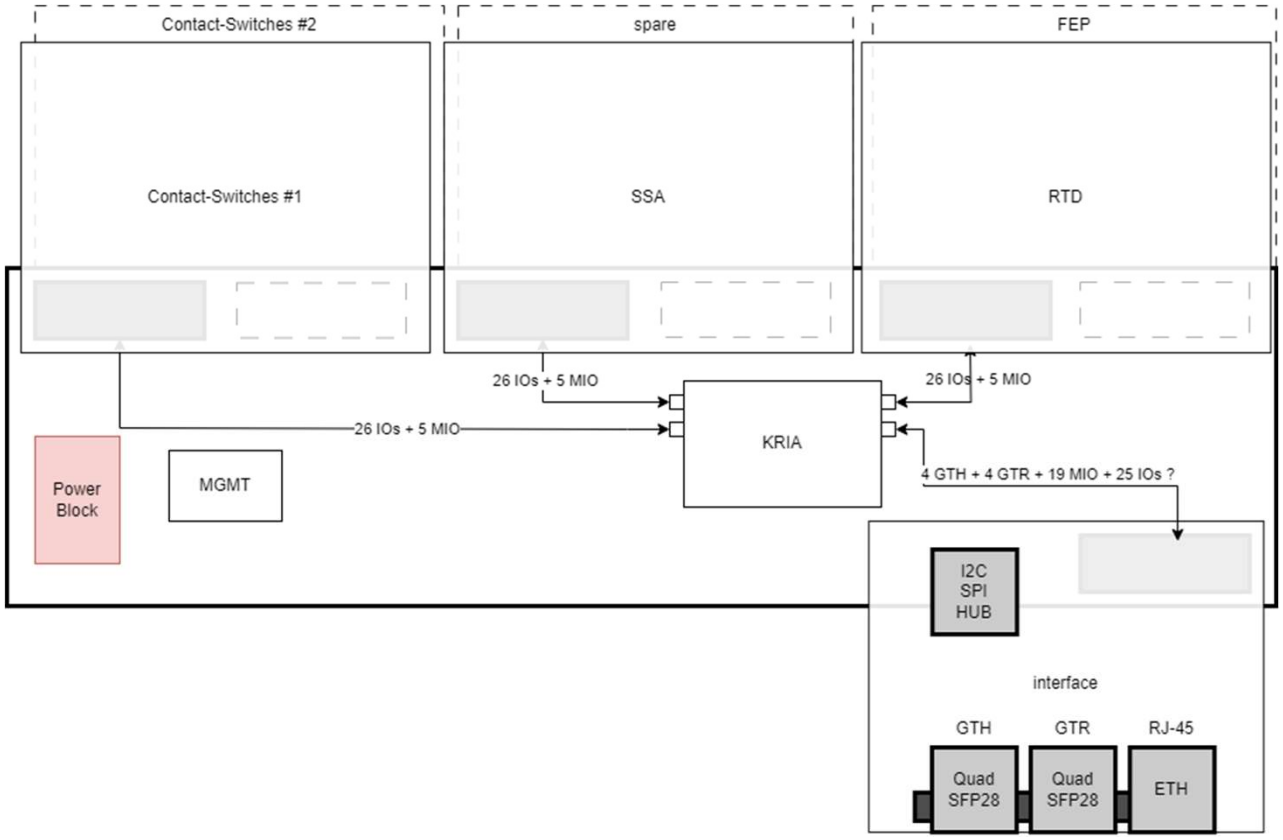
FSP **scope (**according **to SOW)**:

Detailed tests of “Proof of Concept Prototype” and all the information gathered in the scope of PDR task will allow to start design phase of the final electronics for the system. The purpose of the phase is to:

- Develop electric schematics of the device
- Make detailed mechanical planning of the system
- Plan and prepare routing of all PCBs in the system
- Develop mechanical project for the enclosure/box
- Prepare manufacturing data for all elements

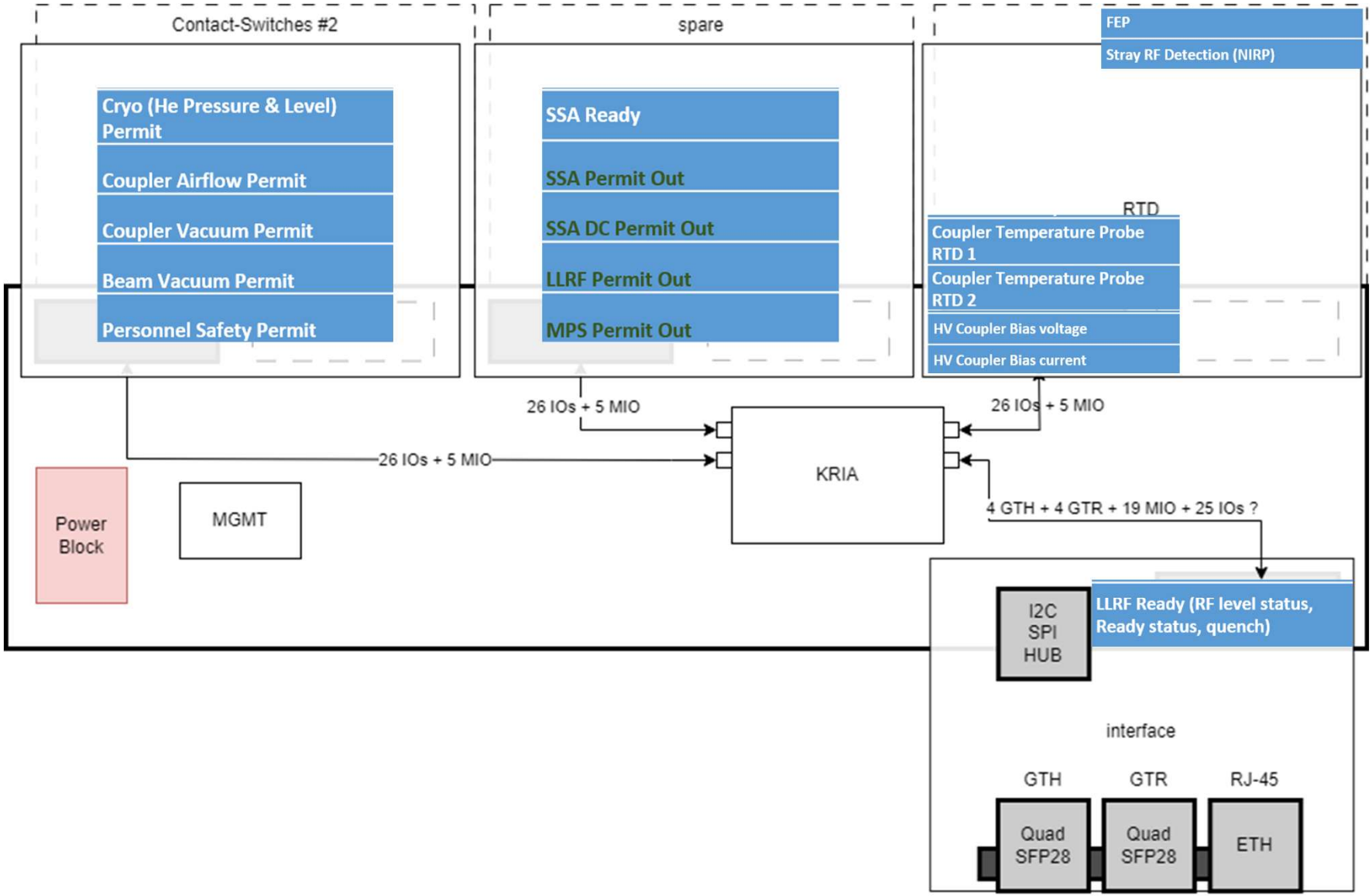
The design phase will end with the production of the Initial Prototype device (electronics, mechanics). **As part of the task the prototype will be fully evaluated, and prototype firmware/software will be implemented. At this stage also the prototype evaluation in the PIP-II IT (or other dedicated test-stand is foreseen).**

# The Full Scale prototype structure

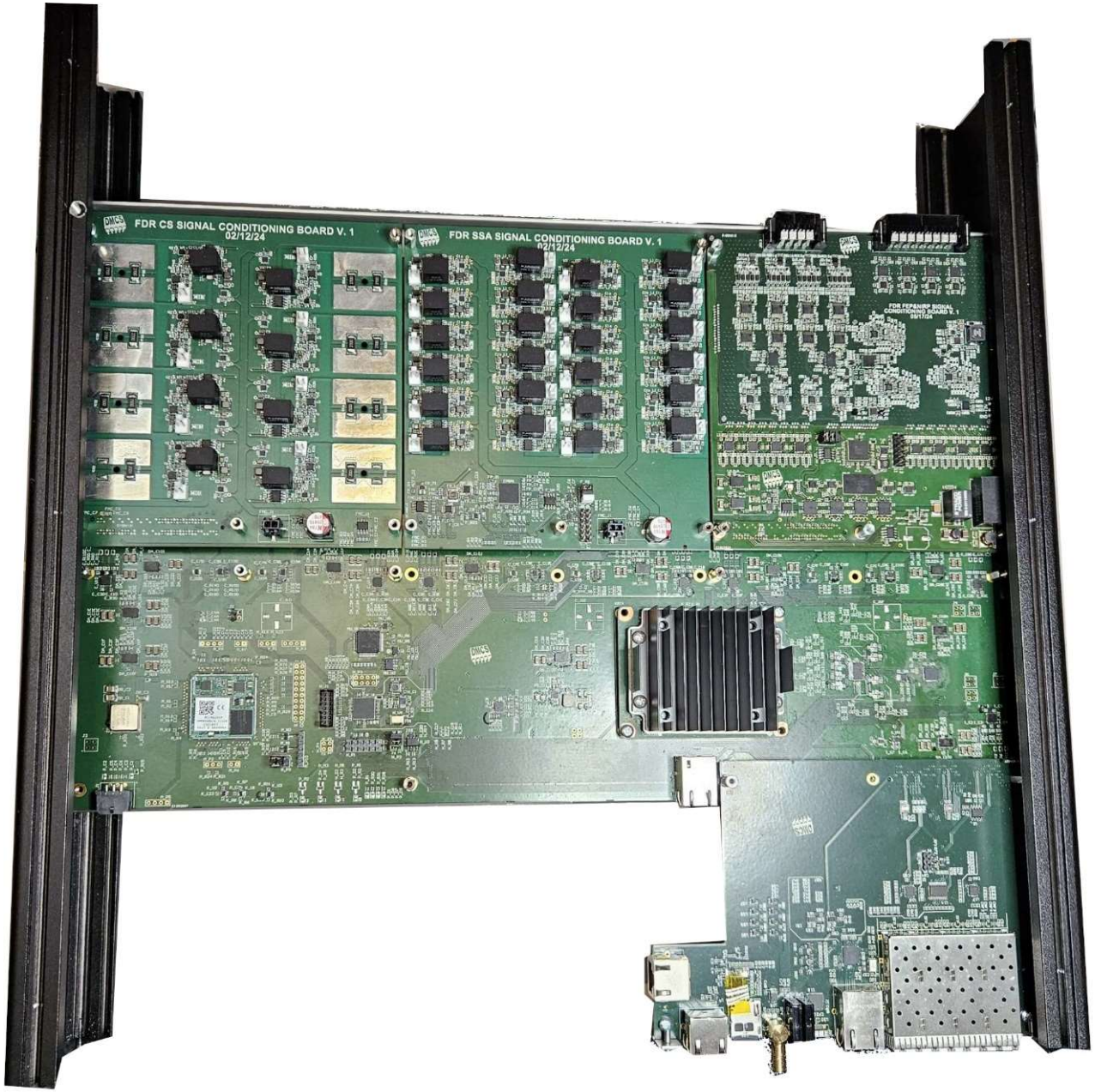



| NO | Signal Origination | Signal Name | FMC board (SLOT) |
|---|---|---|---|
| 1 | Cryo | He Pressure & Level Module | CS0 (TOP0) |
| 2 | Fluids/PLC | Coupler Window Cooling Airflow Permit C1 | CS0 (TOP0) |
| 3 | Fluids/PLC | Coupler Window Cooling Airflow Permit C2 | CS0 (TOP0) |
| 4 | Fluids/PLC | Coupler Window Cooling Airflow Permit C3 | CS1 (BOT 0) |
| 5 | Fluids/PLC | Coupler Window Cooling Airflow Permit C4 | CS1 (BOT 0) |
| 6 | Vacuum/PLC | Coupler Vacuum Permit C1 | CS0 (TOP0) |
| 7 | Vacuum/PLC | Coupler Vacuum Permit C2 | CS0 (TOP0) |
| 8 | Vacuum/PLC | Coupler Vacuum Permit C3 | CS1 (BOT 0) |
| 9 | Vacuum/PLC | Coupler Vacuum Permit C4 | CS1 (BOT 0) |
| 10 | Vacuum/PLC | Beam Vacuum Permit | CS0 (TOP0) |
| 11 | PSS | Personal Safety Permit C1 | CS0 (TOP0) |
| 12 | PSS | Personal Safety Permit C2 | CS0 (TOP0) |
| 13 | PSS | Personal Safety Permit C3 | CS1 (BOT 0) |
| 14 | PSS | Personal Safety Permit C4 | CS1 (BOT 0) |
| 15 | Cryomodule | Field Emission Probe (FEP) C1 | FEP/NIRP (TOP 2) |
| 16 | | Field Emission Probe (FEP) C2 | FEP/NIRP (TOP 2) |
| 17 | | Field Emission Probe (FEP) C3 | FEP/NIRP (TOP 2) |
| 18 | | Field Emission Probe (FEP) C4 | FEP/NIRP (TOP 2) |
| 19 | NIRP | RF antenna 1 | FEP/NIRP (TOP 2) |
| 20 | NIRP | RF antenna 2 | FEP/NIRP (TOP 2) |
| 21 | NIRP | RF antenna 3 | FEP/NIRP (TOP 2) |
| 22 | NIRP | RF antenna 4 | FEP/NIRP (TOP 2) |
| 23 | NIRP | RF antenna 5 | FEP/NIRP (TOP 2) |
| 24 | NIRP | RF antenna 6 | FEP/NIRP (TOP 2) |
| 25 | LLRF | LLRF Ready (RF level status, Ready status, quench) | Interface |
| 26 | Timing/Controls | L-clock | Interface |
| 27 | Timing/Controls | A-clock | Interface |
| 28 | Bias Power Supply | Coupler Bias Voltage (V) C1 | RTD/HV (BOT 2) |
| 29 | Bias Power Supply | Coupler Bias Voltage (V) C2 | RTD/HV (BOT 2) |
| 30 | Bias Power Supply | Coupler Bias Voltage (V) C3 | RTD/HV (BOT 2) |
| 31 | Bias Power Supply | Coupler Bias Voltage (V) C4 | RTD/HV (BOT 2) |
| 32 | Bias Power Supply | Coupler Bias Current (A) C1 | RTD/HV (BOT 2) |
| 33 | Bias Power Supply | Coupler Bias Current (A) C2 | RTD/HV (BOT 2) |
| 34 | Bias Power Supply | Coupler Bias Current (A) C3 | RTD/HV (BOT 2) |
| 35 | Bias Power Supply | Coupler Bias Current (A) C4 | RTD/HV (BOT 2) |
| 36 | Cryomodule | Temperature Probe RTD 1 C1 | RTD/HV (BOT 2) |
| 37 | Cryomodule | Temperature Probe RTD 1 C2 | RTD/HV (BOT 2) |
| 38 | Cryomodule | Temperature Probe RTD 1 C3 | RTD/HV (BOT 2) |
| 39 | Cryomodule | Temperature Probe RTD 1 C4 | RTD/HV (BOT 2) |
| 40 | Cryomodule | Temperature Probe RTD 2 C1 | RTD/HV (BOT 2) |
| 41 | Cryomodule | Temperature Probe RTD 2 C2 | RTD/HV (BOT 2) |
| 42 | Cryomodule | Temperature Probe RTD 2 C3 | RTD/HV (BOT 2) |
| 43 | Cryomodule | Temperature Probe RTD 2 C4 | RTD/HV (BOT 2) |
| 44 | HPRF/SSA | SSA Ready C1 | SSA |
| 45 | HPRF/SSA | SSA Ready C2 | SSA |
| 46 | HPRF/SSA | SSA Ready C3 | SSA |
| 47 | HPRF/SSA | SSA Ready C4 | SSA |
| 48 | RFPI | SSA Inh (Permit) C1 | SSA |
| 49 | RFPI | SSA Inh (Permit) C2 | SSA |
| 50 | RFPI | SSA Inh (Permit) C3 | SSA |
| 51 | RFPI | SSA Inh (Permit) C4 | SSA |
| 52 | RFPI | SSA DC Inh (Permit) C1 | SSA |
| 53 | RFPI | SSA DC Inh (Permit) C2 | SSA |
| 54 | RFPI | SSA DC Inh (Permit) C3 | SSA |
| 55 | RFPI | SSA DC Inh (Permit) C4 | SSA |
| 56 | RFPI | LLRF Permit C1 | SSA |
| 57 | RFPI | LLRF Inh (Permit) C2 | SSA |
| 58 | RFPI | LLRF Inh (Permit) C3 | SSA |
| 59 | RFPI | LLRF Inh (Permit) C4 | SSA |
| 60 | RFPI | MPS Inh (Permit) C1 | SSA |
| 61 | RFPI | MPS Inh (Permit) C2 | SSA |
| 62 | RFPI | MPS Inh (Permit) C3 | SSA |
| 63 | RFPI | MPS Inh (Permit) C4 | SSA |

# The Full Scale prototype structure



# The Full Scale prototype – top view

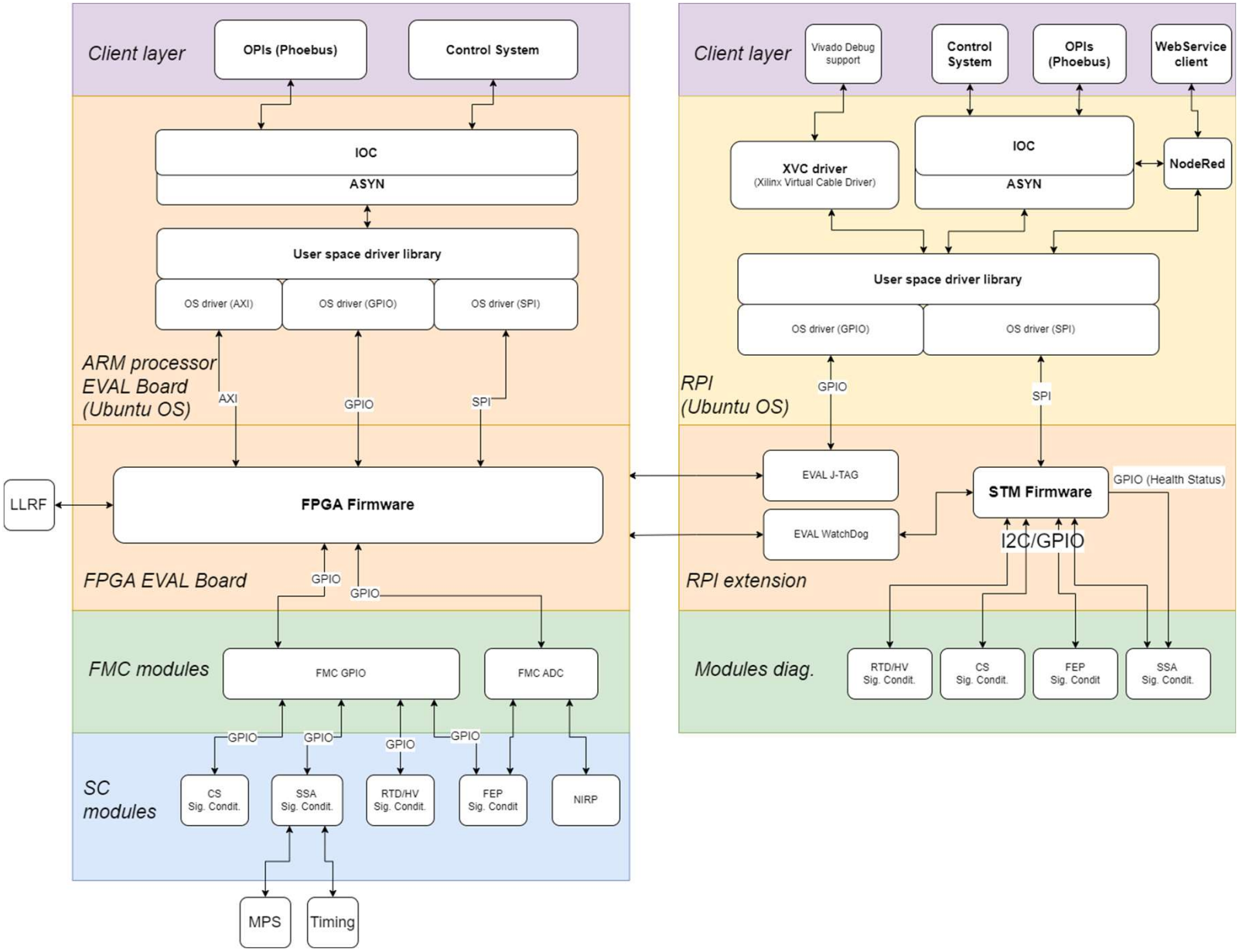


# The Full Scale prototype – bottom view

# The RFPI FSP software overview

- The RFPI prototype software divided in two main blocks (as for PoC):
  - SW/FW for the main logic unit and peripherals interface and management,
  - SW/FW for diagnostics and management subsystem.
- Software structure unified (as much as possible) for both parts,
- Firmware/Software developed for the
  - Xilinx KRIA SOM – main logic unit,
  - Microchip SOM – management unit,
  - Lattice iCE40 FPGAs – small, high-performance FPGAs for communication purposes
- The Ubuntu OS chosen as feasible for both platforms (Xilinx board and Microchip SOM),
- The EPICS control system chosen for both implementations – to be consistent with the overall linac infrastructure.

# The FSP software overview



# The RFPI FDR prototype technnical talks

**08:40** → 09:00 **RFPI System Design Overview**
**Mówca**: Wojciech Cichalewski (LUT-DMCS)

**09:00** → 09:15 **RFPI Full Scale Prototype Hardware Overview**
**Mówca**: Wojciech Jalmuzna (Lodz University of Technology)

**09:15** → 09:30 **Main logic realization/execution HW**
**Mówca**: Dr Piotr Amrozik (TUL-DMCS)

**09:30** → 10:00 **Signal Conditioning Modules**
**Mówcy**: Bartosz Pekoslawski (TUL-DMCS), Pawel Marciniak (TUL-DMCS)

**10:00** → 10:15 **RFPI FSP mechanics and interfaces**
**Mówca**: Grzegroz Jablonski

**10:50** → 11:05 **FW for main protection functionality and management**
**Mówcy**: Grzegroz Jablonski, Rafal Kielbik (TUL-DMCS)

**11:05** → 11:25 **SW for main protection functionality and management**
**Mówcy**: Kacper Klys, Prof. Wojciech Tylman (TUL-DMCS)

**11:25** → 11:35 **Quality Control/ HW&SW Documentation**
**Mówca**: Wojciech Jalmuzna (Lodz University of Technology)

**11:35** → 11:50 **Test Stand Design and Preparation**
**Mówca**: Dr Rafal Kielbik (TUL-DMCS)

**11:50** → 12:05 **RFPI FSP Test Results**
**Mówca**: Wojciech Cichalewski (LUT-DMCS)

# Summary

- The full scale design prototype is the next (after PoC) stage of the new RFPI system design (before final one),
- The hardware and software structure of this RFPI prototype has been improved based on the PoC development and evaluation findings,
- Over 80 % of the hardware modules has been developed, designed and produced locally (by DMCS),
- Software for main modules and the diagnostics and management has been proposed and is under development,
- Tests at the PIP-II modules test facility are ongoing,
- All together 4 pieces of the RFPI FSP hardware in preparation (2 dedicated for permanent installation @CMTF)

# Thank You