

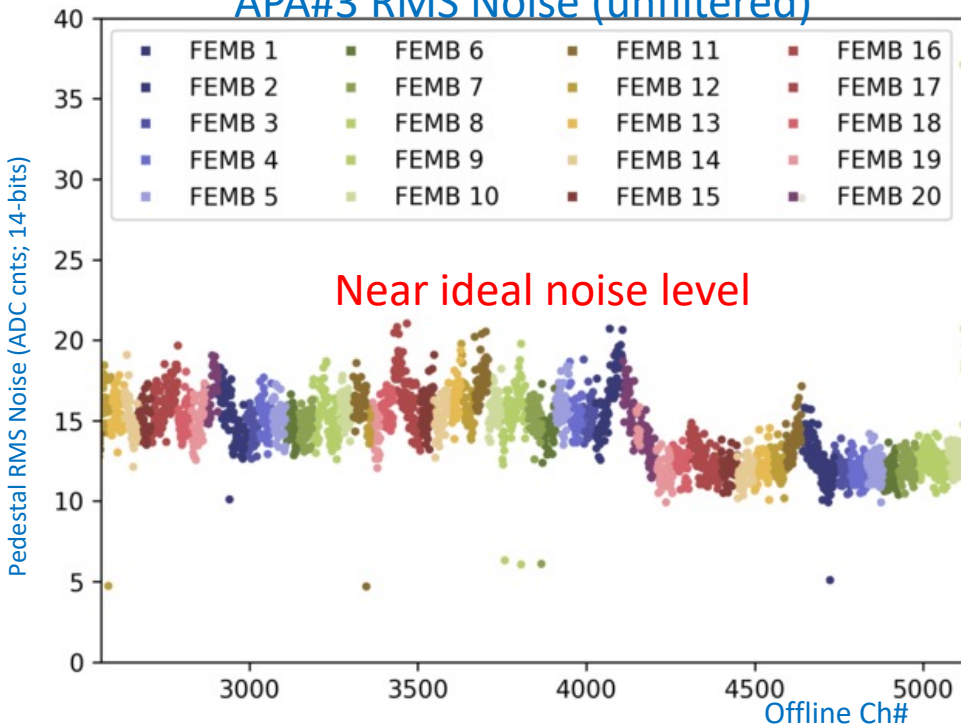
NP04 TPC Electronics Performance

Cheng-Ju Lin and David Christian

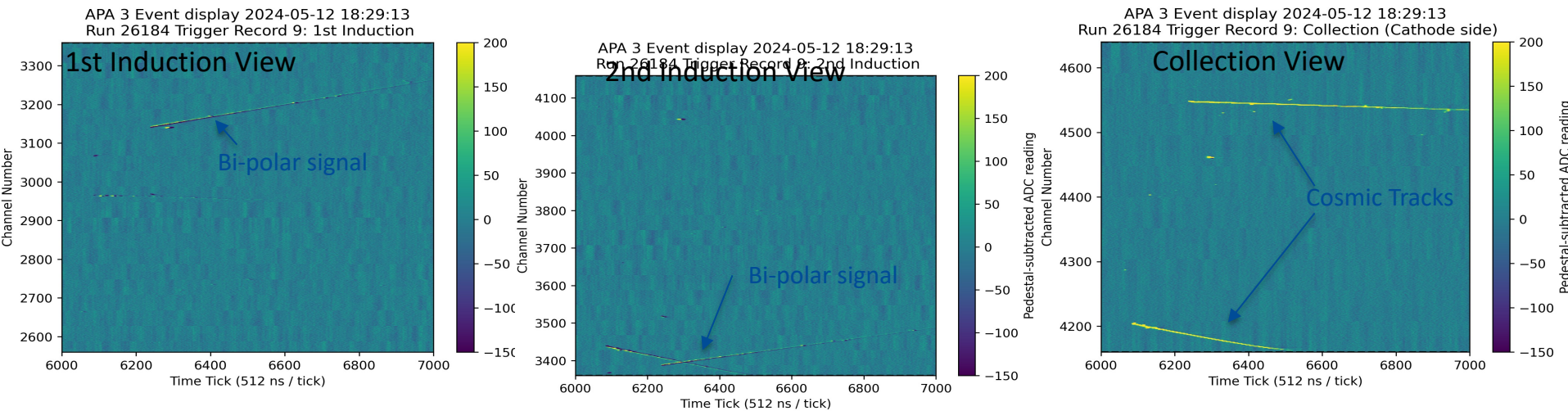
FD1 Technical Board Meeting
12 June 2024

- TPC readout electronics have been performing reliably for the past few months
- All 10,240 channels on 80 Frontend Motherboards are functioning well → **we have 0 dead electronic channels !**
- Overall noise performance is decent

APA#3 RMS Noise (unfiltered)

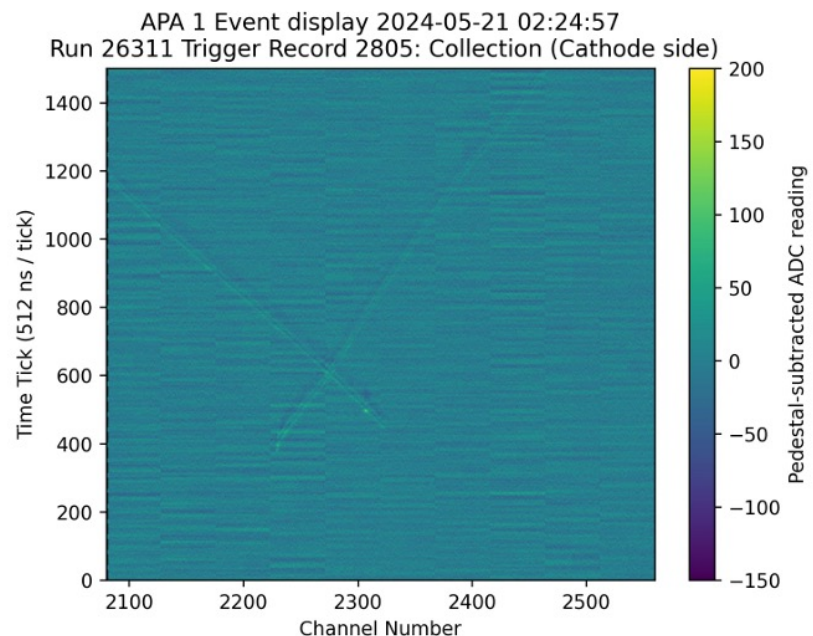
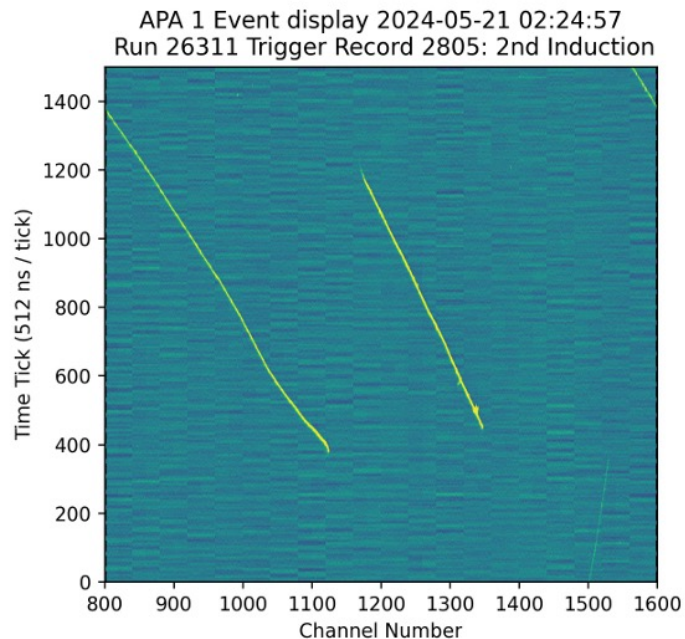


- APA1 and 2 have slightly higher coherent noise. With offline noise filter, noise level is also near ideal level



- Some issues impacting the readout electronics:
 - About 20 APA “wires” are disconnected to the TPC electronics for various reasons
 - Electrical shorts across wires that come and go. High noise on a few channels to a large fraction of channels
 - Origins are likely not related to the TPC electronics, but they do impact the operations of the electronics

- Most significant issue is the APA#1 HV bias on the collection plane
 - Based on the bias current and voltage measurement, the connection is likely intermittent
 - Not able to maintain a stable bias voltage on the collection wires
 - APA#1 is effectively a two-view TPC



- Lessons Learned for FD1
 - APA bias QC test failed to catch the APA#1 collection bias problem:
 - 👉 Looking into modifying the warm filter board to allow direct connectivity measurement of the bias line by measuring the capacitance. Testing the prototype board this week on CRP6 coldbox
 - 👉 Looking into adding a redundant bias line for the collection wires
- TPC Electronics/BDE Hardware Database Liaison: Martin Tzanov (LSU)