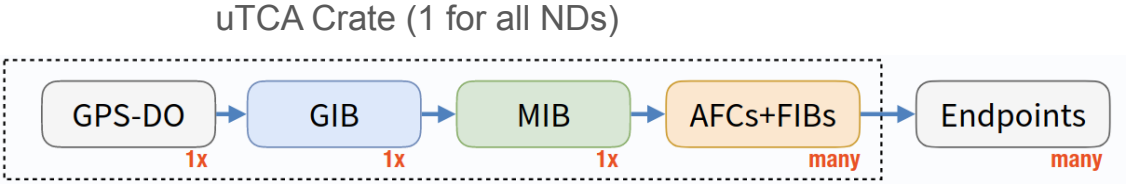# DAQ WG Status Report

Nicolò Tosi for the DAQ WG

Quick recap of central DAQ and Timing architecture

- DAQ is based on Ethernet, timing is based on a custom protocol over Fiber

- Central DAQ expects 10G fibers from endpoints
  - Option for 1G to lower cost and complexity exists

- Central DAQ maintains a firmware block to be integrated in the endpoints

DAQ is optimized for FD, ND is somewhat simpler
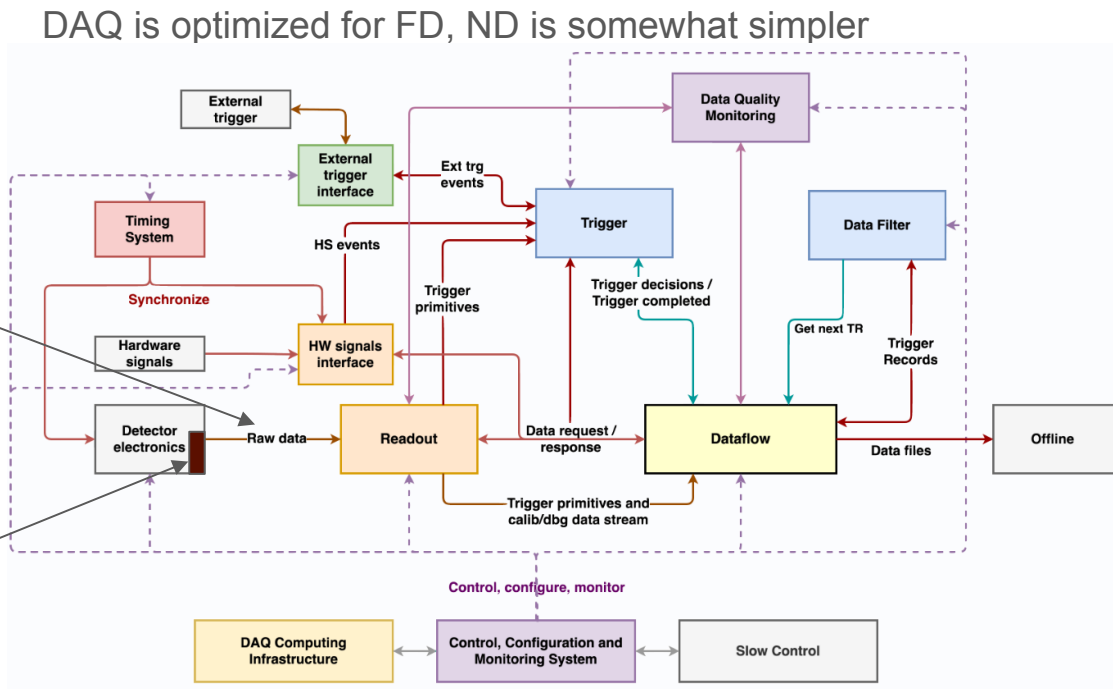
Quick recap of Timing architecture

uTCA Crate (1 for all NDs)

GPS-DO → GIB → MIB → AFCs+FIBs → Endpoints

1x   1x   1x   many   many

Fiber transmits encoded clock (62.5 MHz and data (timestamps, sync command, spill, …)

Master Clock

Timing Data

0   1   Z

Endpoints transmit back for delay compensation

Endpoint reference design available as FMC
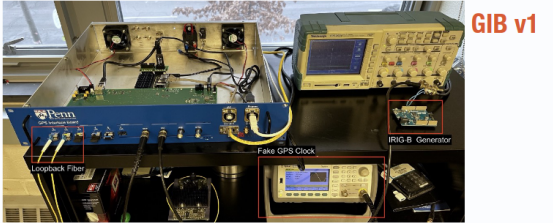
GIB v1

MIB v2

FIB v1+ AFC v4

8 Fibers per FIB, 8 Endpoints per fiber

Test of timing system performance and integration aspects

Delayed due to delay in availability of timing endpoint FMC boards

- One FMC board is in Genova, will be used as Master

- Two additional FMCs are now available at CERN thanks to D. Cussans.
  - I will pick them up and meet Dave and other experts at CERN "sometime in June"
  - The plan is to integrate them with FPGAs to test as endpoints
  - We want to measure jitter between the two, acquire familiarity, etc…
  - Availability of FW developers in Bologna is very low for 2024

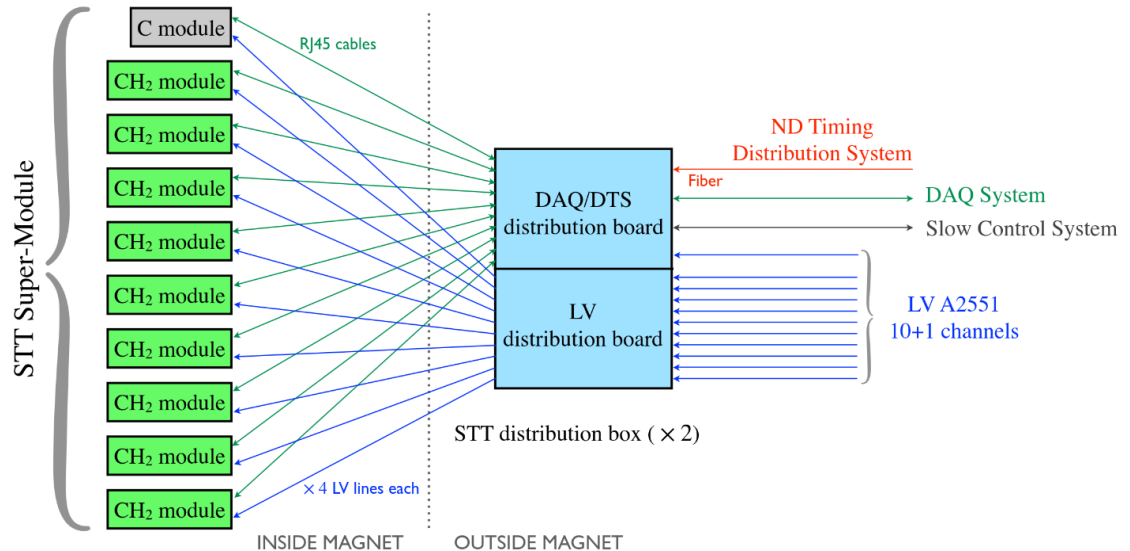# Status of subdetector hardware side - GRAIN

- Significant progress made on GRAIN ASIC specification

- ASIC Design effort starting now, first prototype submission end of 2025
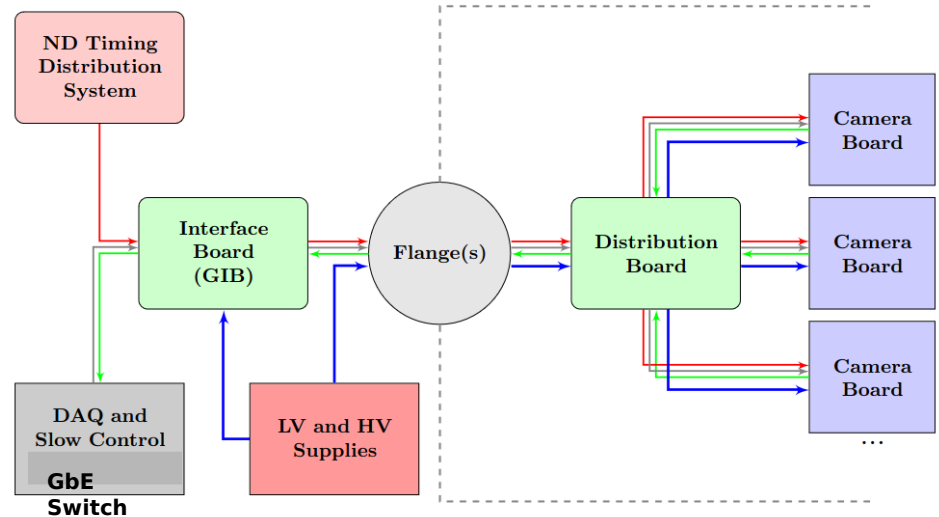
- Interface board (the actual DAQ endpoint) design will start in 2025
- Will feature: ASIC interface, data buffering, DAQ endpoint, Timing endpoint

Status of subdetector hardware side - Tracker

- Significant progress made on front end board design for STT
- Viable architecture but room for optimization exists

- "distribution" board: expressed desire to share development effort with GRAIN, may share many aspects with GRAIN Interface Board
- Will feature: FEB interface, DAQ endpoint, Timing endpoint

Status of subdetector hardware side - ECAL

No significant news on back-end after discussion with CAEN in January

Tests are still ongoing on the Front End and the viability of the CAEN FERS is yet to be completely confirmed

Contact person will be *Antonio Di Domenico*

A contact for the magnet for DCS/DSS matters may also be useful

Progress on TDR

- Substantial text present in the DCS and DSS section
  - Thanks to Camillo, general description draft is complete
  - Missing subdetector specific subsections, some figures, tables, etc…

- Some general DAQ and Timing text written.
  - Need to fill this table based on changes to the Front End w.r.t. CDR
  - You can be conservative, the total is going to be small
  - What beam scenario?

Subdetector	ECAL	GRAIN	STT	Total
Average hit size [bits]		80		-
Hits per spill [#]				
Cosmics and background hits [Hz]				
Hits from calibration [#]				
Total data rate [Mbps]				

Table 1.6: Expected data rates for which beam scenario??

Other news

- I was unable to organize a proper meeting with all the stakeholders about **beam timing**
  - Most relevant experts not attending this CM
  - Many of them at CERN for ProtoDUNE, will try to organize something there

- Depending on Camillo's future availability, an additional person with experience on DCS/DSS matters may be required