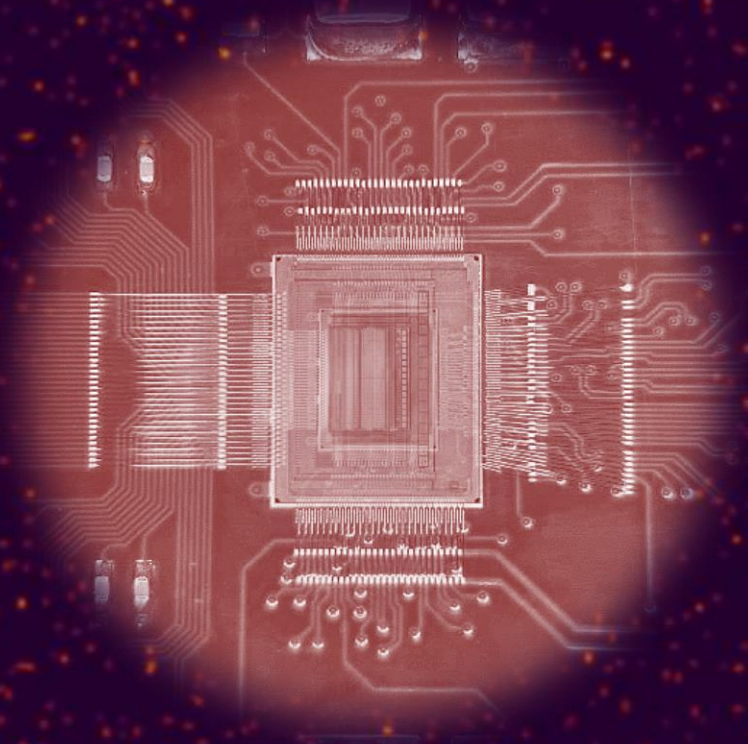
RDC4 Meeting

GAMPix:

Grid Activated Multiscale Pixel

A fine-grained, low-noise and ultra-low power pixelated charge readout for NL TPCs



Aldo Pena Perez and Bahrudin Trbalic
On behalf of the GAMPIx team and SLAC TID-ID IC Dept.

Thursday, 20th May 2024

SLAC | TID TECHNOLOGY INNOVATION DIRECTORATE
TID-ID INTEGRATED CIRCUITS DEPARTMENT
STANFORD UNIVERSITY
U.S. DEPARTMENT OF ENERGY

Agenda

1. **GAMPix Concept**
   Motivation and background
2. **Applications**
   γ-TPC in Space and DUNE
3. **Key Specifications**
   Design for low-power and low-noise
4. **ASIC Readout Architectures**
   Brief overview
5. **Conclusions**

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GAMPix Concept

GAMPix Concept

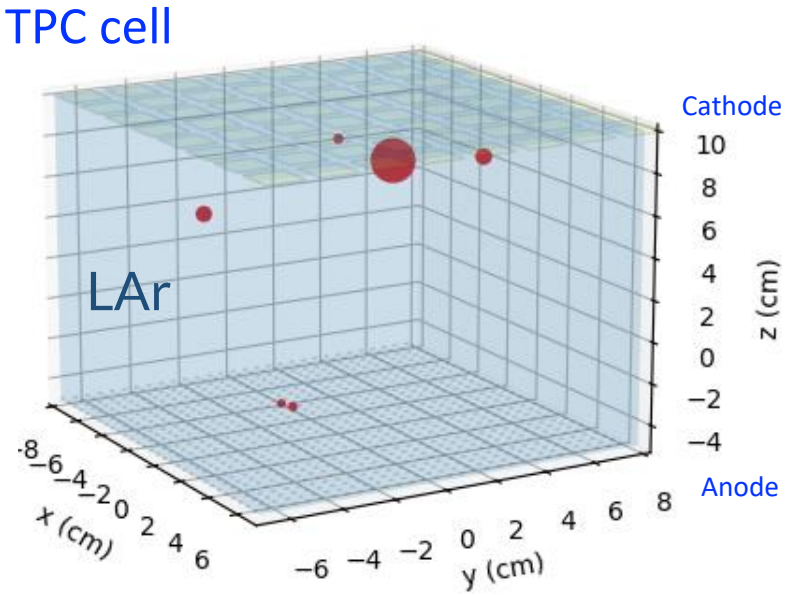
Grid **A**ctivated **M**ultiscale **Pix**el Readout

Key features:

- A novel fine-grained, low-noise and ultra-low power pixelated charge readout [1-2]
- Electron track detection with a dual scale system in LArTPCs

Low { **Noise**, **Threshold**, **Power** }

Diffusion Independent
(Can use diffusion to estimate drift length)

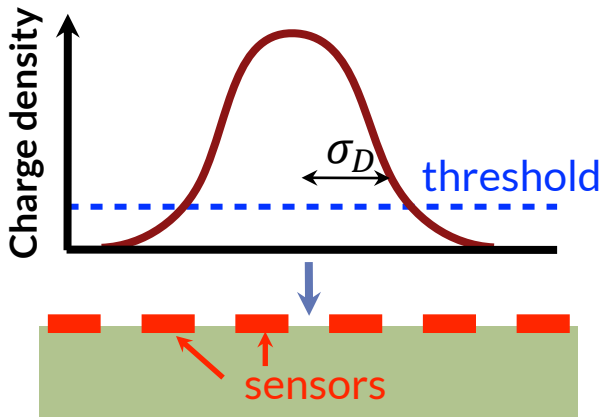


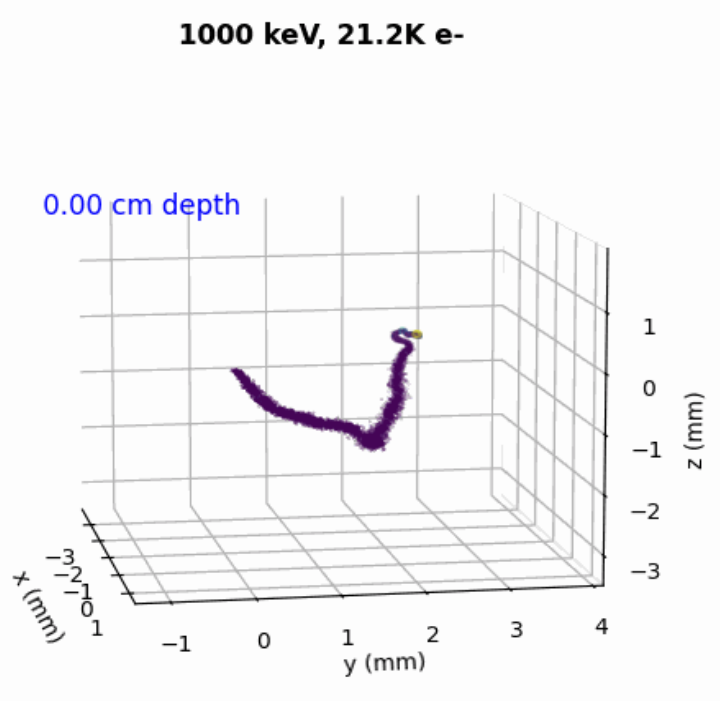
Example: MeV gamma ray measured in LAr TPC. Red circles are electron recoil tracks.

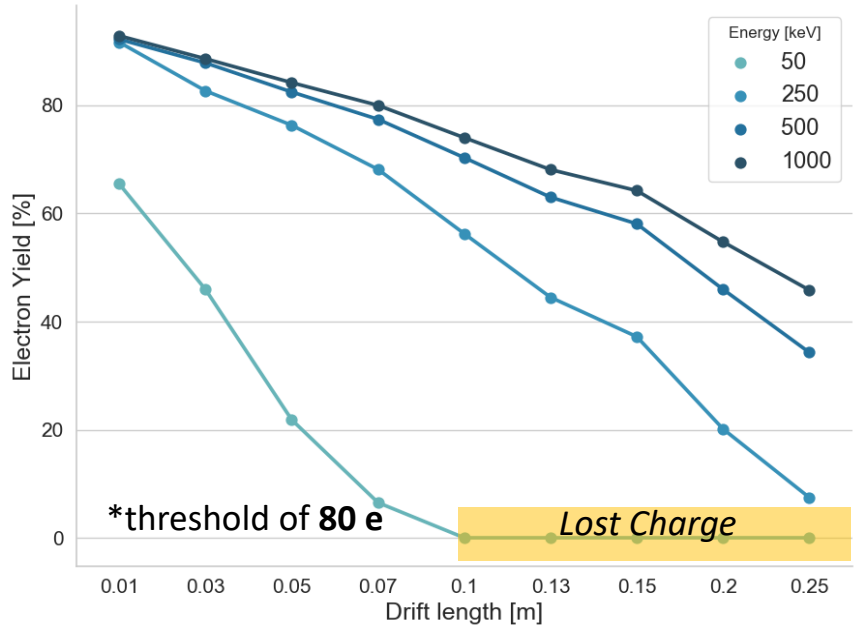
GAMPix Concept

Challenges with fine scale readout

- Electron clouds **diffuse** while drifting to anode
- **Charge loss** when diffusion ~ sensor size
- High sensor count – prohibitive power in cryogenic TPC

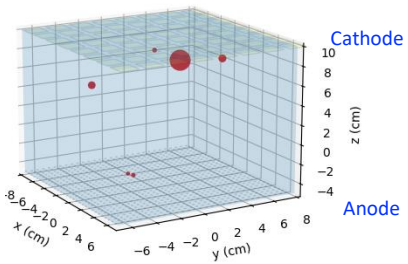






GAMPix Concept

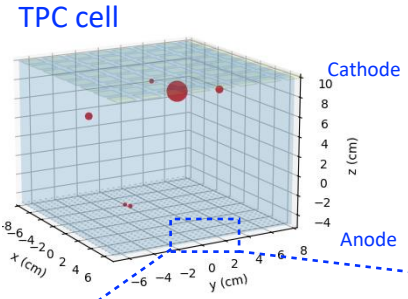
TPC cell



Approach:

Coarse (cm-pitch) induction grids followed by fine grained pixels

GAMPix Concept



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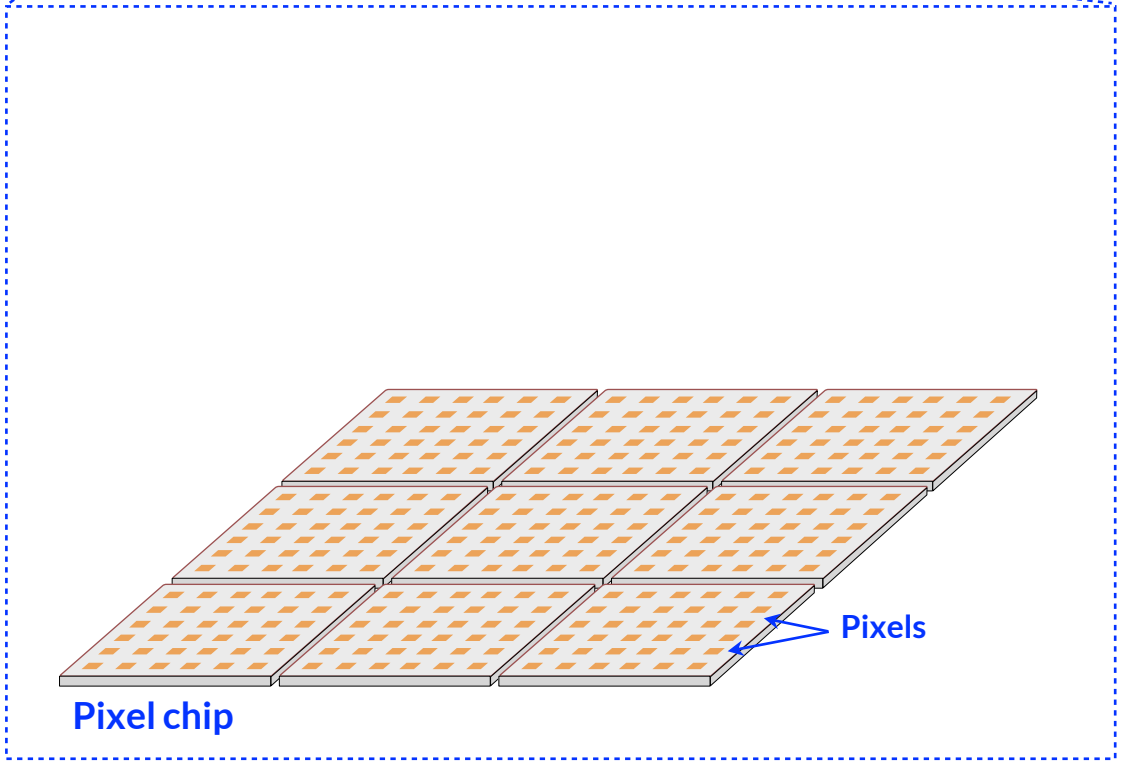
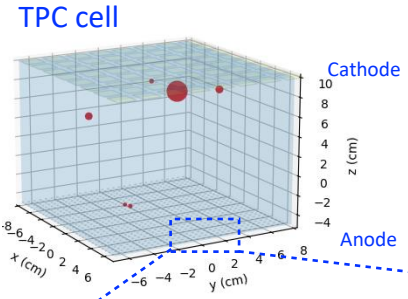


Pixel chips:

- Image track

GAMPix Concept



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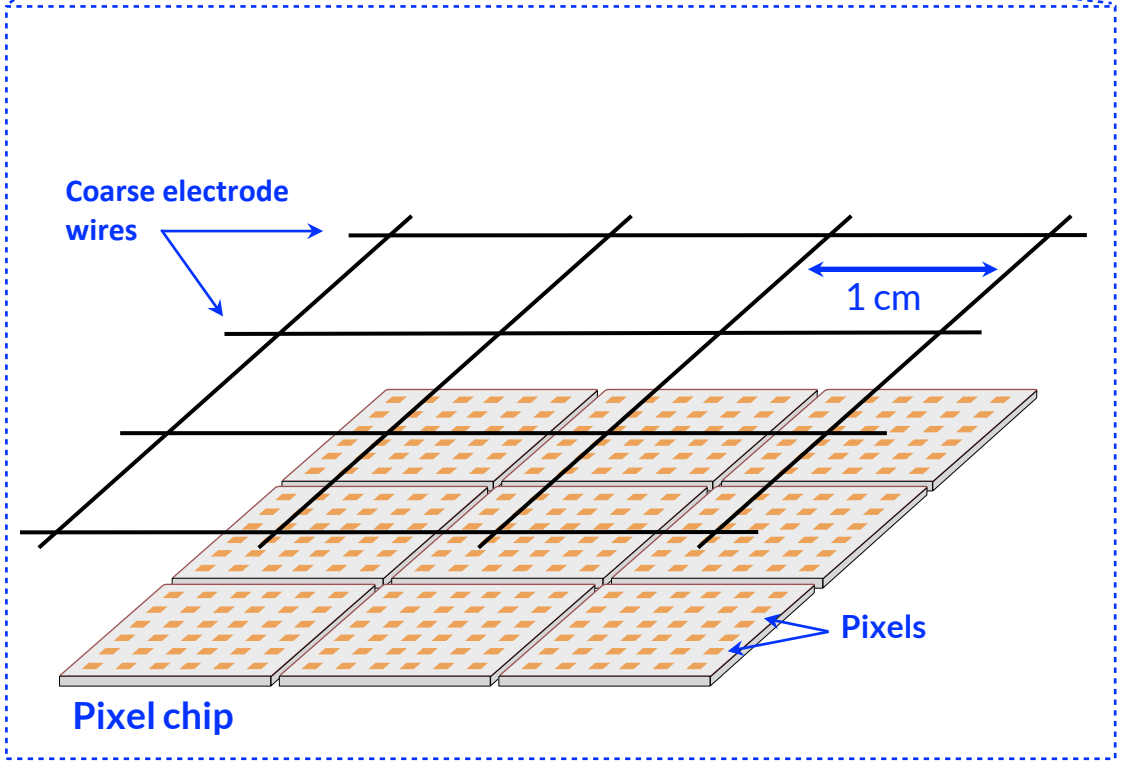


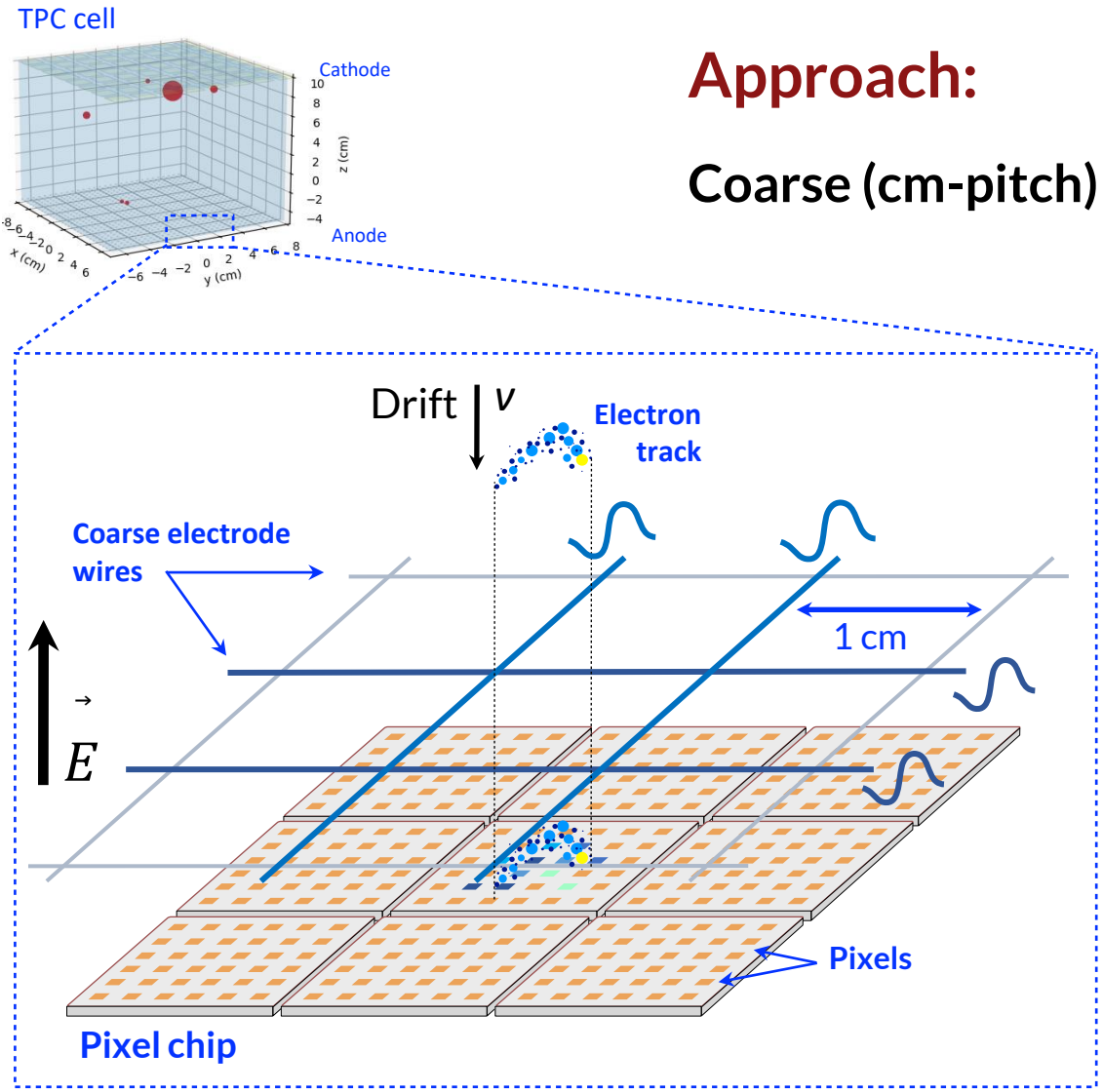
Pixel chips:

- Image track

Coarse grids:

- Measure charge **integral**, with σ_e~15 e$^-$

GAMPix Concept



Approach:

Coarse (cm-pitch) induction grids followed by fine grained pixels

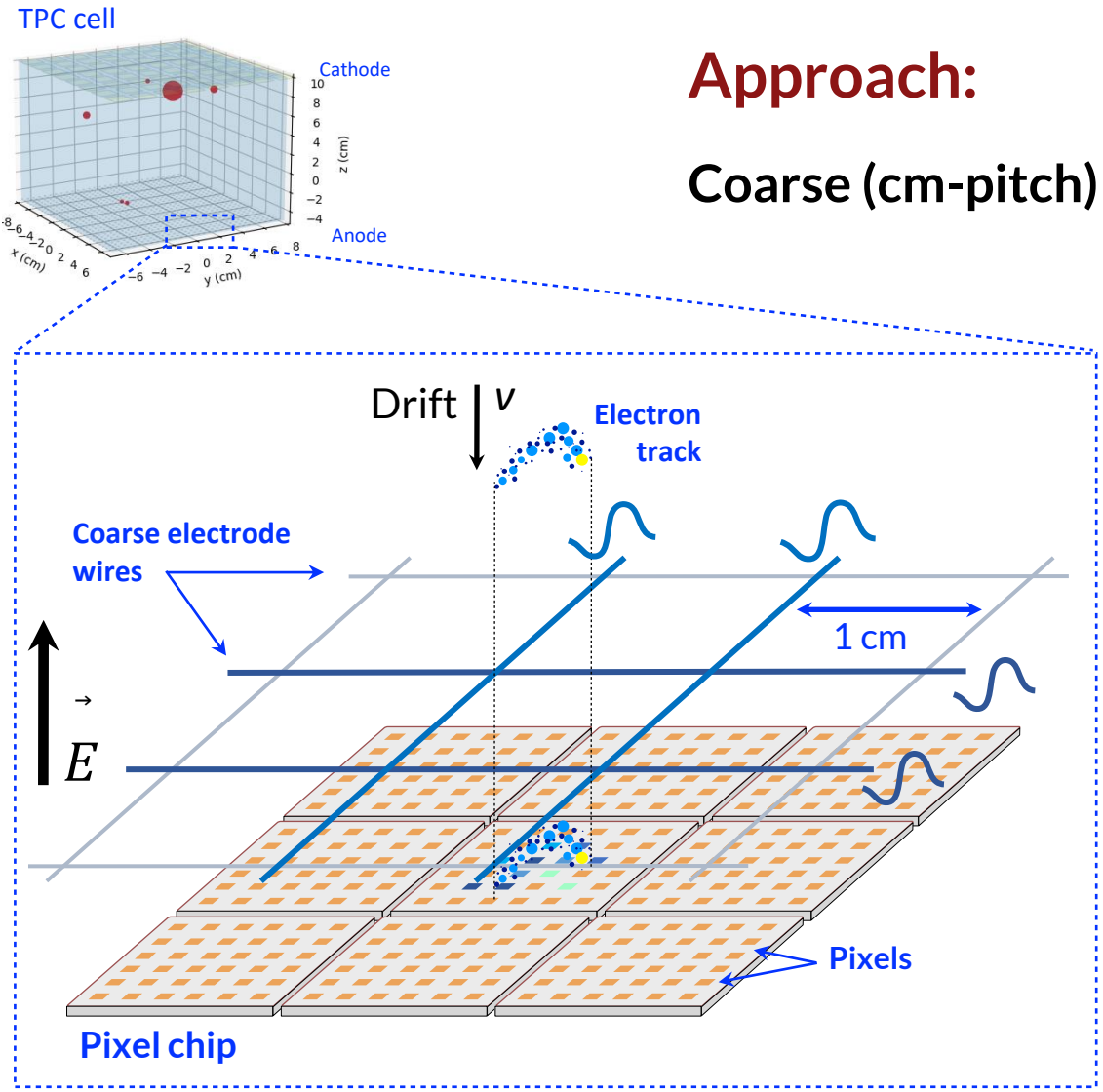
Pixel chips:

- Image track
- **Power-up in < 1 µsec following coarse trigger**
- Power reduced by **10^3–10^4**, to ~1 W/m^2

Coarse grids:

- Measure charge **integral**, with σ_e~15 e$^-$
- Provide **trigger signal (address)** to pixel chips

GAMPix Concept



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- Measure charge **integral**, with σ_e~15 e$^-$
- Provide **trigger signal (address)** to pixel chips

Solves both power consumption and charge loss due to diffusion

Also: drift length measured by amount of diffusion

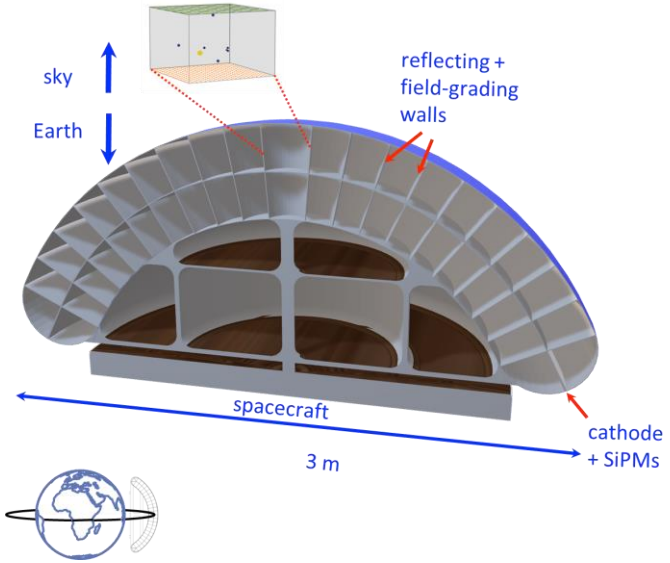
2

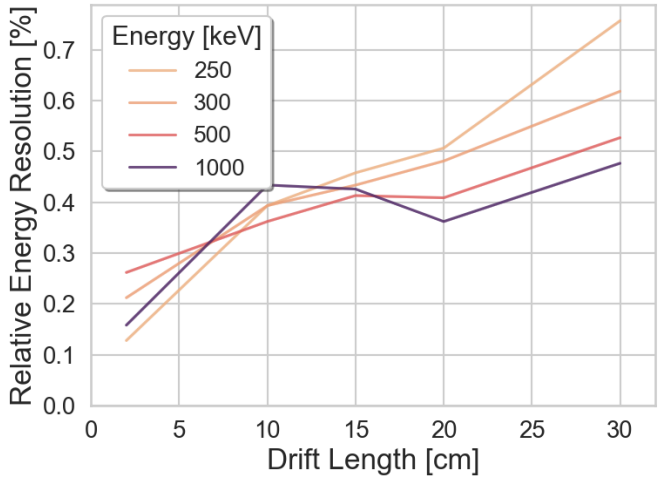
Applications

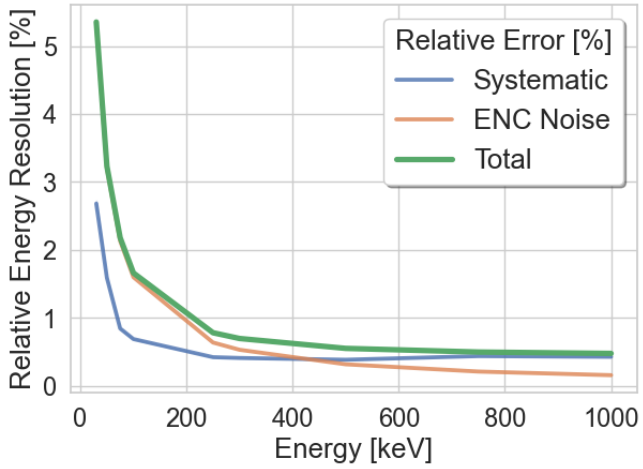
Applications

γ-TPC in Space (GammaTPC Telescope)

- 500µm-pixels, ENC 20e-
- 1cm-wires, ENC 30e-
- Track imaging resolution ~0.25mm
- Energy resolution < 1% for electron tracks > 100keV (2k e-)
- Power consumption ~1W/m2 (Saves by a factor of 10^3-10^4)
- Drift length measurements vis diffusion with ~5% accuracy



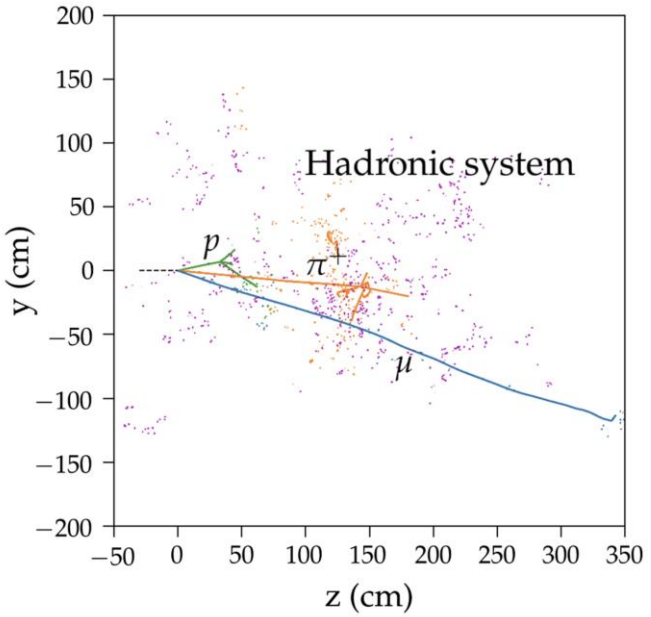


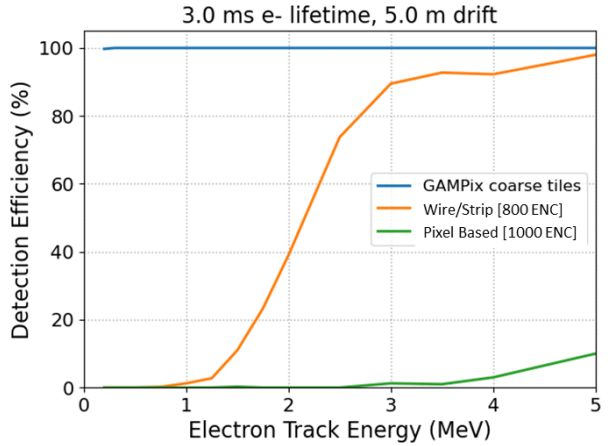


Applications

Potential on DUNE

- Possible readout for DUNE Far Detector Module #3
- 5mm-pixels, 5cm-wires/grids
- Small charge deposition (blips) retained
  → Lower detection threshold (sub-MeV) and better energy resolution
- Drift length determined without external t_0
  → improve background rejection
- Expect to improve the supernova neutrino measurements and the energy resolution in all the measurements

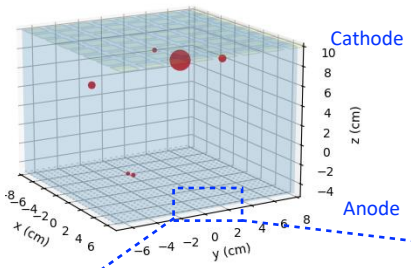


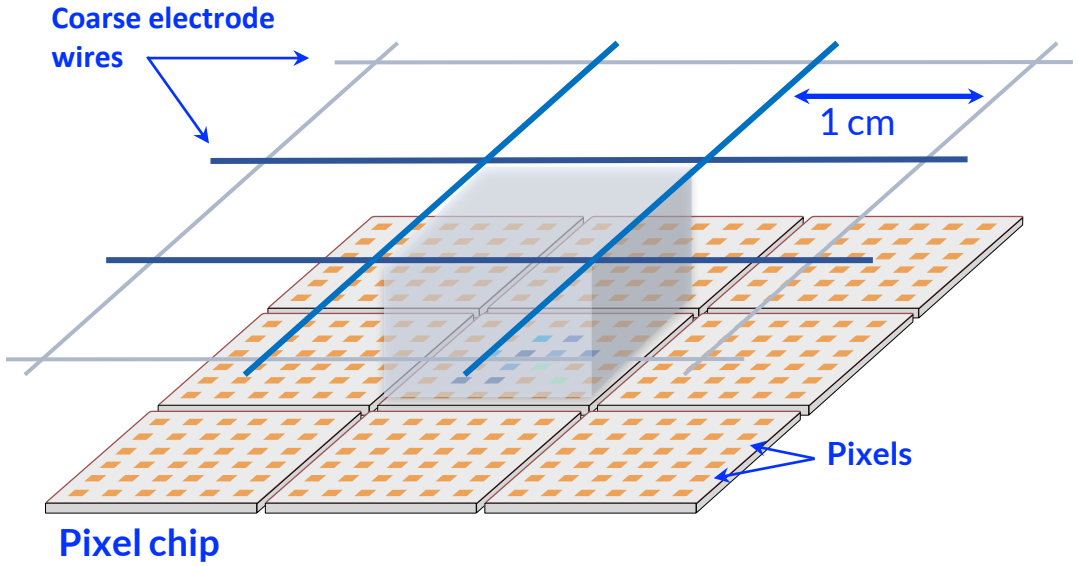


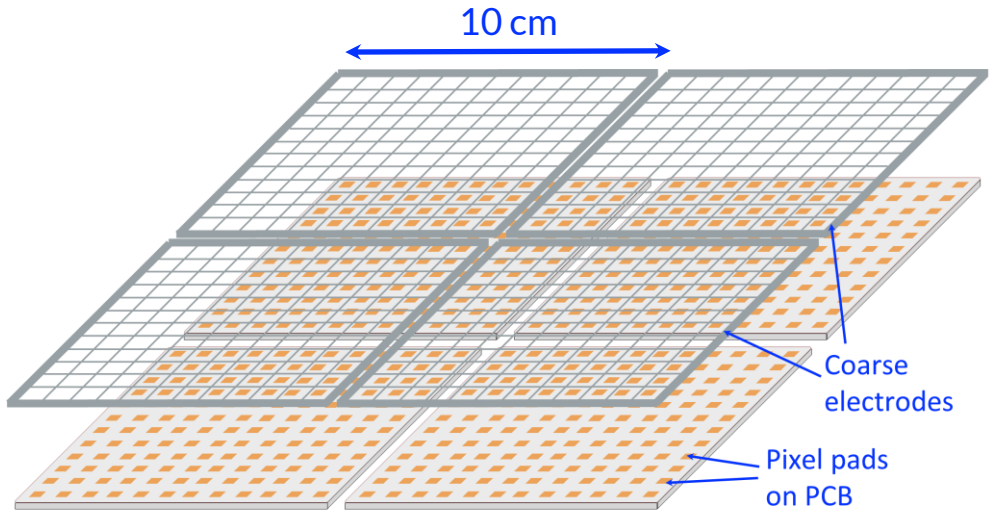
Applications

γ-TPC vs DUNE

TPC cell

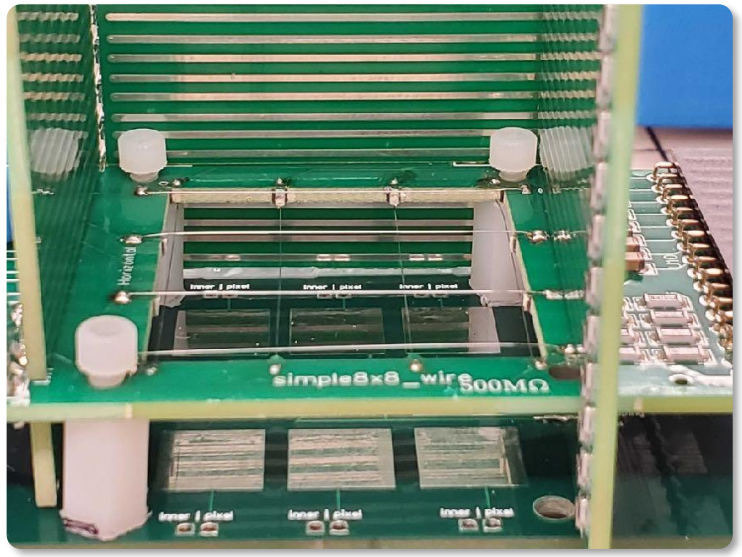




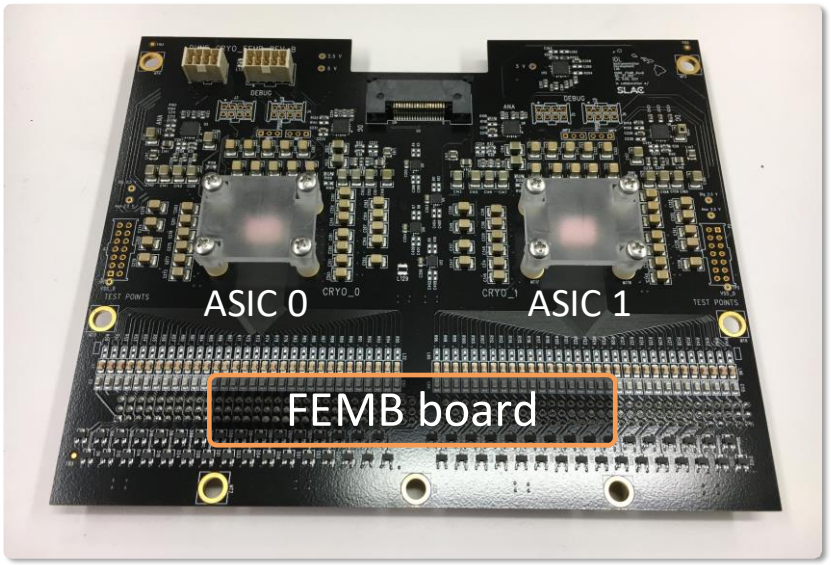


Towards GAMPix Hardware Test

- Built a small LAr TPC prototype for upcoming test in lab setup
- Initial proof-of-concept, with existing (higher noise, no power-switching) CRYO ASIC (σ_e~100e- @ few pF load)



Chip Photograph
R&D Prototype | 7mm x 9mm



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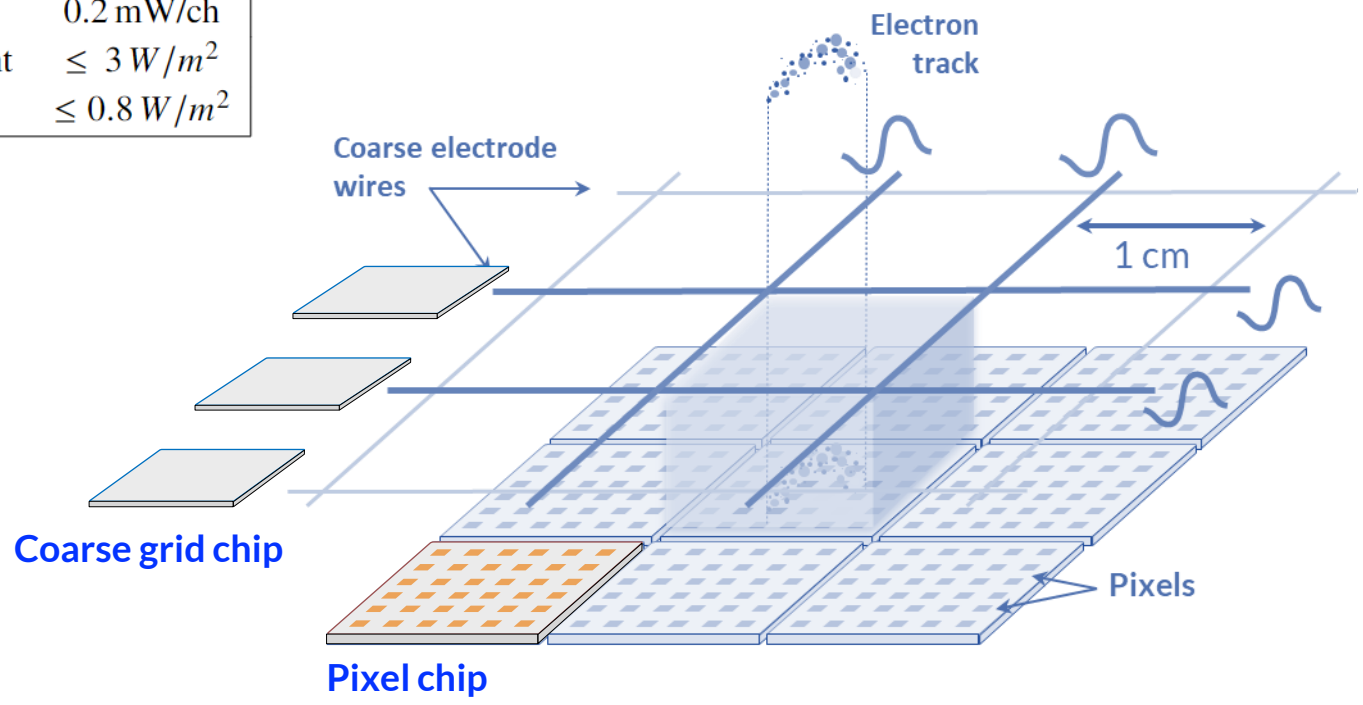
Key Specifications

Key Specifications (preliminary)

Coarse grid wires		Pixels	
Pitch	$1\,cm$	Pitch	$500\,\mu m$
Wire length	$\leq\ 20\,cm$	Pad size	$200,\,\mu m$
Wire diameter	$100 - 200\,\mu m$	Pad capacitance	$500\,fF$
Capacitance	$\leq\ 2 - 3\,pF$	Noise - requirement	$< \sim 50\,e^-$
Noise - requirement	$<\ 30\,e^-$	Noise - expected	$<\ 25\,e^-$
Noise - goal	$10\,e^-$	On power - expected	0.2 mW/ch
Noise - expected	$<\ 20\,e^-$	Average power - requirement	$\leq\ 3\,W/m^2$
Power - requirement	$\leq\ 1\,mW/ch$	Average power - expected	$\leq 0.8\,W/m^2$

- Two readout systems aimed for GAMPix
  - **Pixel chip**
    Low-noise, power-pulsed pixelated architecture
  - **Coarse grid chip**
    Low-noise, low-power single (or few) channel architecture



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ASIC Readout Architectures

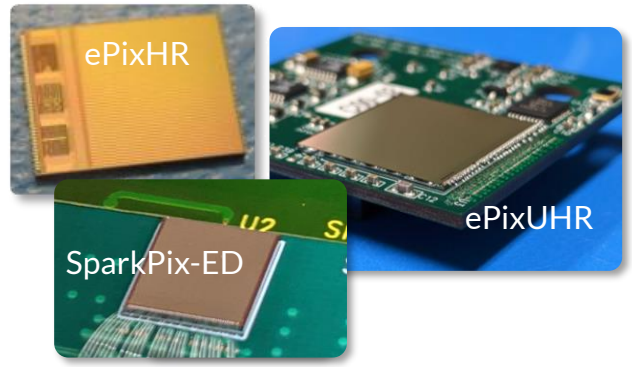
ASIC Readout Architectures

R&D Design Strategy

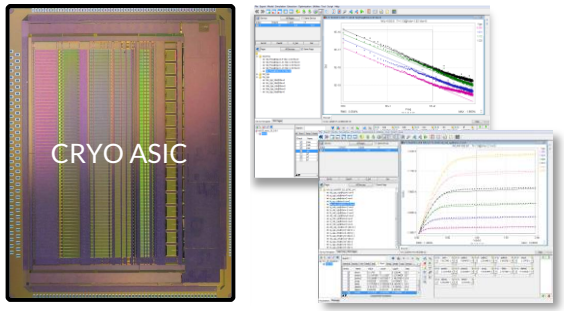
- Design leverage SLAC's expertise in:

GAMPix
Grid Activated Multiscale Pixel

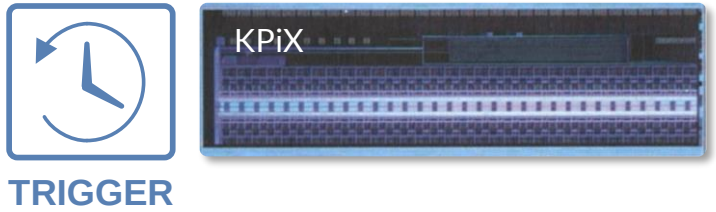
Low-Noise Performance
- Reticle-size pixelated ASICs
  ePix [3] and Spark-Pix families [4]



Cryogenic Operation
- System-on-Chip ASIC for neutrino applications
  CRYO ASIC [5-7] +
  Custom Cryogenic Models

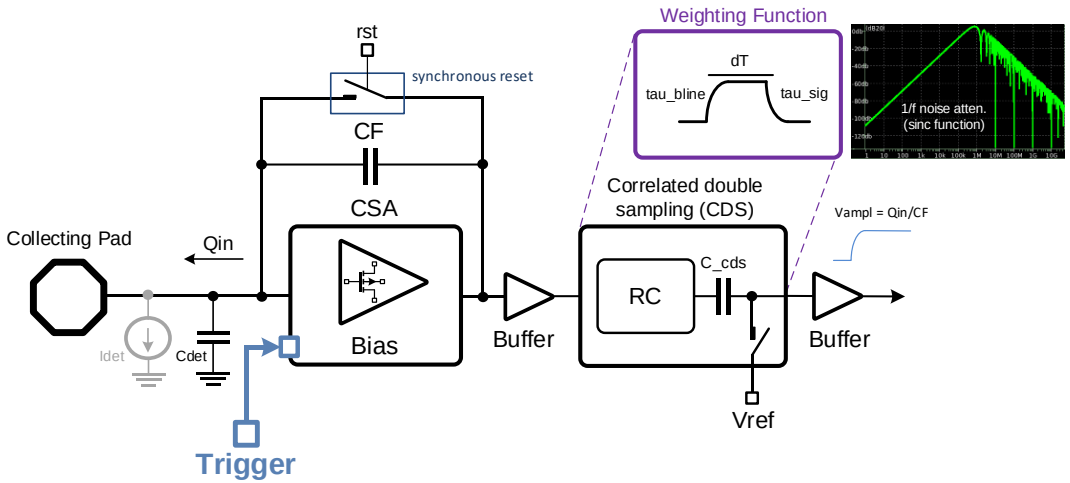


Fast Power Switching
- Power pulsed ASICs
  KPiX [8]



ASIC Readout Architectures

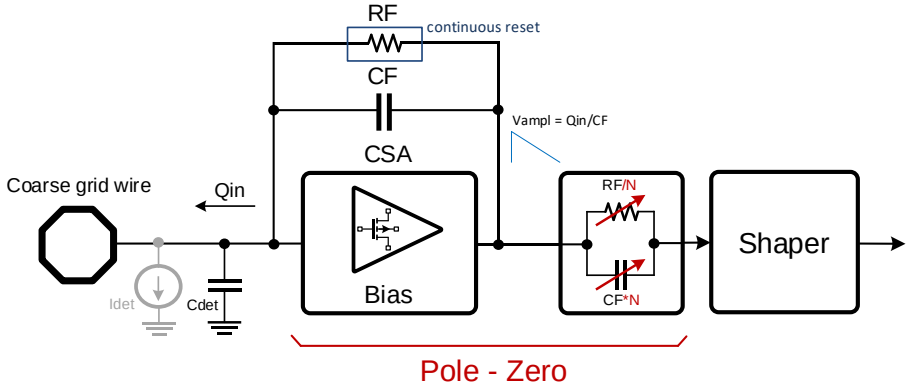
Pixel Readout: Synchronous-Reset



Key Features

- Scheme for duty cycle systems where signal arrival is defined → GAMPix
  - Widely used approach in our high-speed x-ray imager ASICs
- Compatible with a trigger signal
  - Would enable fast recovery times → Simple switch in feedback
- Correlated Double Sampling (CDS) mitigates CSA flicker, acts as shaper
- Preliminary noise (CSA only) is ~18e- at 87K with Cdet = 500fF

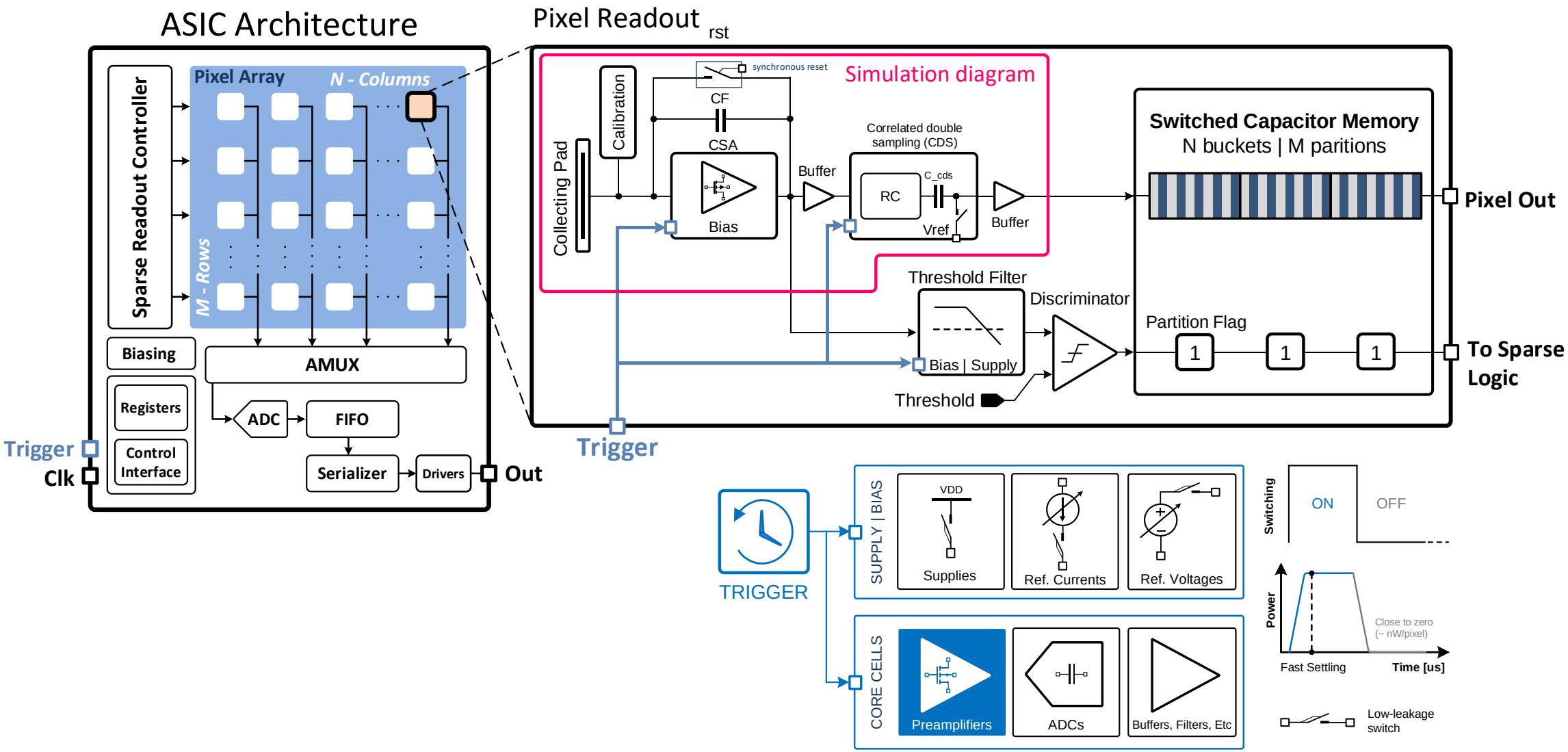
Coarse Grid Readout: Continuous-Reset



Key Features

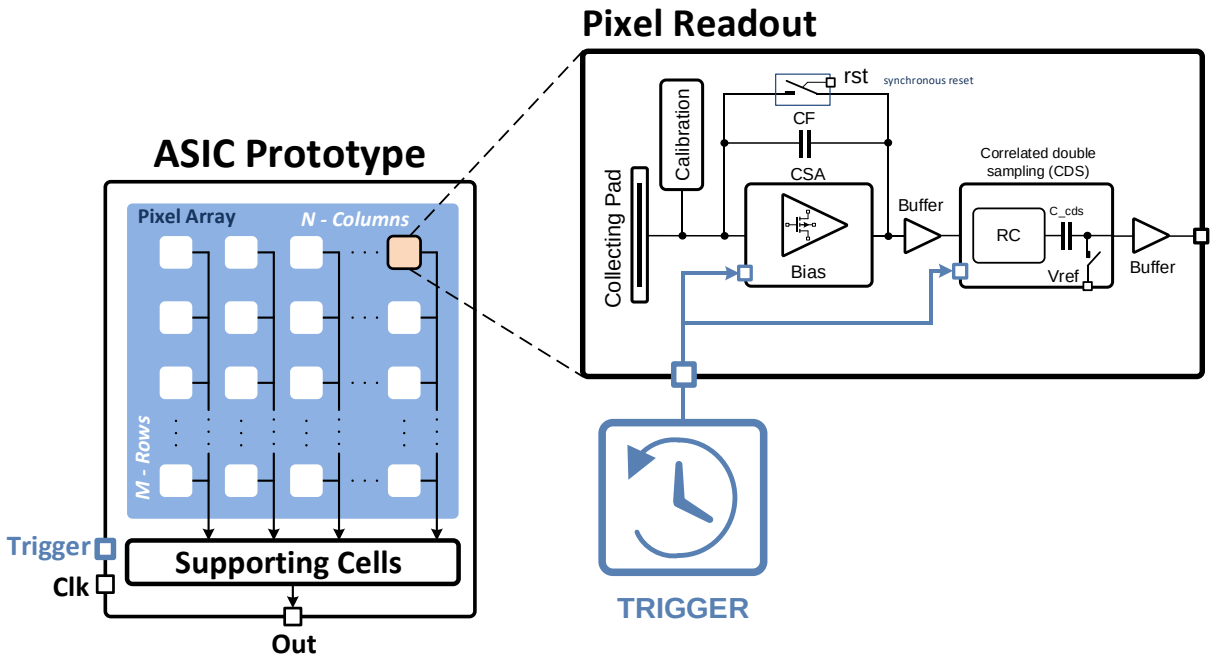
- Scheme for continuous data streaming systems and shaping of the signal
  - Scheme used in CRYO ASIC - A charge readout for LN TPCs
- Serves as trigger system for the pixel readout
- Pole-zero scheme with antialiasing filter (Bessel or Semi-Gaussian)
- Programmable shaping times
- Preliminary noise (CSA + Bessel) is ~40e- at 87K with Cdet = 2.5pF

ASIC Readout Architectures (Pixel Chip)



ASIC Readout Architectures

Development Plan – Phase I



Small R&D prototype [1-2]

- 5mm x 5mm proof-of-concept R&D prototype
- Design and fabrication in 130nm CMOS
  - Verification at 300K and 233K (foundry models)
  - Cold optimization (custom cryo models)
- Small matrix array of pixel readout
- Pixel architecture with low-noise and power-pulsed
- External trigger system
- Supporting electronics with reduced functions (i.e., bias, programming the device, etc.)
- **Goal -** Retire highest risks of the design: **Noise & low-power at 87K**

ASIC Readout Architectures

CSA-1

Folded with PMOS input

- Based on KPiX [8]
- Gain boosting (> 80dB)
- Power pulsed
- 2.0V supply
- Coarse electrode readout
- Low quiescent current
- For now, ideal bias

CSA-2

Class-C inverter-based

- Used in SD ADCs [9]
- Gain boosting (> 90dB)
- Power pulsed
- 2.0V supply
- Pixel readout
- Low quiescent current
- Initial biasing circuitry

Simulation conditions
CSA supply = 2.0V
CF = 4fF | Cdet = 500fF | Qin,max = ~1fC

Parameter AC frequency response	Simulation Across Temperatures							
	27 C (300 K) Foundry models		- 40 C (233 K) Foundry models		- 113 C (165 K) Custom cryogenic models		- 186 C (87 K) Custom cryogenic models	
Amplifier	**CSA-1** [1]	**CSA-2** [2]	**CSA-1** [1]	**CSA-2**	**CSA-1** [1]	**CSA-2**	**CSA-1** [1]	**CSA-2**
DC gain [dB]	86.43	86.03	90.43	92.38	89.75	98.07	79.13	102.39
Phase Margin [deg]	67.18	80.36	66.51	78.88	67.69	79.02	68.19	73.27
GBW [MHz]	139.17	94.02	148.75	111.94	131.42	134.03	152.88	147.26
ON-state [3] **Current consumption [uA]**	467.09	83.78	359.23	85.59	282.17	83.87	216.74	77.95
OFF-state **Current consumption [uA]**	A few pA, however, simulations with leakage current analysis are in progress							
Settling time after trigger [nsec]	< 500n	< 500n	< 500n	< 500n	< 500n	< 500n	< 500n	< 500n

[1,2] For now, ideal bias. Room for improvement to reduced quiescent current

ASIC Readout Architectures

Simulation conditions

CSA supply = 2.0V

CF = 4fF | Cdet = 500fF | Qin,max = ~1fC

Parameter Noise of CSA [e-]	Simulation Across Temperatures			
	27 C (300 K) Foundry models	- 40 C (233 K) Foundry models	- 113 C (165 K) Custom cryogenic models	- 186 C (87 K) Custom cryogenic models
Folded architecture [1]	~25	~23	~20	~18
Inverter-based architecture [2]	~28	~26	~24	~20

[1] Only noise of CSA is reported with ideal bias circuit

[2] Only noise of CSA is reported with preliminary biasing circuitry

5

Conclusions

Conclusions

- **GAMPix:** A fine-grained, low-noise and ultra-low power pixelated charge readout for NL TPCs
- Sub-millimeter tracking images
- Noise level < 50e-
- Triggered by the coarse grid: **meet the power budget and reduce the data volume**
- Energy resolution <1% for γ-TPC: electron tracks > 100keV, drift length < 30cm
- Provides drift length < 5% accuracy
- Application on γ-TPC in space and on DUNE
- GAMPix paper on arXiv:2402.00902
- Testing and development underway at SLAC
- Look for collaborating efforts with other groups!

References

1. T. Shutt et al. “Development of a novel readout system for a liquid Argon time projection chamber MeV Gamma-Ray Telescope”, 2021 NASA-APRA.
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3. A. Dragone, et al., “ePix: a class of architectures for second generation LCLS cameras”, Journal of Physics Conference Series.
4. L. Rota et al., “SparkPix-ED: a readout ASIC with 1 MHz frame-rate for rare event experiments at LCLS-II”, 2021 iWORID.
5. A. Peña-Perez et al., “CRYO: A System-on-Chip for Charge Readout in the nEXO Experiment”, 2022 IEEE NSS/MIC.
6. A. Peña-Perez et al., “CRYO: A System-On-Chip ASIC for Noble Liquid TPC Experiments”, 2020 IEEE NSS/MIC.
7. A. Gupta et al., “Read-Out Architecture of CRYO System-on-Chip ASIC for Noble Liquid TPC Detectors”, 2020 MWSCAS
8. J. Brau et al., "KPiX – A 1,024 channel readout ASIC for the ILC“, 2012 IEEE NSS/MIC.
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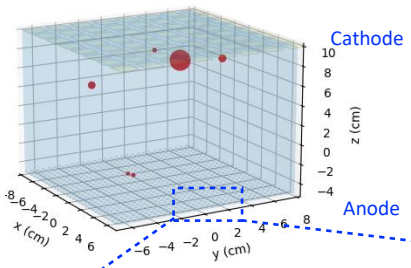
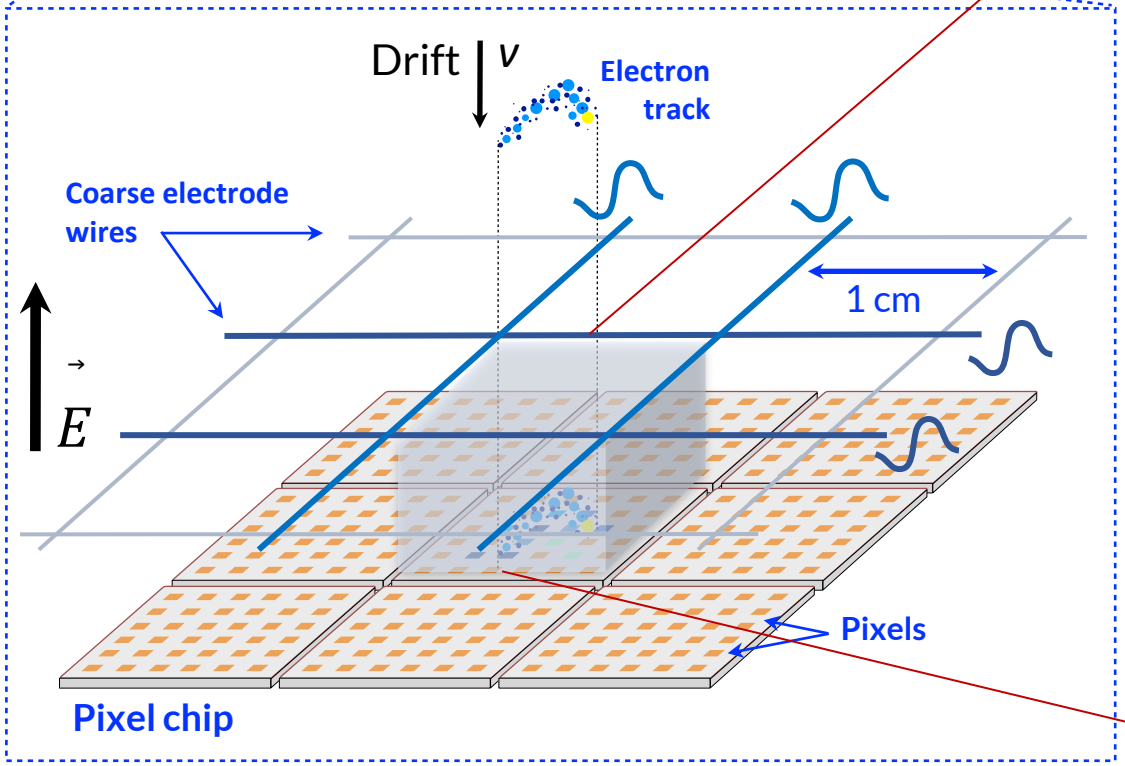
Backup Material

GAMPix Concept

TPC cell





Electric Fields in GAMPix Unit